1/4.5-Inch 1.6Mp CMOS Digital Image Sensor

MT9M032 Data Sheet

For the latest data sheet, refer to Aptina's Web site: www.aptina.com

Features

- Maximum frame rate (1284H x 812V/60 fps at 99 MHz)
- Superior low-light performance
- Low dark current
- Global reset release (GRR), which starts the exposure of all rows simultaneously
- Simple two-wire serial interface
- Programmable controls: gain, frame rate, frame size, exposure
- Horizontal and vertical mirror image
- Automatic black level calibration
- On-chip phase-locked loop (PLL) oscillator
- Bulb exposure mode for arbitrary exposure times
- Snapshot mode to take frames on demand
- Parallel data output
- Electronic rolling shutter (ERS), progressive scan
- Arbitrary image decimation with anti-aliasing
- Programmable I/O slew rate
- Programmable power-down mode (mode A or mode B)
- Xenon and LED flash support with fast exposure adaptation
- Flexible support for external auto focus, optical zoom, and mechanical shutter

Ordering Information

Table 1: Available Part Numbers

Part Number	Description
MT9M032C12STC	48-pin Pb-free CLCC/color
MT9M032C12STMU	48-pin Pb-free CLCC/mono

Table 2: Key Performance Parameters

Parameter		Value
Optical format		1/4.5-inch (4:3)
Active imager size		3.24mm(H) x 2.41mm(V)
Active pixels		1472H x 1096V
Pixel size		2.2 x 2.2µm
Color filter array		RGB Bayer pattern, mono
Shutter type		Global reset release (GRR) (snapshot only), electronic rolling shutter (ERS)
Maximum data rate/master clock		99 Mp/s / 49.5 MHz
Frame rate	1440H x 1080V	Programmable up to 30 fps
	1280H x 720V	Programmable up to 60 fps
ADC resolution		12-bit, on-chip
Responsivity		1.4 V/lux-sec (550nm) 2.1 V/lux-sec (monochrome)
Dynamic range		70.1dB
SNR_{MAX}		38.1dB
Supply voltage	Digital	1.7–1.9V
	I/O	2.6–3.1V
	PLL	2.6–3.1V
	Analog	2.6–3.1V
Power consumption		364.6mW at 2.8V
Operating temperature		–30°C to +70°C
Packaging		48-pin CLCC

Applications

- High definition surveillance camera
- High speed surveillance camera
- ePTZ camera

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General Description

The Aptina MT9M032 is a 1/4.5-inch format CMOS active-pixel digital image sensor with a pixel array of 1472H x 1096V. The default active imaging array size is 1440 x 1080. It incorporates sophisticated on-chip camera functions such as windowing, mirroring, and snapshot mode. It is programmable through a simple two-wire serial interface and has very low power consumption.

The MT9M032 digital image sensor features Aptina's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

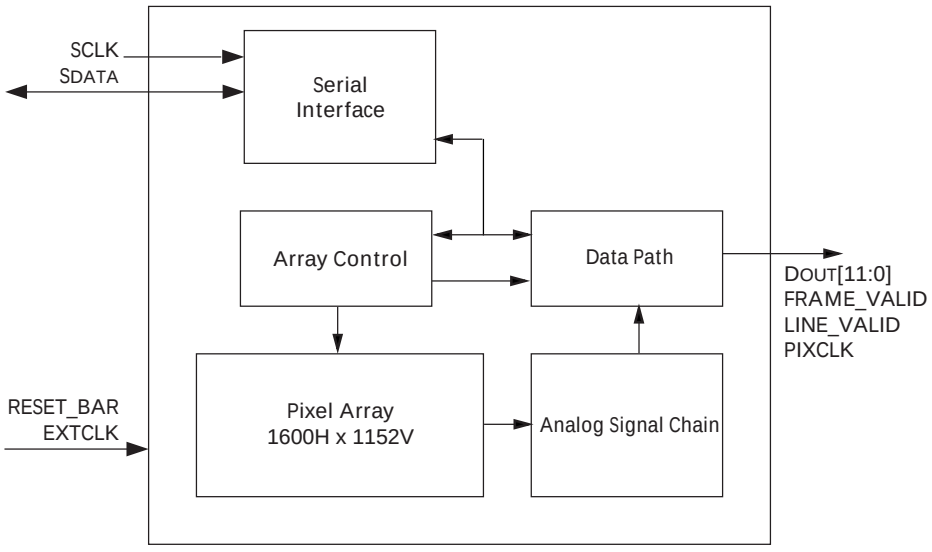
Functional Overview

The MT9M032 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) to generate all internal clocks from a single master input clock running between 8 and 16.5 MHz.

User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.6Mp active-pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light.

The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an ADC. The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The pixel data are output at a rate of up to 99 Mp/s, in addition to frame and line synchronization signals in parallel mode corresponding to a pixel clock rate of 99 MHz. Figure 1 shows the block diagram of the sensor.

Figure 1: Block Diagram – Parallel Output



The pixel array contains optically active and light-shielded (dark) pixels. The dark pixels are used to provide data for on-chip offset correction algorithms (black level control).

The sensor contains a set of control and status registers that can be used to control many aspects of the sensor behavior including the frame size, exposure, and gain setting. These registers can be accessed through a two-wire serial interface.

The output from the sensor (MT9M032C12STC) is a Bayer pattern; alternate rows are a sequence of either green and red pixels or blue and green pixels. The offset and gain stages of the analog signal chain provide per-color control of the pixel data.

A flash strobe output signal is provided to allow an external xenon or LED light source to synchronize with the sensor exposure time and to support the provision of an external mechanical shutter.

Signal Descriptions

Table 3 provides signal descriptions for the MT9M032.

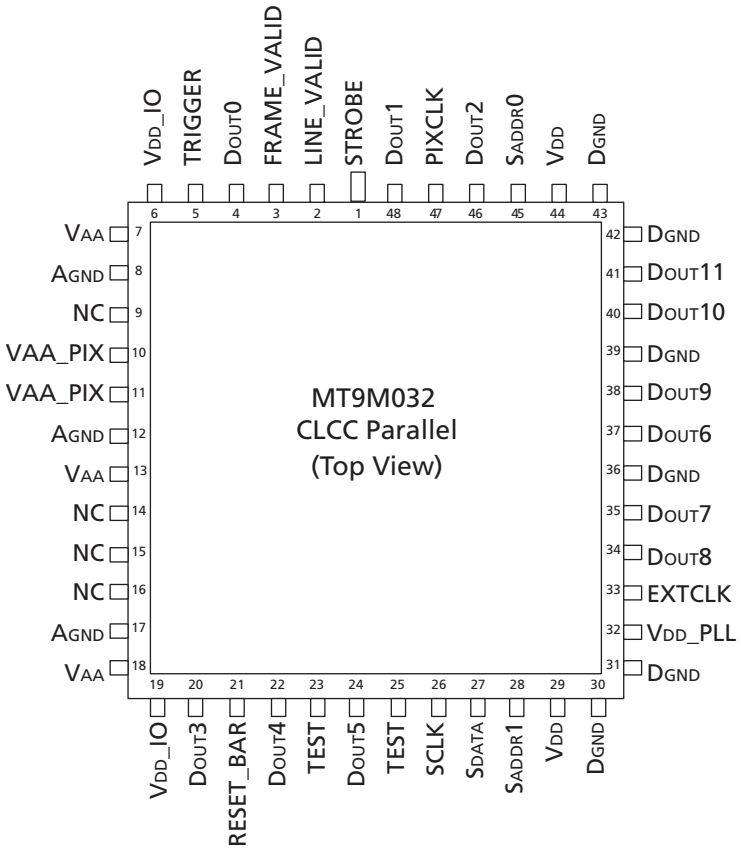
Table 1: Signal Descriptions

Pin Numbers	Name	Type	Description
26	SCLK	Input	Serial clock. Pull to VDD_IO with a 1.5kΩ resistor (depending on bus loading).
21	RESET_BAR	Input	Master reset signal, active LOW.
33	EXTCLK	Input	Input clock signal 8–49.5 MHz.
5	TRIGGER	Input	Snapshot trigger. Used to trigger one frame of output in snapshot modes.
23, 25	TEST	Input	Enables manufacturing test modes. Tie to digital GND for functional operation.
45	SADDR0	Input	Serial address. Pull to VDD_IO or DGND to set serial address.
28	SADDR1	Input	Serial address. Pull to VDD_IO or DGND to set serial address.
27	SDATA	I/O	Serial data. Pull to VDD_IO with a 1.5kΩ resistor (depending on bus loading).
1	STROBE	Output	Snapshot strobe. Driven HIGH when all pixels are exposing in snapshot modes.
4	DOUT[0]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
48	DOUT[1]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
46	DOUT[2]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
20	DOUT[3]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
22	DOUT[4]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
24	DOUT[5]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
37	DOUT[6]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
35	DOUT[7]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
34	DOUT[8]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
38	DOUT[9]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
40	DOUT[10]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
41	DOUT[11]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
47	PIXCLK	Output	Pixel clock. Used to qualify the LINE_VALID (LV), FRAME_VALID (FV), and DOUT(11:0). These outputs should be captured on the falling edge of this signal.
3	FRAME_VALID	Output	Frame valid. Qualified by PIXCLK. Driven HIGH during active pixels and horizontal blanking of each frame and LOW during vertical blanking.
2	LINE_VALID	Output	Line valid output. Qualified by PIXCLK. Driven HIGH with active pixels of each line and LOW during horizontal blanking periods. External pull-down resistor to DGND (typical 10kΩ–100kΩ) required for proper initialization sequence.
29, 44	VDD	Supply	Digital power 1.8V nominal.
10, 11	VAA_PIX	Supply	Pixel array power 2.8V nominal.
7, 13, 18	VAA	Supply	Analog power 2.8V nominal.
32	VDD_PLL	Supply	PLL power 2.8V nominal.
6, 19	VDD_IO	Supply	I/O power supply 2.8V nominal.

Table 1: Signal Descriptions (Continued)

Pin Numbers	Name	Type	Description
30, 31, 36, 39, 42, 43	DGND	Supply	Digital ground.
8, 12, 17	AGND	Supply	Analog ground.
9, 14, 15, 16	NC	–	No connect.

Figure 2: 48-Pin CLCC 10 x 10 Package Pinout Diagram (Top View)

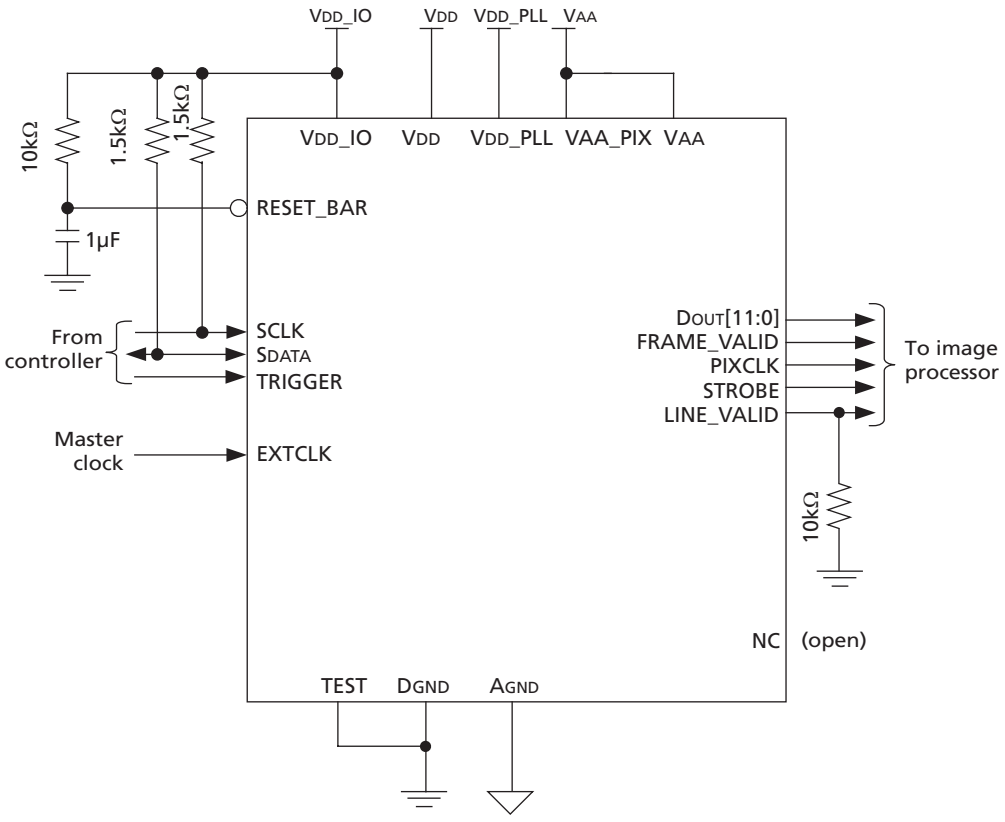


Typical Connections

Figure 3 shows typical connections for the MT9M032 sensor. For low-noise operation, the MT9M032 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled from ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

The MT9M032 also supports different digital core (VDD/DGND) and I/O power (VDD_IO/DGND) power domains that can be at different voltages. PLL requires a clean power source (VDD_PLL).

Figure 3: Typical Configuration



Notes:
1. Typical connection shows only one scenario out of multiple possible variations for this sensor.
2. All inputs must be configured with VDD_IO.
3. VAA and VAA_PIX must be tied together.

Pixel Array Structure

The MT9M032 pixel array consists of a 1600-column by 1152-row matrix of pixels addressed by column and row. The address (column 0, row 0) represents the upper-right corner of the entire array, looking at the sensor, as shown in Figure 4.

The array consists of a 1440-column by 1080-row active region in the center representing the default output image resolution, surrounded by a boundary region (also active), surrounded by a border of dark pixels (see Table 2 and Table 3). The boundary region can be used to avoid edge effects when doing color processing, while the optically black column and rows can be used to monitor the black level.

Table 2: Pixel Type by Column

Column	Pixel Type
0–15	Active boundary (16)
16–1455	Active image (1440)
1456–1471	Active boundary (16)
1472–1599	Black (128)

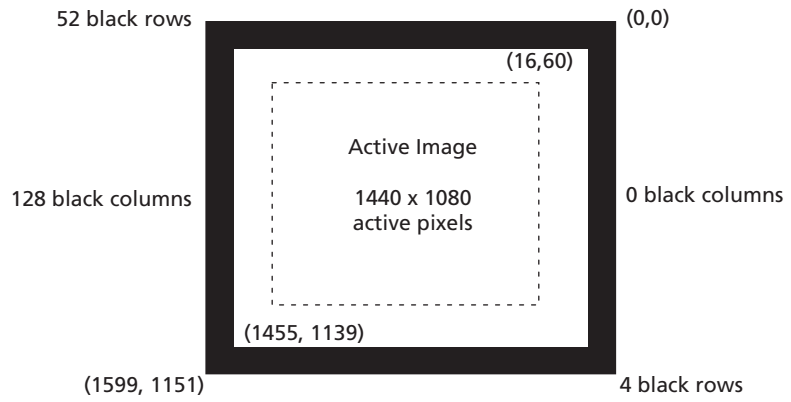
Table 3: Pixel Type by Row

Row	Pixel Type
0–51	Black (52)
53–59	Active boundary (8)
60–1139	Active image (1080)
1140–1147	Active boundary (8)
1148–1151	Black (4)

Default Readout Order

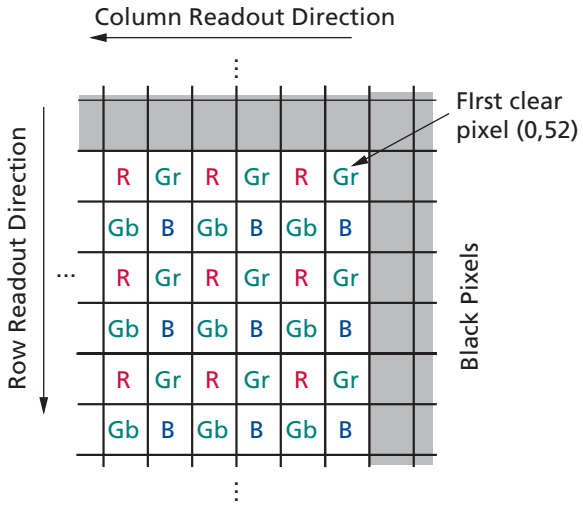
By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 4). This reflects the actual layout of the array on the die. Also, the first pixel data read out of the sensor in default condition is that of pixel (16,60).

Figure 4: Pixel Array Description



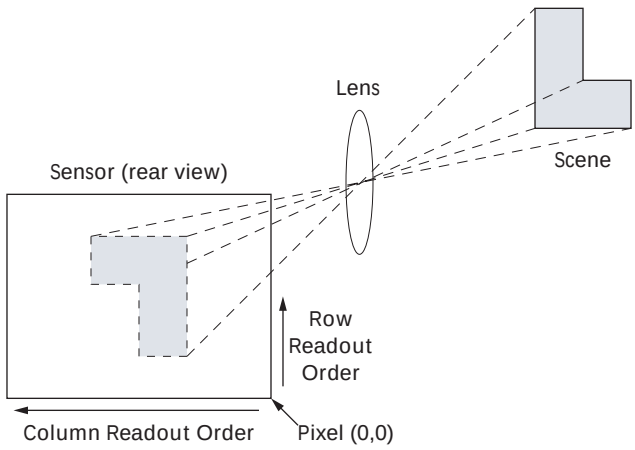
Sensor pixels are output in a Bayer pattern format consisting of four "colors"—GreenR, GreenB, Red, and Blue (Gr, Gb, R, B)—representing three filter colors. When no mirror modes are enabled, even-numbered rows contain alternate greenR and red pixels; odd-numbered rows contain alternate blue and greenB pixels. Even-numbered columns contain greenR and blue pixels; odd-numbered columns contain red and greenB pixels. The GreenR and GreenB pixels have the same color filter, but they are treated as separate colors by the data path and analog signal chain.

Figure 5: Pixel Color Pattern Detail (Top Right Corner)



When the sensor is imaging, the active surface of the sensor faces the scene, as shown in Figure 6. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced, as shown in Figure 5.

Figure 6: Imaging a Scene

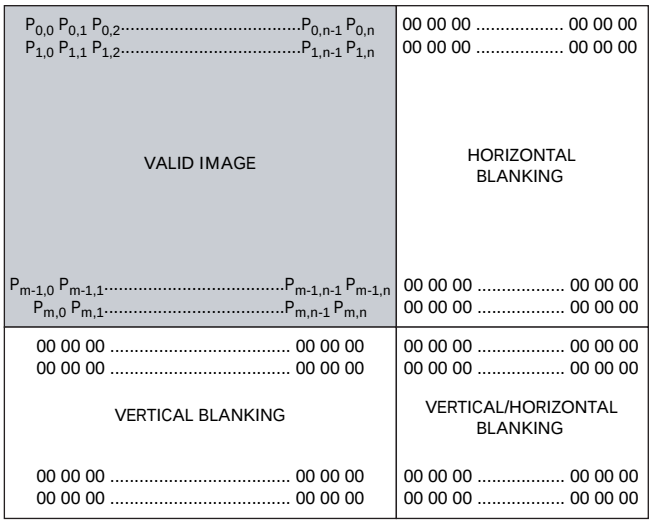


Output Data Format

Parallel Pixel Data Interface

MT9M032 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 7. The amount of horizontal blanking and vertical blanking is programmable; LV is HIGH during the shaded region of the figure. FV timing is described in the next section.

Figure 7: Spatial Illustration of Image Readout



Output Data Timing

The sensor core output data is synchronized with the PIXCLK output. When LV is HIGH, one pixel data is output on the 12-bit DOUT output every PIXCLK period. By default, the internal PLL is used and PIXCLK runs at the 2X master clock. The falling edge of PIXCLK appears at the center of the DOUT. This allows PIXCLK to be used as a clock to sample the data.

By default, PIXCLK is not enabled, and its on or off is register controllable. When on, PIXCLK is continuously enabled, even during the blanking period. The MT9M032 can be programmed to delay the PIXCLK edge relative to the DOUT transitions. This can be achieved by programming the corresponding register bits.

Figure 8: Pixel Data Timing Example

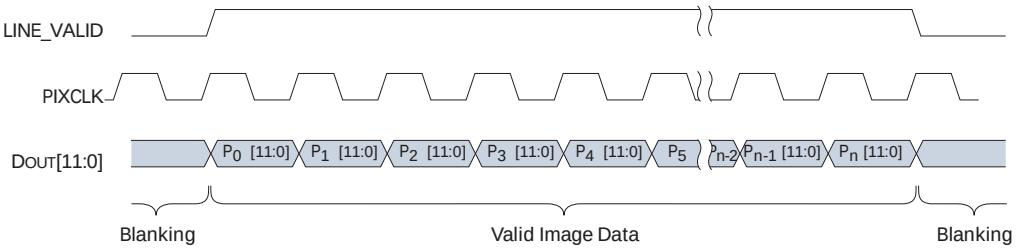
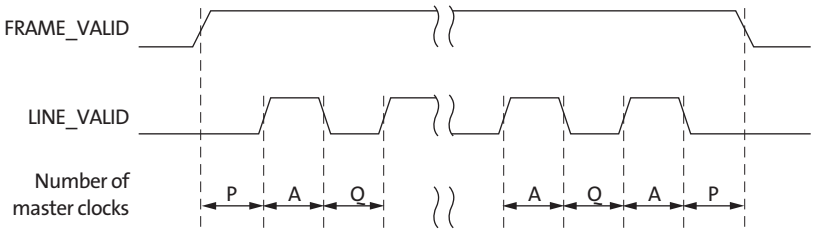


Figure 9: Row Timing and FV/LV Signals

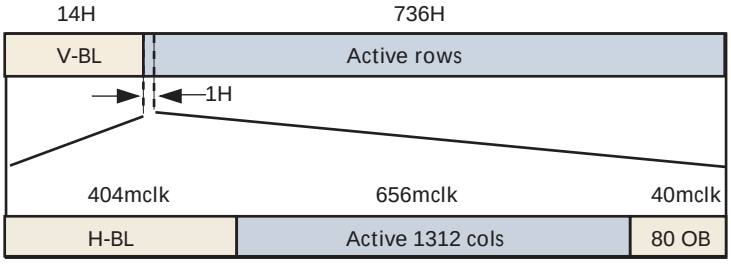


The sensor timing is shown in terms of pixel clock and master clock cycles (Figure 8 and Figure 9).

Row Timing Details

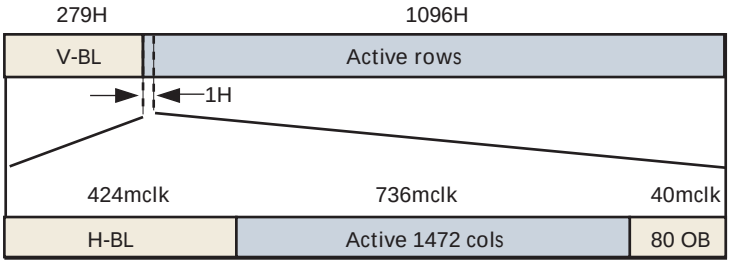
This section discusses the row timing details for 1440 x 1080 30 fps and 1280 x 720 60 fps modes. In Figure 10 and Figure 11, H-BL is horizontal blanking, OB is optically black columns, H is one row, and V-BL is vertical blanking. The internal master clock (MCLK) frequency is half the pixel clock (PCLK) frequency (PCLK = 99 MHz, MCLK = 49.5 MHz). Each PCLK outputs one active pixel or one black pixel. H-BL setting value uses MCLK as a unit (one horizontal blank needs two PCLKs).

Figure 10: 1280 x 720/60 fps Row Timing Details



- mclk = 49.5 MHz
  H = H-BL + Active Cols/2+ OB/2
  H = 404 mclks + 656 mclks + 40 mclks = 1100 mclks = 22.22µs
- V = 14H + 736H = 750H
  ^{t}FRAME = H x V
  = 1100 x 750 = 825000 mclks = 825000 mclks/49.5 MHz = 16.66ms
- Frame rate = 1/^{t}FRAME
  = 1/16.66ms = 60 fps
- Active readout window is 1312 (1280 + 32 boundary) columns x 736 (720 + 16 boundary) rows

Figure 11: 1440 x 080/30 fps Mode



- mclk = 49.5 MHz
- H = H-BL + Active Cols/2 + OB/2
  = 424 clks + 736 mclks + 40 mclks = 1200 mclks = 24.24µs
- V = 279H + 1096H = 1375H
- ^{t}FRAME = H x V
  = 1200 x 1375 = 1650000 mclks = 1650000 mclks/49.5 MHz = 33.33ms
- Frame rate = 1/^{t}FRAME
  = 1/33.33ms = 30 fps

Active readout window is 1472 (1440 + 32 boundary) columns x 1096 (1080 + 16 boundary) rows

Serial Bus Description

Registers are written to and read from the MT9M032 through the two-wire serial interface bus. The MT9M032 is a serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out of the MT9M032 through the serial data (SDATA) line. The SDATA line is pulled up to VDD_IO off-chip by a 1.5kΩ resistor. Either the slave or master device can pull the SDATA line LOW—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial defines several different transmission codes, as shown in the following sequence:

1. a start bit
2. the slave device 8-bit address
3. an (a no) acknowledge bit
4. an 8-bit message
5. a stop bit

Sequence

A typical READ or WRITE sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request is a READ or a WRITE, where a “0” indicates a WRITE and a “1” indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a WRITE, the master then transfers the 8-bit register address to which a WRITE should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The MT9M032 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address, just as in the WRITE request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is automatically incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A "0" in the LSB (least significant bit) of the address indicates write mode (0xB8), and a "1" indicates read mode (0xB9).

The two-wire serial interface device addresses consists of 7 bits. For the MT9M032 sensor, the device is fixed at [1011100].

For the CLCC package, the MT9M032 allows for multiple device addresses in Master/slave mode as shown in Table 4. The 2 LSBs of the device address are defined by SADDR0 and SADDR1 input port values.

Table 4: Device Addresses

SADDR1	SADDR0	Device Address
0	0	0xB8
0	1	0xBA
1	0	0xBC
1	1	0xBE

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

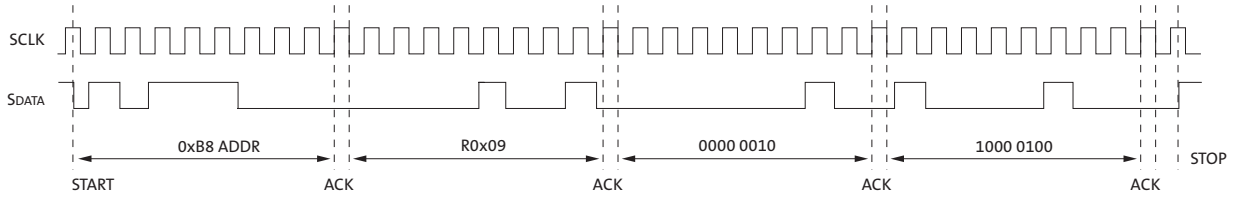
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample Write and Read Sequences

16-Bit Write Sequence

A typical WRITE sequence for writing 16 bits to a register is shown in Figure 12. A start bit given by the master, followed by the write address, starts the sequence. The image sensor then sends an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each 8-bit transfer, the image sensor sends an acknowledge bit. All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

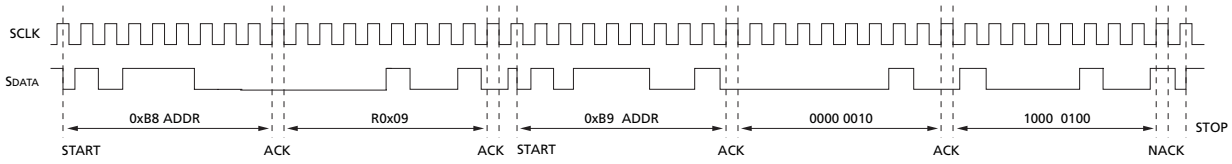
Figure 12: Timing Diagram Showing a Write to R0x09 with the Value 0x0284



16-Bit Read Sequence

A typical READ sequence is shown in Figure 13. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specify that a READ is about to happen from the register. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Figure 13: Timing Diagram Showing a Read from R0x09; Returned Value 0x0284



Registers

Register Map

Register Notation

In this document, registers are described either by address or by name. Table 5 on page 20 and Table 6 on page 25 show the locations used within the address space. Locations that are not shown in the table are reserved for future use; they should not be read from or written to in order to maintain compatibility with future designs. Locations that are shown as "Reserved" should not be accessed. The default read values of these registers is subject to change.

Caution **The effect of writing to reserved registers is undefined and may include the possibility of causing permanent electrical damage to the sensor.**

Bit Fields

Some registers provide control of several different pieces of related functionality, and this makes it necessary to refer to bit fields within registers. As an example of the notation used for this, the least significant 4 bits of the chip version register are referred to as R0x0000[3:0].

Frame Sync'd

Frame start is defined as the point at which the first dark row is read out internally to the sensor. In the register tables the "Sync'd" column shows which registers or register fields are Frame Sync'd (with F attributes).

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame.Many changes to the sensor register settings can cause a bad frame. For example, when Row Size (R0x003) is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row size, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. If the masked bad frame option is enabled, both LV and FV are inhibited for these frames so that the vertical blanking time between frames is extended by the frame time. In the register tables, the "Bad Frame" column shows where changing a register or register field will cause a bad frame (with BF attributes). The following notation is used:

N—No. Changing the register value will not produce a bad frame.

Y—Yes. Changing the register value might produce a bad frame.

Register List and Default Values

Table 5: Core Register – Register List and Default Values

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic; – = undefined after reset

Register Number Dec (Hex)	Register Description	Data Format (Binary)	Default Value Dec (Hex)
R0:0(R0x000)	Chip Version	???? ???? ???? ????	5122 (0x1402)
R1:0(R0x001)	Row Start	0000 0ddd dddd dddd	60 (0x003C)
R2:0(R0x002)	Column Start	0000 dddd dddd dddd	16 (0x0010)
R3:0(R0x003)	Row Size	0000 0ddd dddd dddd	1079 (0x0437)
R4:0(R0x004)	Column Size	0000 dddd dddd dddd	1439 (0x059F)
R5:0(R0x005)	Horizontal Blank	0000 dddd dddd dddd	0 (0x0000)
R6:0(R0x006)	Vertical Blank	0000 0ddd dddd dddd	8 (0x0008)
R7:0(R0x007)	Output Control	dd0d dddd dddd dddd	40834 (0x9F82)
R8:0(R0x008)	Shutter Width Upper	0ddd dddd 0000 dddd	0 (0x0000)
R9:0(R0x009)	Shutter Width Lower	dddd dddd dddd dddd	800 (0x0320)
R10:0(R0x00A)	Pixel Clock Control	d0dd 0ddd 0ddd dddd	0 (0x0000)
R11:0(R0x00B)	Restart	0000 0000 0000 dddd	0 (0x0000)
R12:0(R0x00C)	Shutter Delay	000d dddd dddd dddd	0 (0x0000)
R13:0(R0x00D)	Reset	0000 0000 0000 000d	0 (0x0000)
R15:0(R0x00F)	Reserved	–	0 (0x0000)
R16:0(R0x010)	Reserved	–	83 (0x0053)
R17:0(R0x011)	PLL Config 1	dddd dddd 00dd dddd	15364 (0x3C04)
R18:0(R0x012)	Reserved	–	0 (0x0000)
R20:0(R0x014)	Reserved	–	54 (0x0036)
R21:0(R0x015)	Reserved	–	16 (0x0010)
R30:0(R0x01E)	Read Mode 1	dddd dddd dddd dddd	326 (0x0146)
R32:0(R0x020)	Read Mode 2	dddd d000 0ddd dddd	64 (0x0040)
R34:0(R0x022)	Reserved	–	0 (0x0000)
R35:0(R0x023)	Reserved	–	0 (0x0000)
R36:0(R0x024)	Reserved	–	2 (0x0002)
R37:0(R0x025)	Reserved	–	518 (0x0206)
R38:0(R0x026)	Reserved	–	151 (0x0097)
R39:0(R0x027)	Reserved	–	11 (0x000B)
R41:0(R0x029)	Reserved	–	1153 (0x0481)
R42:0(R0x02A)	Reserved	–	4230 (0x1086)
R43:0(R0x02B)	Green1 Gain	0ddd dddd dddd dddd	16 (0x0010)
R44:0(R0x02C)	Blue Gain	0ddd dddd dddd dddd	16 (0x0010)
R45:0(R0x02D)	Red Gain	0ddd dddd dddd dddd	16 (0x0010)
R46:0(R0x02E)	Green2 Gain	0ddd dddd dddd dddd	16 (0x0010)
R48:0(R0x030)	Reserved	–	0 (0x0000)
R50:0(R0x032)	Reserved	–	0 (0x0000)
R53:0(R0x035)	Global Gain	dddd dddd dddd dddd	16 (0x0010)
R60:0(R0x03C)	Reserved	–	26 (0x001A)
R61:0(R0x03D)	Reserved	–	7 (0x0007)
R62:0(R0x03E)	Reserved	–	135 (0x0087)
R63:0(R0x03F)	Reserved	–	0 (0x0000)

Table 5: Core Register – Register List and Default Values (Continued)

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic; – = undefined after reset

Register Number Dec (Hex)	Register Description	Data Format (Binary)	Default Value Dec (Hex)
R64:0(R0x040)	Reserved	–	7 (0x0007)
R65:0(R0x041)	Reserved	–	3 (0x0003)
R66:0(R0x042)	Reserved	–	5 (0x0005)
R67:0(R0x043)	Reserved	–	1 (0x0001)
R68:0(R0x044)	Reserved	–	515 (0x0203)
R69:0(R0x045)	Reserved	–	4112 (0x1010)
R70:0(R0x046)	Reserved	–	4112 (0x1010)
R71:0(R0x047)	Reserved	–	4112 (0x1010)
R72:0(R0x048)	Reserved	–	16 (0x0010)
R73:0(R0x049)	Row Black Target	0000 dddd dddd dddd	168 (0x00A8)
R74:0(R0x04A)	Reserved	–	16 (0x0010)
R75:0(R0x04B)	Row Black Default Offset	0000 dddd dddd dddd	40 (0x0028)
R76:0(R0x04C)	Reserved	–	16 (0x0010)
R77:0(R0x04D)	Reserved	–	38 (0x0026)
R78:0(R0x04E)	Reserved	–	4112 (0x1010)
R79:0(R0x04F)	Reserved	–	23 (0x0017)
R80:0(R0x050)	Reserved	–	32768 (0x8000)
R81:0(R0x051)	Reserved	–	7 (0x0007)
R82:0(R0x052)	Reserved	–	32768 (0x8000)
R83:0(R0x053)	Reserved	–	7 (0x0007)
R84:0(R0x054)	Reserved	–	8 (0x0008)
R86:0(R0x056)	Reserved	–	32 (0x0020)
R87:0(R0x057)	Reserved	–	10 (0x000A)
R88:0(R0x058)	Reserved	–	32768 (0x8000)
R89:0(R0x059)	Reserved	–	7 (0x0007)
R90:0(R0x05A)	Reserved	–	7 (0x0007)
R91:0(R0x05B)	BLC_Sample_Size	0000 0000 0000 000d	1 (0x0001)
R92:0(R0x05C)	BLC_Tune_1	0000 dddd dddd dddd	90 (0x005A)
R93:0(R0x05D)	BLC_Delta_Thresholds	0ddd dddd 0ddd dddd	11539 (0x2D13)
R94:0(R0x05E)	BLC_Tune_2	0ddd 000d dddd dddd	16895 (0x41FF)
R95:0(R0x05F)	BLC_Target_Thresholds	0ddd dddd 0ddd dddd	8989 (0x231D)
R96:0(R0x060)	Green1_Offset	0000 000d dddd dddd	32 (0x0020)
R97:0(R0x061)	Green2_Offset	0000 000d dddd dddd	32 (0x0020)
R98:0(R0x062)	Black_Level_Calibration	dddd d000 0000 00dd	0 (0x0000)
R99:0(R0x063)	Red_Offset	0000 000d dddd dddd	32 (0x0020)
R100:0(R0x064)	Blue_Offset	0000 000d dddd dddd	32 (0x0020)
R101:0(R0x065)	Reserved	–	0 (0x0000)
R104:0(R0x068)	Reserved	–	0 (0x0000)
R105:0(R0x069)	Reserved	–	0 (0x0000)
R106:0(R0x06A)	Reserved	–	0 (0x0000)
R107:0(R0x06B)	Reserved	–	0 (0x0000)
R108:0(R0x06C)	Reserved	–	0 (0x0000)
R109:0(R0x06D)	Reserved	–	0 (0x0000)
R112:0(R0x070)	Reserved	–	124 (0x007C)

Table 5: Core Register – Register List and Default Values (Continued)

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic;
– = undefined after reset

Register Number Dec (Hex)	Register Description	Data Format (Binary)	Default Value Dec (Hex)
R113:0(R0x071)	Reserved	–	31492 (0x7B04)
R114:0(R0x072)	Reserved	–	30726 (0x7806)
R115:0(R0x073)	Reserved	–	5128 (0x1408)
R116:0(R0x074)	Reserved	–	5642 (0x160A)
R117:0(R0x075)	Reserved	–	13836 (0x360C)
R118:0(R0x076)	Reserved	–	19000 (0x4A38)
R119:0(R0x077)	Reserved	–	19510 (0x4C36)
R120:0(R0x078)	Reserved	–	30544 (0x7750)
R121:0(R0x079)	Reserved	–	31234 (0x7A02)
R122:0(R0x07A)	Reserved	–	30980 (0x7904)
R123:0(R0x07B)	Reserved	–	30726 (0x7806)
R124:0(R0x07C)	Reserved	–	30726 (0x7806)
R125:0(R0x07D)	Reserved	–	31744 (0x7C00)
R126:0(R0x07E)	Reserved	–	31240 (0x7A08)
R127:0(R0x07F)	Reserved	–	31236 (0x7A04)
R128:0(R0x080)	Reserved	–	25 (0x0019)
R129:0(R0x081)	Reserved	–	5892 (0x1704)
R130:0(R0x082)	Reserved	–	0 (0x0000)
R131:0(R0x083)	Reserved	–	5638 (0x1606)
R132:0(R0x084)	Reserved	–	7432 (0x1D08)
R134:0(R0x086)	Reserved	–	4870 (0x1306)
R135:0(R0x087)	Reserved	–	4360 (0x1108)
R144:0(R0x090)	Reserved	–	1140 (0x0474)
R145:0(R0x091)	Reserved	–	0 (0x0000)
R146:0(R0x092)	Reserved	–	1 (0x0001)
R147:0(R0x093)	Reserved	–	0 (0x0000)
R148:0(R0x094)	Reserved	–	10510 (0x290E)
R154:0(R0x09A)	Reserved	–	0 (0x0000)
R155:0(R0x09B)	Reserved	–	0 (0x0000)
R156:0(R0x09C)	Reserved	–	0 (0x0000)
R157:0(R0x09D)	Formatter0	dddd dddd dddd dddd	8789 (0x2255)
R158:0(R0x09E)	Formatter1	000d 00dd 00dd dddd	286 (0x011E)
R159:0(R0x09F)	Formatter2	dddd 0000 0111 0001	113 (0x0071)
R160:0(R0x0A0)	Reserved	–	0 (0x0000)
R161:0(R0x0A1)	Reserved	–	0 (0x0000)
R162:0(R0x0A2)	Reserved	–	0 (0x0000)
R163:0(R0x0A3)	Reserved	–	0 (0x0000)
R164:0(R0x0A4)	Reserved	–	0 (0x0000)
R165:0(R0x0A5)	Reserved	–	0 (0x0000)
R166:0(R0x0A6)	Reserved	–	0 (0x0000)
R167:0(R0x0A7)	Reserved	–	0 (0x0000)
R168:0(R0x0A8)	Reserved	–	0 (0x0000)
R169:0(R0x0A9)	Reserved	–	0 (0x0000)
R170:0(R0x0AA)	Reserved	–	0 (0x0000)

Table 5: Core Register – Register List and Default Values (Continued)

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic; – = undefined after reset

Register Number Dec (Hex)	Register Description	Data Format (Binary)	Default Value Dec (Hex)
R171:0(R0x0AB)	Reserved	–	0 (0x0000)
R172:0(R0x0AC)	Reserved	–	0 (0x0000)
R173:0(R0x0AD)	Reserved	–	0 (0x0000)
R174:0(R0x0AE)	Reserved	–	32 (0x0020)
R175:0(R0x0AF)	Reserved	–	0 (0x0000)
R176:0(R0x0B0)	Reserved	–	0 (0x0000)
R177:0(R0x0B1)	Reserved	–	0 (0x0000)
R178:0(R0x0B2)	Reserved	–	0 (0x0000)
R179:0(R0x0B3)	Reserved	–	0 (0x0000)
R180:0(R0x0B4)	Reserved	–	0 (0x0000)
R181:0(R0x0B5)	Reserved	–	0 (0x0000)
R182:0(R0x0B6)	Reserved	–	0 (0x0000)
R183:0(R0x0B7)	Reserved	–	0 (0x0000)
R184:0(R0x0B8)	Reserved	–	0 (0x0000)
R185:0(R0x0B9)	Reserved	–	0 (0x0000)
R186:0(R0x0BA)	Reserved	–	0 (0x0000)
R187:0(R0x0BB)	Reserved	–	0 (0x0000)
R188:0(R0x0BC)	Reserved	–	0 (0x0000)
R189:0(R0x0BD)	Reserved	–	0 (0x0000)
R190:0(R0x0BE)	Reserved	–	0 (0x0000)
R191:0(R0x0BF)	Reserved	–	0 (0x0000)
R192:0(R0x0C0)	Reserved	–	0 (0x0000)
R193:0(R0x0C1)	Reserved	–	0 (0x0000)
R194:0(R0x0C2)	Reserved	–	0 (0x0000)
R195:0(R0x0C3)	Reserved	–	0 (0x0000)
R196:0(R0x0C4)	Reserved	–	0 (0x0000)
R197:0(R0x0C5)	Reserved	–	0 (0x0000)
R198:0(R0x0C6)	Reserved	–	0 (0x0000)
R199:0(R0x0C7)	Reserved	–	0 (0x0000)
R200:0(R0x0C8)	Reserved	–	0 (0x0000)
R201:0(R0x0C9)	Reserved	–	0 (0x0000)
R202:0(R0x0CA)	Reserved	–	0 (0x0000)
R203:0(R0x0CB)	Reserved	–	0 (0x0000)
R204:0(R0x0CC)	Reserved	–	0 (0x0000)
R205:0(R0x0CD)	Reserved	–	0 (0x0000)
R206:0(R0x0CE)	Reserved	–	0 (0x0000)
R207:0(R0x0CF)	Reserved	–	0 (0x0000)
R208:0(R0x0D0)	Reserved	–	0 (0x0000)
R209:0(R0x0D1)	Reserved	–	0 (0x0000)
R210:0(R0x0D2)	Reserved	–	0 (0x0000)
R211:0(R0x0D3)	Reserved	–	0 (0x0000)
R212:0(R0x0D4)	Reserved	–	0 (0x0000)
R213:0(R0x0D5)	Reserved	–	0 (0x0000)
R214:0(R0x0D6)	Reserved	–	0 (0x0000)

Table 5: Core Register – Register List and Default Values (Continued)

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic; – = undefined after reset

Register Number Dec (Hex)	Register Description	Data Format (Binary)	Default Value Dec (Hex)
R215:0(R0x0D7)	Reserved	–	0 (0x0000)
R216:0(R0x0D8)	Reserved	–	0 (0x0000)
R217:0(R0x0D9)	Reserved	–	0 (0x0000)
R218:0(R0x0DA)	Reserved	–	0 (0x0000)
R219:0(R0x0DB)	Reserved	–	0 (0x0000)
R220:0(R0x0DC)	Reserved	–	0 (0x0000)
R221:0(R0x0DD)	Reserved	–	0 (0x0000)
R222:0(R0x0DE)	Reserved	–	0 (0x0000)
R223:0(R0x0DF)	Reserved	–	0 (0x0000)
R224:0(R0x0E0)	Reserved	–	0 (0x0000)
R225:0(R0x0E1)	Reserved	–	0 (0x0000)
R226:0(R0x0E2)	Reserved	–	0 (0x0000)
R227:0(R0x0E3)	Reserved	–	0 (0x0000)
R228:0(R0x0E4)	Reserved	–	0 (0x0000)
R229:0(R0x0E5)	Reserved	–	0 (0x0000)
R230:0(R0x0E6)	Reserved	–	0 (0x0000)
R231:0(R0x0E7)	Reserved	–	0 (0x0000)
R232:0(R0x0E8)	Reserved	–	0 (0x0000)
R233:0(R0x0E9)	Reserved	–	0 (0x0000)
R234:0(R0x0EA)	Reserved	–	0 (0x0000)
R235:0(R0x0EB)	Reserved	–	0 (0x0000)
R236:0(R0x0EC)	Reserved	–	0 (0x0000)
R237:0(R0x0ED)	Reserved	–	0 (0x0000)
R238:0(R0x0EE)	Reserved	–	0 (0x0000)
R239:0(R0x0EF)	Reserved	–	0 (0x0000)
R240:0(R0x0F0)	Reserved	–	0 (0x0000)
R241:0(R0x0F1)	Reserved	–	0 (0x0000)
R248:0(R0x0F8)	Reserved	–	1 (0x0001)
R250:0(R0x0FA)	Reserved	–	0 (0x0000)
R251:0(R0x0FB)	Reserved	–	0 (0x0000)
R252:0(R0x0FC)	Reserved	–	0 (0x0000)
R253:0(R0x0FD)	Reserved	–	0 (0x0000)
R255:0(R0x0FF)	Chip_Version_Alt	???? ???? ???? ????	5122 (0x1402)

Register Descriptions

Table 6: Core Registers – Register Description
R/W (Read or Write) bit; RO (Read Only) bit

Register Number Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R0:0 R0x000	15:0	0x1402	Chip Version (RO)		
	Chip version.				
R1:0 R0x001	15:0	0x003C	Row Start (R/W)	Y	Y
	The Y coordinate of the upper-left corner of the FOV. If this register is set to an odd value, the next lower even value will be used.				
R2:0 R0x002	15:0	0x0010	Column Start (R/W)	Y	N
	The X coordinate of the upper-left corner of the FOV.				
R3:0 R0x003	15:0	0x0437	Row Size (R/W)	Y	Y
	The height of the FOV minus one. If this register is set to an even value, the next higher odd value will be used.				
R4:0 R0x004	15:0	0x059F	Column Size (R/W)	Y	Y
	The width of the FOV minus one. If this register is set to an even value, the next higher odd value will be used.				
R5:0 R0x005	15:0	0x0000	Horizontal Blank (R/W)	Y	Y
	Extra time added to the end of each row, in pixel clocks. Incrementing this register will increase exposure and decrease frame rate. Setting a value less than the minimum will use the minimum horizontal blank. The minimum horizontal blank depends on the mode of the sensor.				
R6:0 R0x006	15:0	0x0008	Vertical Blank (R/W)	Y	N
	Extra time added to the end of each frame in rows minus one. Incrementing this register will decrease frame rate, but not affect exposure. Setting a value less than the minimum will use the minimum vertical blank.				
R7:0 R0x007	15:0	0x9F82	Output Control (R/W)		
	15	0x0001	Reserved		
	14	0x0000	Reserved		
	13	X	Reserved		
	12:10	0x0007	Reserved		
	9:7	0x0007	Reserved		
	6	0x0000	Reserved		
	5:4	X	Reserved		
	3	0x0000	Reserved		
	2	0x0000	Reserved		

Table 6: Core Registers – Register Description (Continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Number Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R7:0 R0x007	1	0x0001	Chip Enable When this bit is cleared, sensor readout is stopped and analog circuitry is put in a state which draws minimal power. When this bit is set, the chip operates according to the current mode. Writing this bit does not affect the values of any other registers. Mirrored on R241[0]. To protect Chip Enable operation from abnormal color shift, apply the following procedure: before Chip Enable is cleared, set register R0x0B = 0x0003; before Chip Enable is set, set register R0x0B = 0x0000.	N	N
	0	0x0000	Synchronize Changes When set, changes to certain registers (those with the SC attribute) are delayed until the bit is clear. When cleared, all the delayed WRITEs will happen immediately. Registers with the F attribute will still have the update synchronized to the next frame boundary. Mirrored on R241[1].	N	N
R8:0 R0x008	15:0	0x0000	Shutter Width Upper (R/W)		
	15	X	Reserved		
	14:8	0x0000	Dark Col Sample Start The start point for sampling 8 pixels of dark columns which follow pixel data. If the value is larger than 72(0x48), it will automatically be set to “0”.	Y	N
	7:4	X	Reserved		
	3:0	0x0000	Shutter Width Upper The most significant bits of the shutter width, which are combined with Shutter Width Lower (R9).	Y	N
	The most significant bits of the shutter width, which are combined with Shutter Width Lower (R9).				
R9:0 R0x009	15:0	0x0320	Shutter Width Lower (R/W)	Y	N
	The least significant bits of the shutter width. This is combined with Shutter_Width_Upper and Shutter_Delay such that the effective shutter width is (((((Shutter_Width_Upper)*65536) + Shutter_Width_Lower)*t_ROW) - Shutter_Delay - C) in PIXCLKs. This should allow a shutter width from about 40?s to about 40s at default row time. If set to zero, a value of “1” will be used. In ERS bulb mode, shutter width has to be greater than or equal to 3.				
R10:0 R0x00A	15:0	0x0000	Pixel Clock Control (R/W)		
	15	0x0000	Invert Pixel Clock When set, LV, FV, and DOUT should be captured on the rising edge of PIXCLK. When clear, they should be captured on the falling edge. This is accomplished by inverting the PIXCLK output.	N	N
	14	X	Reserved		
	13:12	0x0000	Power Down Mode Standby mode B on/off, Standby mode A, which is set by Chip Enable (R7, bit 1) supersedes these bits. 0: normal operation (default mode: sensor continues outputting images) 1: standby mode B (sensor powers down) 2: reserved 3: reserved	N	N
	11	X	Reserved		

Table 6: Core Registers – Register Description (Continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Number Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R10:0 R0x00A	10:8	0x0000	Shift Pixel Clock Two's complement value representing how far to shift the PIXCLK output pin relative to DOUT, in CLK_IN cycles. Positive values shift PIXCLK later in time relative to DOUT (and thus relative to the internal array/datapath clock. No effect unless PIXCLK is divided by Divide Pixel Clock.	N	N
	7	X	Reserved		
	6:0	0x0000	Divide Pixel Clock Produces a PIXCLK that is divided by the value times two. The value must be zero or a power of 2. This will slow down the internal clock in the array control and datapath blocks, including pixel readout. It will not affect the a two-wire serial interface clock. A value of 0 corresponds to a PIXCLK with the same frequency as CLK_IN. A value of 1 means f_PIXCLK = (f_CLK_IN / 2); 2 means f_PIXCLK = (f_CLK_IN / 4); 64 means f_PIXCLK = (f_CLK_IN / 128); and so on.	N	N
R11:0 R0x00B	15:0	0x0000	Restart (R/W)		
	15:3	X	Reserved		
	2	0x0000	Trigger Setting this bit in snapshot mode will cause the next Trigger to occur as if the TRIGGER signal were properly asserted or de-asserted. Ineffective if not in snapshot mode. The sense of this bit is NOT affected by Invert Trigger. When using this bit instead of the TRIGGER signal, make sure that either the TRIGGER signal is continuously asserted, or that the signal is continuously de-asserted and Invert_Trigger is set.	N	N
	1	0x0000	Pause Restart When set, Restart will not automatically be cleared. Instead, the sensor will pause at row 0 after Restart is set. When Pause_Restart is cleared, the sensor will resume. This allows for a repeatable delay from clearing restart to FV.	N	N
	0	0x0000	Restart Setting this bit will cause the sensor to abandon the current frame and restart from the first row. It will take up to 2*t_ROW for the restart to take effect. This bit automatically resets to "0" unless Pause_Restart is set.	N	N
R12:0 R0x00C	15:0	0x0000	Shutter Delay (R/W)	Y	N
	A negative adjustment to the effective shutter width in aclks. See Shutter_Width_Lower.				
R13:0 R0x00D	15:0	0x0000	Reset (R/W)	N	N
	Setting this bit will put the sensor into reset mode, which will set the sensor to its default power-up state and cause it to halt. Clearing this bit will resume normal operation. This is equivalent to pulling the RESET_BAR pin low, except that the two-wire serial interface remains functional.				
R17:0 R0x011	15:0	0x3C04	PLL Config 1 (R/W)		
	15:8	0x003C	PLL m Factor PLL output frequency multiplier.	N	N
	7:6	X	Reserved		
	5:0	0x0004	PLL n Divider PLL output frequency divider minus 1.	N	N

Table 6: Core Registers – Register Description (Continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Number Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R30:0 R0x01E	15:0	0x0146	Read Mode 1 (R/W)		
	15	X	Reserved		
	14	X	Reserved		
	13	0x0000	Output Bad Frames When set, frames that would normally be suppressed as "Bad Frames" will not be suppressed. When cleared, setting registers with the BF attribute will cause one frame to be dropped in the output stream. Ineffective unless Maintain Frame Rate is set.		
	12	0x0000	Maintain Frame Rate When set, writing registers with the BF attribute will create bad frames, but if these WRITEs would not otherwise change the frame rate, the frame rate will be maintained. When cleared, writing registers with the BF attribute will interrupt the frame rate to avoid creating a bad frame.	N	N
	11	0x0000	XOR Line Valid When set, produces a LV signal that is the XOR of FV and the normal LV. Ineffective if Continuous Line Valid is set. When clear, produce a normal LV.	N	N
	10	0x0000	Continuous Line Valid When set, produce the LV signal even during the vertical blank period. When cleared, produces LV only when active rows are being read out (that is, only when FV is HIGH).	N	N
	9	0x0000	Invert Trigger When set, the sense of the TRIGGER input signal will be inverted.	N	N
	8	0x0001	Snapshot When set, the sensor enters snapshot mode, and will wait for a trigger event between frames. When cleared, the sensor is in continuous mode.	Y	N
	7	0x0000	Global Reset When set, the global reset release shutter will be used. When cleared, the electronic rolling shutter will be used.	Y	N
	6	0x0001	Bulb Exposure When set, exposure time will be controlled by an external trigger. When cleared, exposure time will be controlled by the Shutter_Width_Lower and Shutter_Width_Upper registers.	Y	N
	5	0x0000	Invert Strobe When set, the STROBE signal will be normally HIGH, except during exposure, when it will be LOW. When clear, the STROBE signal is normally LOW except during exposure.	N	N
	4	0x0000	Strobe Enable When set, a strobe signal will be generated by the digital logic during integration. When clear, the strobe pin will be set to the value of Invert_Strobe.	N	N

Table 6: Core Registers – Register Description (Continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Number Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
	3:2	0x0001	Strobe Start Determines the timepoint when the strobe is asserted. 0: first trigger 1: simultaneous exposure 2: shutter width 3: second trigger	Y	N
	1:0	0x0002	Strobe End Determines the timepoint when the strobe is de-asserted. If this is set equal to or less than Strobe_Start, the width of the strobe pulse will be t_ROW. See Strobe_Start.	Y	N
R32:0 R0x020	15:0	0x0040	Read Mode 2 (R/W)		
	15	0x0000	Mirror Row When set, row readout in the active image occurs in reverse numerical order starting from (Row_Start + Row_Size). When clear, row readout of the active image occurs in numerical order. This has no effect on the readout of the dark rows.	Y	Y
	14	0x0000	Mirror Column When set, column readout in the active image occurs in reverse numerical order, starting from (Column_Start + Column_Size). When clear, column readout of the active image occurs in numerical order. This has no effect on the readout of the dark columns.	Y	N
	13	X	Reserved		
	12	0x0000	Show Dark Columns When set, the dark columns used for digital black level adjustment will be output to the left of the active image, making the output image wider. This has no effect on integration time or frame rate. When clear, only columns that are part of the active image will be output.	Y	N
	11	0x0000	Show Dark Rows When set, the dark rows used for the analog black level adjustment will be output before the active image rows, making the output image taller. This has no effect on integration time or frame rate. When clear, only rows from the active image will be output.	Y	N
	10:7	X	Reserved		
R32:0 R0x020	6	0x0001	Row BLC When set, digitally compensates for differing black levels between rows by adding Dark Target (R73) and subtracting the average value of the 8 same-color dark pixels at the beginning of the row. When clear, digitally adds Row Black Default Offset (R75) to the value of each pixel.	Y	N
	5:0	X	Reserved		

Table 6: Core Registers – Register Description (Continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Number Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R43:0 R0x02B	15:0	0x0010	Green1 Gain (R/W)		
	15	X	Reserved		
	14:8	0x0000	Green1 Digital Gain Digital Gain for the Green1 channel minus 1 times 8. The actual digital gain is (1 + value/8), and can range from 1 (a setting of 0) to 16 (a setting of 120) in increments of 1/8.	Y	N
	7	X	Reserved		
	6	0x0000	Green1 Analog Multiplier Analog gain multiplier for the Green1 channel minus 1. If 1, an additional analog gain of 2X will be applied. If 0, no additional gain is applied.	Y	N
	5:0	0x0010	Green1 Analogl Gain Analog gain setting for the Green1 channel times 8. The effective gain for the channel is (((Green1_Digital_Gain/8) + 1) * (Green1_Analog_Multiplier + 1) * (Green1_Analog_Gain/16)).	Y	N
R44:0 R0x02C	15:0	0x0010	Blue Gain (R/W)		
	15	X	Reserved		
	14:8	0x0000	Blue Digital Gain Digital Gain for the Blue channel minus 1 times 8. The actual digital gain is (1 + value/8), and can range from 1 (a setting of 0) to 16 (a setting of 120) in increments of 1/8.	Y	N
	7	X	Reserved		
	6	0x0000	Blue Analog Multiplier Analog gain multiplier for the Blue channel minus 1. If 1, an additional analog gain of 2X will be applied. If 0, no additional gain is applied.	Y	N
	5:0	0x0010	Blue Analog Gain Analog gain setting for the Blue channel times 8. The effective gain for the channel is (((Blue_Digital_Gain/8) + 1) * (Blue_Analog_Multiplier + 1) * (Blue_Analog_Gain/16)).	Y	N
R45:0 R0x02D	15:0	0x0010	Red Gain (R/W)		
	15	X	Reserved		
	14:8	0x0000	Red Digital Gain Digital Gain for the Red channel minus 1 times 8. The actual digital gain is (1 + value/8), and can range from 1 (a setting of 0) to 16 (a setting of 120) in increments of 1/8.	Y	N
	7	X	Reserved		
	6	0x0000	Red Analog Multiplier Analog gain multiplier for the Red channel minus 1. If 1, an additional analog gain of 2X will be applied. If 0, no additional gain is applied.	Y	N
	5:0	0x0010	Red Analog Gain Analog gain setting for the Red channel times 8. The effective gain for the channel is (((Red_Digital_Gain/8) + 1) * (Red_Analog_Multiplier + 1) * (Red_Analog_Gain/16)).	Y	N

Table 6: Core Registers – Register Description (Continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Number Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R46:0 R0x02E	15:0	0x0010	Green2 Gain (R/W)		
	15	X	Reserved		
	14:8	0x0000	Green2 Digital Gain Digital Gain for the Green2 channel minus 1 times 8. The actual digital gain is (1 + value/8), and can range from 1 (a setting of 0) to 16 (a setting of 120) in increments of 1/8.	Y	N
	7	X	Reserved		
	6	0x0000	Green2 Analog Multiplier Analog gain multiplier for the Green2 channel minus 1. If 1, an additional analog gain of 2X will be applied. If 0, no additional gain is applied.	Y	N
	5:0	0x0010	Green2 Analog Gain Analog gain setting for the Green2 channel times 8. The effective gain for the channel is (((Green2_Digital_Gain/8) + 1) * (Green2_Analog_Multiplier + 1) * (Green2_Analog_Gain/16)).	Y	N
R53:0 R0x035	15:0	0x0010	Global Gain (WO)	Y	N
	Writing the Global_Gain sets all four individual gain registers R43–R46 to the value. This register should not be read. See Green1_Gain (R43) for a description of the various fields.				
R73:0 R0x049	15:0	0x00A8	Row Black Target (R/W)	Y	N
	The target black level for the Row BLC algorithm.				
R75:0 R0x04B	15:0	0x0028	Row Black Default Offset (R/W)	Y	N
	A two's complement offset digitally added to all active image pixel values when Row BLC (R30[6]) is disabled.				
R91:0 R0x05B	15:0	0x0001	BLC_Sample_Size (R/W)	N	N
	If set, the "moving average" calculation in the BLC algorithm will use a sample size of 32. If cleared, it will use a sample size of 1 (that is, each frame's black level will be considered independent of other frames).				
R92:0 R0x05C	15:0	0x005A	BLC_Tune_1 (R/W)		
	15:12	X	Reserved		
	11:8	0x0000	BLC_Delta_Damping A number subtracted from the calculated correction's magnitude when in delta mode. Setting this to a positive number will correct by that much less than the delta value. A negative (two's complement) number will correct by more (possibly worsening the overshoot). This applies to the magnitude of the delta, so a positive damping value will be subtracted from a positive delta and added to a negative delta.	Y	N
	7:0	0x005A	BLC_DAC_Settling_Time The number of PIXCLKs it takes for a newly set offset to take effect divided by 2. Used to configure the fast sample algorithm. After setting a calibration value in fast sample mode, (value * 2) PIXCLKs will elapse before the next sample is taken.	Y	N

Table 6: Core Registers – Register Description (Continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Number Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R93:0 R0x05D	15:0	0x2D13	BLC_Delta_Thresholds (R/W)		
	15	X	Reserved		
	14:8	0x002D	BLC_High_Delta_Threshold Upper delta threshold divided by 4. If the average black value for a color is higher than this value times 4 or lower than BLC_Low_Delta_Threshold times 4, the fast sampling and binary search modes will be activated (if enabled). Once the black level is between the BLC_High_Delta_Threshold and the BLC_Low_Delta_Threshold, the delta adjustment mode will be used (though fast sample mode will continue until the end of the frame). This value should be set no lower than BLC High Target Threshold.	Y	N
	7	X	Reserved		
	6:0	0x0013	BLC_Low_Delta_Threshold Lower delta threshold divided by 4. See BLC_High_Delta_Threshold. Should be no higher than BLC_Low_Target_Threshold.	Y	N
R94:0 R0x05E	15:0	0x41FF	BLC_Tune_2 (R/W)		
	15	X	Reserved		
	14:12	0x0004	BLC_Step_Size Base 2 log of the change in pixel value (in LSBs) of a pixel when the analog offset is changed by one.	N	N
	11:9	X	Reserved		
	8:0	0x01FF	BLC_Max_Adjust The maximum adjustment (positive or negative) that the BLC delta adjustment mode is allowed to make to the analog offset.	N	N
R95:0 R0x05F	15:0	0x231D	BLC_Target_Thresholds (R/W)		
	15	X	Reserved		
	14:8	0x0023	BLC_High_Target_Threshold The upper target threshold of the BLC algorithm divided by 4. The target black value is 4 times the average of the BLC_High_Target_Threshold and the BLC_Low_Target_Threshold. When the black value for a color is within these thresholds, it will be considered to be on target.	Y	N
	7	X	Reserved		
	6:0	0x001D	BLC_Low_Target_Threshold The lower target threshold for the BLC algorithm divided by 4. See BLC High Target Threshold above.	Y	N
R96:0 R0x060	15:0	0x0020	Green1_Offset (R/W)	Y	N
	Two's complement representation of the analog offset value for Green1. If Manual_BLC (R98[0]) is set, this value will be used as the analog offset. Otherwise, the value may be overridden by the BLC algorithm. When read, this register returns the offset currently in use. The user-programmed value is always retained internally, and may be read by setting Manual_BLC. A value of –256 will set the offset to –255.				
R97:0 R0x061	15:0	0x0020	Green2_Offset (R/W)	Y	N
	Two's complement representation of the analog offset value for Green2. See Green1_Offset.				

Table 6: Core Registers – Register Description (Continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Number Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R98:0 R0x062	15:0	0x0000	Black_Level_Calibration (R/W)		
	15	0x0000	Disable_Fast_Sample When set, the fast sampling mode (multiple samples per frame) will not be used if the black level falls outside the delta thresholds; instead, only one sample-adjust will take place per frame. Binary search mode may still be used. When cleared, fast sample mode will be used when necessary.	Y	N
	14	0x0000	Lock_Green_Calibration When set, the calibration offset chosen for Green1 will be used for Green2 pixels as well. Only effective if Green1_Analog_Gain equals Green2_Analog_Gain and Green1_Analog_Multiplier equals Green2_Analog_Multiplier.	Y	N
	13	0x0000	Lock_Red_Blue_Calibration When set, the calibration offset chosen for Red will be used for Blue pixels as well. Only effective if Red_Analog_Gain equals Blue_Analog_Gain and Red_Analog_Multiplier equals Blue_Analog_Multiplier.	Y	N
	12	0x0000	Recalculate_Black_Level When set, any running averages will be reset and the fast sample and binary search modes will be activated (if enabled). This bit always reads 0.	Y	N
	11	0x0000	Disable_Binary_Search When set, binary search mode will not be used when the black level falls outside the delta thresholds; instead the delta mode will be used. Fast sampling mode may still be used if enabled.	Y	N
	10:2	X	Reserved		
R98:0 R0x062	1	0x0000	Disable_Calibration When set, analog calibration is disabled. When cleared, the programmed or automatic offsets will be used.	N	N
	0	0x0000	Manual_BLC When set, the user-programmed calibration offsets from R96-R97 and R99–R100 will be used. Also, black level calculation will be disabled. When cleared, the BLC algorithm will adjust the offsets to maintain the target black level.	Y	N
R99:0 R0x063	15:0	0x0020	Red_Offset (R/W)	Y	N
	Two's complement representation of the analog offset value for Red. See Green1_Offset.				
R100:0 R0x064	15:0	0x0020	Blue_Offset (R/W)	Y	N
	Two's complement representation of the analog offset value for Blue. See Green1_Offset.				
R148:0 R0x094	15:0	0x290E	Reserved		
	15:14	X	Reserved		
	13:8	0x0029	Reserved		
	7:1	0x0007	Reserved		
	0	0x0000	Reserved		
R157:0 R0x09D	15:0	0x2255	Formatter0 (R/W)		
	15:12	0x0002	FV delay adjustment frame valid delay control (two's complement [-8, 7]).	Y	N
	11:8	0x0002	LV delay adjustment line valid delay control (two's complement [-8, 7]).	Y	N

Table 6: Core Registers – Register Description (Continued)
R/W (Read or Write) bit; RO (Read Only) bit

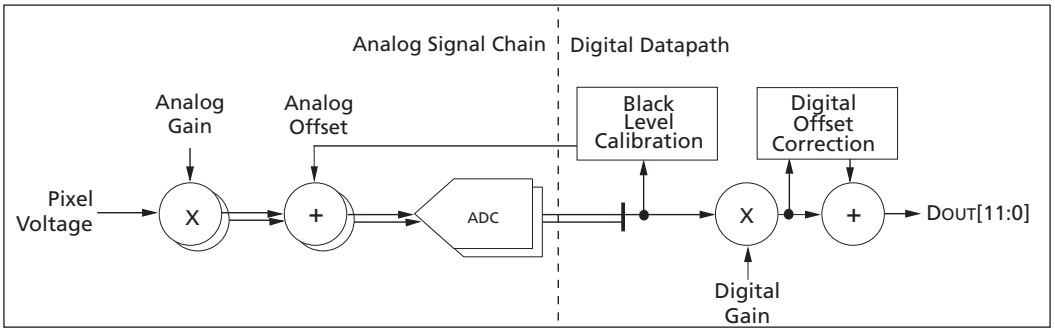
Register Number Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R159:0 R0x09F	15:0	0x0071	Formatter2 (R/W)		
	13	0x0000	PIXCLK output enable PIXCLK output enable 0 : PIXCLK is always set 0 {default} 1 : enable	N	N
	12	0x0000	DOUT output enable parallel data output enable 0 : DOUT bus is always set 0x000 {default} 1 : enable	N	N
R255:0 R0x0FF	15:0	0x1402	Chip_Version_Alt (RO)	N	N
	Mirror of R0[15:0].				

Signal Chain and Datapath

The signal chain and datapath are shown in Figure 14. Each color is processed independently, including separate gain and offset settings. Voltages sampled from the pixel array are first passed through an analog gain stage, which can produce gain factors between 1 and 7.875. An analog offset is then applied, and the signal is sent through a 12-bit analog-to-digital converter. In the digital space, a digital gain factor of between 1 and 16 is applied, and then a digital offset of between –2048 and 2047 is added. The resulting 12-bit pixel value is then output on the DOUT[11:0] ports.

The analog offset applied is determined automatically by the black level calibration algorithm, which attempts to shift the output of the analog signal chain so that black is maintained. The digital offset is a fine-tuning of the analog offset.

Figure 14: Signal Path



Gains

The MT9M032 supports two types of gain: analog gain and digital gain. Combined, gains of between 1 and 126 are possible. It is recommended that analog gain should be maximized before applying digital gain.

The sensor provides per-color gain control as well as the option of global gain control. Per-color and global gain control can be used interchangeably. A WRITE to a global gain register is aliased as a WRITE of the same data to the four associated color-dependent gain registers.

The combined gain for a color C is given by:

$$G_C = AG_C \times DG_C \quad \text{(EQ 1)}$$

Analog Gain

The analog gain is specified independently for each color channel. There are two components, the gain and the multiplier. The gain is specified by Green1_Analog_Gain, Red_Analog_Gain, Blue_Analog_Gain, and Green2_Analog_Gain. The analog multiplier is specified by Green1_Analog_Multiplier, Red_Analog_Multiplier, Blue_Analog_Multiplier, and Green2_Analog_Multiplier. These combine to form the analog gain for a given color C, as shown in this equation:

$$AG_C = (1 + C\_Analog\_Multiplier) \times (C\_Analog\_Gain / 16) \quad \text{(EQ 2)}$$

The gain component can range from 0 to 7.875 in steps 0.0625 for <4 gain, and 0.125 for >4 gain, and the multiplier component can be either 0 or 1 (resulting in a multiplier of 1 or 2). However, it is best to keep the gain component between 1 and 4 for the best noise performance, and use the multiplier for gains between 4 and 7.825. Green1 and GreenR are equivalent; Green2 and GreenB are equivalent.

Digital Gain

The digital gain is specified independently for each color channel in steps of 0.125. It is controlled by the register fields Green1_Digital_Gain, Red_Digital_Gain, Blue_Digital_Gain, and Green2_Digital_Gain. The digital gain for a color C is given by:

$$DG_C = 1 + (C\_Digital\_Gain / 8) \quad \text{(EQ 3)}$$

Offset

The MT9M032 sensor can apply an offset or shift to the image data in several ways.

An analog offset can be applied on a color-wise basis to the pixel voltage as it enters the ADC. This makes it possible to adjust for offset introduced in the pixel sampling and gain stages to be removed, centering the resulting voltage swing in the ADC's range. This offset can be automatically determined by the sensor using the automatic black level calibration (BLC) circuit, or it can be set manually by the user. It is a fairly coarse adjustment, with adjustment step sizes of four to eight LSBs.

Digital offset is also added on a color-wise and line-wise basis to fine-tune the black level of the output image. This offset is based on an average black level taken from each row's dark columns, and is automatically determined by the digital row-wise black level calibration (RBLC) circuit. If the RBLC circuit is not used, a user-defined offset can be applied instead. This offset has a resolution of 1 LSB.

A digital offset is added on a color-wise basis to account for channel offsets that can be introduced due to “even” and “odd” pixels of the same color going through a slightly different ADC chain. This offset is automatically determined based on dark row data, but it can also be manually set.

Analog Black Level Calibration

The MT9M032 black level calibration circuitry provides a feedback control system since adjustments to the analog offset are imprecise by nature. The goal is that within the dark row region of any supported output image size, the offset should have been adjusted such that the average black level falls within the specified target thresholds.

The analog offsets normally need a major adjustment only when leaving the Reset state or when there has been a change to a color's analog gain. Factors like shutter width and temperature have lower-order impact, and generally only require a minor adjustment to the analog offsets. The MT9M032 has various calibration modes to keep the system stable while still supporting the need for rapid offset adjustments when necessary.

Digital Black Level Calibration

Digital black level calibration is the final calculation applied to pixel data before it is output. It provides a precise black level to complement the coarser-grained analog black level calibration, and also corrects for black level shift introduced by digital gain. This correction applies to the active columns for all rows, including dark rows.

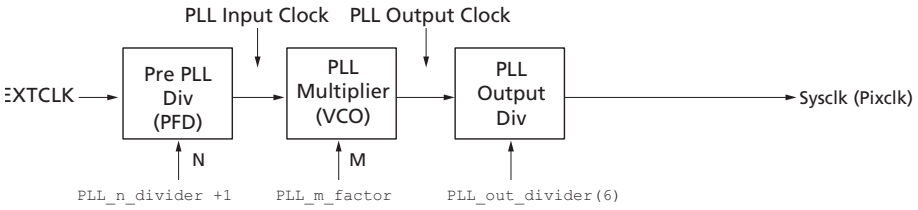
Features

PLL-Generated Master Clock

The PLL can generate a PIXCLK clock signal whose frequency is up to 99 MHz (input clock from 8–16.5 MHz). The PLL-generated clock can be controlled by programming the appropriate register. It is possible to bypass the PLL and use EXTCLK as master clock. By default, the PLL is powered up.

The PLL contains a prescaler to divide the input clock applied on EXTCLK, a VCO to multiply the prescaler output, and PLL output divider stage to generate the output clock. The clocking structure is shown in Figure 15. PLL control can be programmed to generate desired pixel clock frequency.

Figure 15: PLL-Generated Master Clock



Note: The PLL control registers must be programmed while the sensor is in the software standby state. The effect of programming the PLL divisors while the sensor is in the streaming state is undefined.

PLL Setup

To use the PLL:

1. Bring the MT9M032 up as normal, ensure that ^{f}EXTCLK is between 8 and 16.5 MHz.
2. Set PLL out divider to 7. (Power-up default PLL out divider setting is 6.)
3. Set PLL_m_factor and PLL_n_divider based on the desired input (^{f}EXTCLK) and output (^{f}PIXCLK) frequencies.
   Using this formula:
   ^{f}PIXCLK = ^{f}VCO/7
   where
   ^{f}VCO = (^{f}EXTCLK x M) / N
   M = PLL_m_factor,
   N = (PLL_n_divider + 1)
   Example of PLL setting:
   ^{f}EXTCLK = 13.5 MHz
   PLL_m_factor = 0x9A (154), PLL_n_divider = 0x02
   ^{f}PIXCLK = 99 MHz
4. Wait 1ms to ensure that the VCO has locked.
5. Set R0x10 = 0x0053
6. Delay = 1ms
7. Enable parallel data output
8. Delay = 1ms

Table 7: Frequency Parameters

Parameter	Equation	Min	Max	Unit
PLL_n_divider	–	0	63	
PLL_m_factor	–	16	255	
^{f}EXTCLK	–	8	16.5	MHz
^{f}PFD	^{f}EXTCLK /(PLL_n_divider+1)	2	24	MHz
^{f}VCO	^{f}EXTCLK * PLL_m_factor/(PLL_n_divider+1)	320	693	MHz

PLL Setup Sample Code for Parallel Mode After Power-Up (with input clock frequency 13.5 MHz)

1. Set R0x1E = 0x8006 // Master Mode
2. Set R0x9F = 0x0070 // Set-up for changing to 14-bit mode.
3. Set R0x9E = 0x101E // Set 14-bit mode, select 7 divider, parallel mode.
4. Set R0x11 = 0x9A02 // Assuming an input EXTCLK of 13.5 MHz, generates an output PIXCLK of 99 MHz.
5. Delay = 1ms // Ensures VCO has locked.
6. Set R0x10 = 0x0053 // Select PLL as clock source.
7. Set R0x9F = 0x3070 // Parallel data out.

Note: The registers R0x9E and R0x9F need to be set to different values for serial operation. The code example shows the values for parallel operation. For the serial operation: R0x9F = 0xC070, R0x9E = 0x001E.

Maintaining a Constant Frame Rate

Maintaining a constant frame rate while continuing to have the ability to adjust certain parameters is often desired. This is not always possible, however, since register updates are synchronized to the read pointer, and the shutter pointer for a frame is usually active during the readout of the previous frame. Therefore, any register changes that could affect the row time or the set of rows sampled causes the shutter pointer to start over at the beginning of the next frame.

By default, the following register fields cause a “bubble” in the output rate (the vertical blank increases for one frame) if they are written in continuous mode, even if the new value would not change the resulting frame rate:

- Row_Start
- Row_Size
- Column_Size
- Horizontal_Blank
- Vertical_Blank
- Shutter_Delay
- Mirror_Row

The size of this bubble is (SW × ^{t}ROW), calculating the row time according to the new settings.

The Shutter_Width_Lower and Shutter_Width_Upper fields may be written without causing a bubble in the output rate under certain circumstances. Since the shutter sequence for the next frame often is active during the output of the current frame, this would not be possible without special provisions in the hardware. Writes to these regis-

ters take effect two frames after the frame they are written, which allows the shutter width to increase without interrupting the output or producing a corrupt frame (as long as the change in shutter width does not affect the frame time).

Synchronizing Register WRITEs to Frame Boundaries

Changes to most register fields that affect the size or brightness of an image take effect on the frame after the one during which they are written. These fields are noted as "synchronized to frame boundaries" in Table 5 on page 20. To ensure that a register update takes effect on the next frame, the WRITE operation must be completed after the leading edge of FV and before the trailing edge of FV.

As a special case, in snapshot modes (see below), register WRITEs that occur after FV but before the next trigger will take effect immediately on the next frame, as if there had been a restart. However, if the trigger for the next frame in ERS snapshot mode occurs during FV, register WRITE take effect as with continuous mode.

Additional control over the timing of register updates can be achieved by using Synchronize_Changes. If this bit is set, WRITEs to certain register fields that affect the brightness of the output image do not take effect immediately. Instead, the new value is remembered internally. When synchronize_changes is cleared, all the updates simultaneously take effect on the next frame (as if they had all been written the instant synchronize_changes was cleared). Register fields affected by this bit are identified in Table 6: "Core Registers – Register Description," on page 25.

Fields not identified as being frame-synchronized or affected by Synchronize_Changes are updated immediately after the register write is completed. The effect of these registers on the next frame can be difficult to predict if they affect the shutter pointer.

Restart

To restart the MT9M032 at any time during the operation of the sensor, write a "1" to the restart register (R0x0B[0] = 1). This has two effects: first, the current frame is interrupted immediately. Second, any writes to frame-synchronized registers and the shutter width registers take effect immediately, and a new frame starts (in continuous mode). Register updates being held by Synchronize_Changes do not take effect until that bit is cleared. The current row and one following row complete before the new frame is started, so the time between issuing the restart and the beginning of the next frame can vary by about ^{t}ROW.

If Pause_Restart is set, rather than immediately beginning the next frame after a Restart in continuous mode, the sensor pauses at the beginning of the next frame until Pause_Restart is cleared. This can be used to achieve a deterministic time period from clearing the Pause_Restart bit to the beginning of the first frame, meaning that the controller does not need to be tightly synchronized to LV or FV.

Note: When Pause_Restart is cleared, be sure to leave the Restart register set to "1" for proper operation. The restart bit will be cleared automatically by the device.

Window Size

The output image window of the pixel array (the FOV) is programmable and defined by four register fields. Column_Start and Row_Start define the X and Y coordinates of the upper left corner of the FOV. Column_Size defines the width of the FOV, and Row_Size defines the height of the FOV in array pixels.

The Column_Start and Row_Start fields must be set to an even number. The Column_Size and Row_Size fields must be set to odd numbers (resulting in an even size for the FOV). The Row_Start register should be set no lower than 12 if either Manual_BLC is cleared or Show_Dark_Rows is set. The width of the output image, W, is *Column_Size + 1* and height, H, is *Row_Size + 1*. In default, a full resolution image size of 1440 x 1080 in output.

Readout Modes

The MT9M032 sensor supports mirror readout mode. Image can be flipped in the vertical and/or mirrored in the horizontal directions.

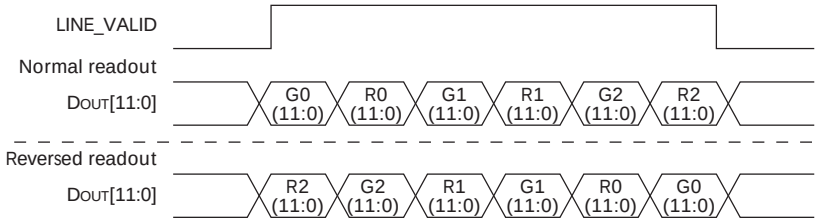
Mirror Mode

By default, active pixels in an image are output in row-major order (an entire row is output before the next row is begun), from lowest row/column number to highest. Mirror mode allows the output order of the rows and columns to be reversed. This only affects pixels in the active region of the image, not pixels read out as dark rows or dark columns. When the readout direction is reversed, the color order is reversed as well (for example, red, green, red, and so on instead of green, red, green, and so on), thus causing the Bayer order of the output image to change.

Column Mirror (Color)

The readout order of the columns are reversed, as shown in Figure 16.

Figure 16: Six Pixels in Normal and Column Mirror Readout Modes (Color)



Row Mirror

The readout order of the rows are reversed, as shown in Figure 17.

Figure 17: Six Pixels in Normal and Column Mirror Readout Modes (Mono)

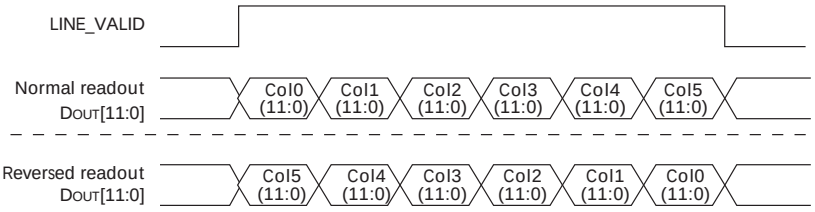


Figure 18: Six Rows in Normal and Row Mirror Readout Modes

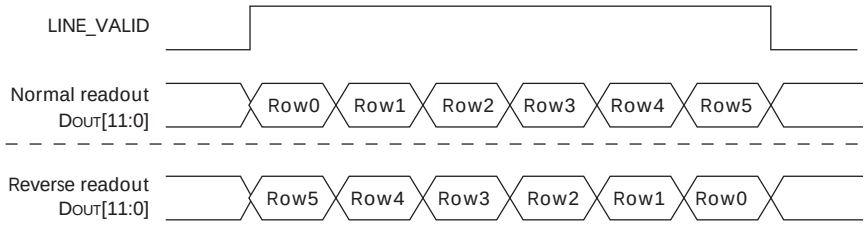


Image Acquisition Modes

The MT9M032 supports two image acquisition modes (shutter types), electronic rolling shutter (ERS), and global reset release (GRR).

Electronic Rolling Shutter

The ERS modes take pictures by scanning the rows of the sensor. On the first scan, each row is released from reset, starting the exposure. On the second scan, the row is sampled, processed, and returned to the reset state. The exposure for any row is therefore the time between the first and second scans. Each row is exposed for the same duration, but at slightly different point in time, which can cause a shear in moving subjects.

Whenever the mode is changed to an ERS mode (even from another ERS mode), and before the first frame following reset, there is an anti-blooming sequence where all rows are placed in reset. This sequence must complete before continuous readout begins.

This delay is:

$^{t}ALLRESET = 16 \times 1096 \times {}^{t}ACLK$ (where $^{t}ACLK$ is $2 * {}^{t}PIXCLK$).

Global Reset Release

The GRR modes attempt to address the shearing effect by starting exposures of all rows at the same time. Instead of the first scan used in ERS mode, the reset to each row is released simultaneously. The second scan occurs as normal, so the exposure time for each row would different. Typically, an external mechanical shutter would be used to stop the exposure of all rows simultaneously.

In GRR modes, there is a startup overhead before each frame as all rows are initially placed in the reset state (^{t}ALLRESET). Unlike ERS mode, this delay always occurs before each frame. However, it occurs as soon as possible after the preceding frame, so typically the time from trigger to the start of exposure does not include this delay. To ensure that this is the case, the first trigger must occur no sooner than ^{t}ALLRESET after the previous frame is read out.

Exposure

The nominal exposure time, ^{t}EXP, is the effective shutter time in ERS modes, and is defined by the shutter width (SW), and the shutter overhead (SO), which includes the effect of Shutter_Delay. Exposure time for other modes is defined relative to this time. Increasing Shutter_Delay (SD) decreases the exposure time. Exposure times are typically specified in units of row time, although it is possible to fine-tune exposures in units of ^{t}ACLKs (where ^{t}ACLK is 2* ^{t}PIXCLK).

This is expressed in the formula:

$^{t}EXP = SW \times {}^{t}ROW - SO \times 2 \times {}^{t}PIXCLK$

The exposure time is calculated by determining the reset time of each pixel row (with time 0 being the start of the first row time), and subtracting it from the sample time. Under normal conditions in ERS modes, every pixel should end up with the same exposure time. In global shutter release modes, the exposure times of individual pixels can vary.

In global shutter release modes (described later), exposure time starts simultaneously for all rows, but still ends as defined above. In a real system, the exposure would be stopped by a mechanical shutter, which would effectively stop the exposure to all rows simultaneously. Since this specification does not consider the effect of an external shutter, each output row's exposure time will differ by ^{t}ROW from the previous row.

Global shutter modes also introduce a constant added to the shutter time for each row, since the exposure starts during the global shutter sequence, and not during any row's shutter sequence.

In Bulb_Exposure modes (also detailed later), the exposure time is determined by the width of the TRIGGER pulse rather than the shutter width registers. In ERS bulb mode, it will still be a multiple of row times, and the shutter overhead equation still applies. In GRR bulb mode, the exposure time is granular to ACLKs, and shutter overhead (and thus Shutter_Delay) have no effect.

Operating Modes

In the default operating mode, the MT9M032 continuously samples and outputs frames. It can be put in snapshot or triggered mode by setting snapshot, which means that it samples and outputs a frame only when triggered. To leave snapshot mode, it is necessary to first clear snapshot then issue a restart.

When in snapshot mode, the sensor can use the ERS or the GRR. The exposure can be controlled as normal, with the Shutter_Width_Lower and Shutter_Width_Upper registers, or it can be controlled using the external TRIGGER signal. The various operating modes are summarized in Table 8.

Table 8: Operating Modes

Mode	Settings	Description
ERS Continuous	Default	Frames are output continuously at the frame rate defined by $^{t}FRAME$. ERS is used, and the exposure time is electronically controlled to be ^{t}EXP.
ERS Snapshot	Snapshot = 1	Frames are output one at a time, with each frame initiated by a trigger. ERS is used, and the exposure time is electronically controlled to be ^{t}EXP.
ERS Bulb	Snapshot = 1; Bulb_Exposure = 1	Frames are output one at a time, with each frame's exposure initiated by a trigger. ERS is used. End of exposure and readout are initiated by a second trigger.
GRR Snapshot	Snapshot = 1; Global_Reset = 1	Frames are output one at a time, with each frame initiated by a trigger. GRR is used. Readout is electronically triggered based on SW.
GRR Bulb	Snapshot = 1; Bulb_Exposure = 1; Global_Reset = 1	Frames are output one at a time, with each frame initiated by a trigger. GRR is used. Readout is initiated by a second trigger.

Notes: 1. In ERS bulb mode, SW must be greater than 4 (use trigger wider than $^{t}ROW*4$).

All operating modes share a common set of operations:

1. Wait for the first trigger, then start the exposure.
2. Wait for the second trigger, then start the readout.

The first trigger is by default automatic, producing continuous images. If snapshot is set, the first trigger can either be a low level on the TRIGGER pin or writing a "1" to the trigger register field. If Invert_Trigger is set, the first trigger is a high level on TRIGGER pin (or a "1" written to Trigger register field). Since TRIGGER is level-sensitive, multiple frames can be output (with a frame rate of ^{t}FRAME) by holding TRIGGER pin at the triggering level.

The second trigger is also normally automatic, and generally occurs SW row times after the exposure is started. If Bulb_Exposure is set, the second trigger can either be a high level on TRIGGER or a write to Restart. If Invert_Trigger is set, the second trigger is a low level on TRIGGER (or a Restart). In bulb modes, the minimum possible exposure time depends on the mechanical shutter used.

After one frame has been output, the chip will reset back to step 1 above, eventually waiting for the first trigger again. The next trigger may be issued after ((VB - 8) x ^{t}ROW) in ERS modes or ^{t}ALLREST in GRR modes.

The choice of shutter type is made by Global_Reset. If it is set, the GRR shutter is used; otherwise, ERS is used. The two shutters are described in "Electronic Rolling Shutter" on page 41 and "Global Reset Release" on page 41.

The default ERS continuous mode is shown in Figure 4 on page 11. Figure 19 shows default signal timing for ERS snapshot modes, while Figure 20 on page 44 shows default signal timing for GRR snapshot modes.

Figure 19: ERS Snapshot Timing

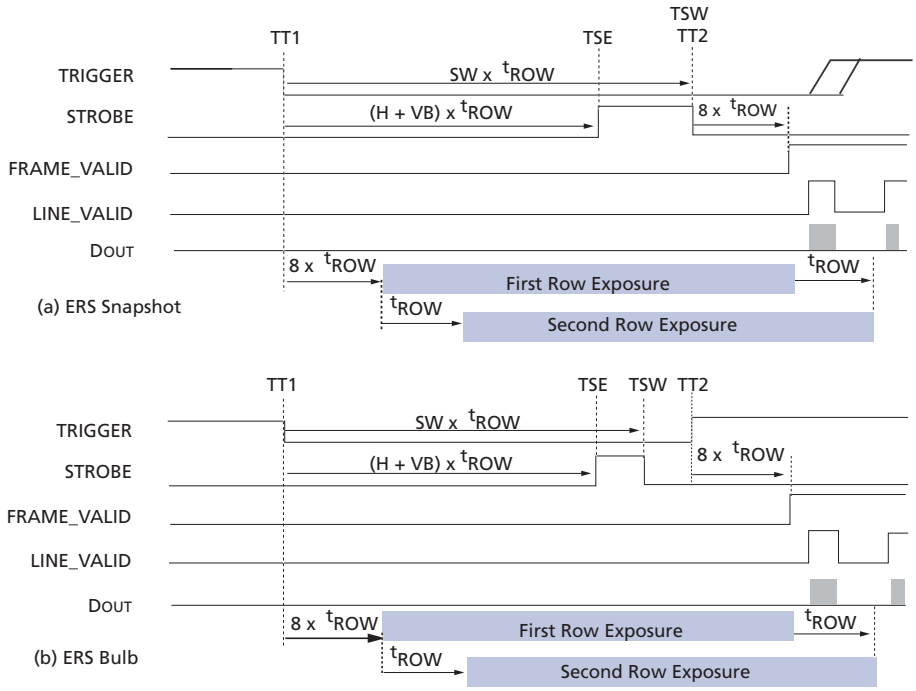
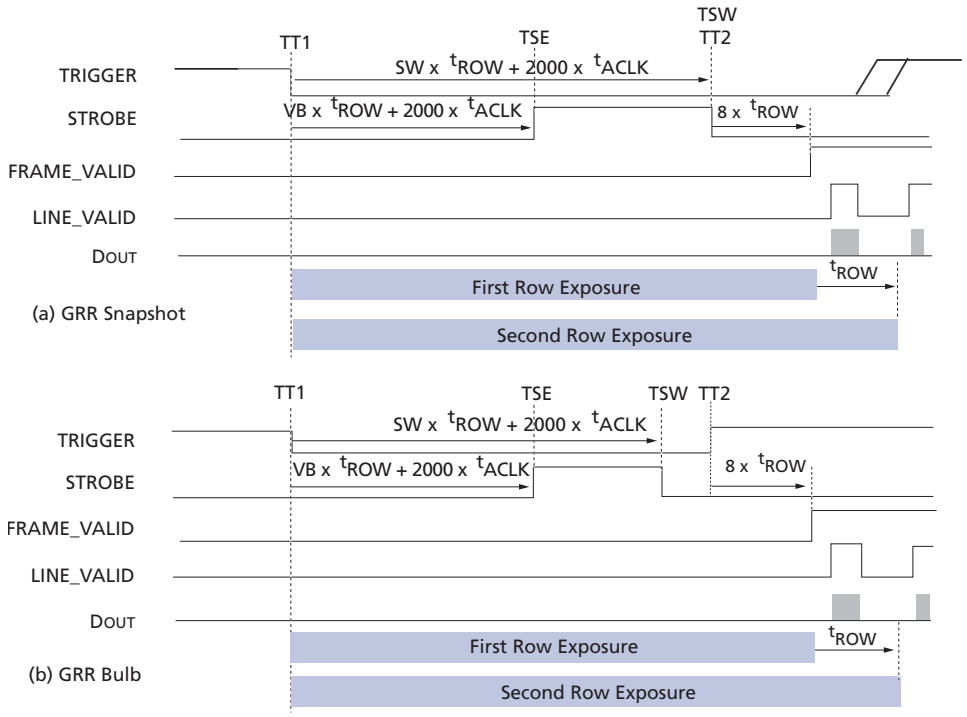


Figure 20: GRR Snapshot Timing



Strobe Control

To support synchronization of the exposure with external events such as a flash or mechanical shutter, the MT9M032 produces a STROBE output. By default, this signal is asserted for approximately the time that all rows are simultaneously exposing, minus the vertical blank time, as shown in Figure 19 on page 43 and Figure 20. Also indicated in these figures are the leading and trailing edges of STROBE, which an be configured to occur at one of several timepoints. The leading edge of STROBE occurs at STROBE_Start, and the trailing edge at STROBE_End, which are set to codes described in Table 9.

Table 9: STROBE Timepoints

Symbol	Timepoint	Code
TT1	Trigger 1 (start of shutter scan)	–
TSE	Start of exposure (all rows simultaneously exposing) offset by VB	1
TSW	End of shutter width (expiration of the internal shutter width counter)	2
TT2	Trigger 2 (start of readout scan)	3

If STROBE_Start and STROBE_End are set to the same timepoint, the strobe is a ^{t}ROW wide pulse starting at the STROBE_Start timepoint. If the settings are such that the strobe would occur after the trailing edge of FV, the strobe may be only ^{t}ACLK wide; however, since there is no concept of a row at that time. The sense of the STROBE signal can be inverted by setting Invert_Strobe (R0x1E[5] = 1). To use strobe as a flash in snapshot modes or with mechanical shutter, set the Strobe_Enable register bit field (R0x1E[4] = 1).

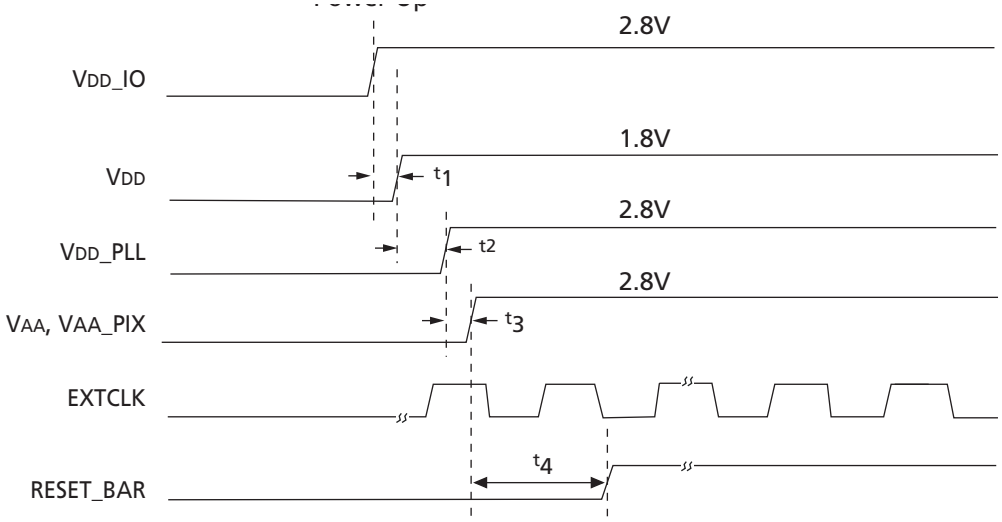
Timing Specifications

Power-Up Sequence

Use the following sequence when powering up the MT9M032:

1. Ensure RESET_BAR is asserted (driven LOW).
2. Bring up all the power supplies at the same time. If both the analog and the digital supplies cannot be brought up simultaneously, ensure the digital supply comes up first. Ensure that all power rails reach minimum voltages.
3. De-assert RESET_BAR (driven HIGH) to make the sensor active.
4. After reset, the sensor must be activated to generate output image data. To active it, the user must load a set of initial file settings. The simplest set of power on initialization settings is:
   REG = 0, 0x1E, 0xC006 // Set parallel mode
   REG = 0, 0x9F, 0x3070 // Parallel data and clock out
   REG = 0, 0x9E, 0x111E // FV_LV timing adjustment
   REG = 0, 0x0B, 0x0001 // restart
   DELAY = 100
   REG = 0, 0x0B, 0x0000 //restart

Figure 1: Power Supply Power-Up Sequence



Notes:
1. The LV signal must be connected to an external pull-down resistor (typically from 10k–100kΩ).
2. The dotted lines are drawn in reference to the minimum voltage of the power supply or minimum VIH for RESET_BAR. Please refer Table 18 on page 10 for DC electrical specifications.
3. After all power rails reach their minimum voltage value, RESET_BAR should stay at LOW at least one millisecond. At least one stable EXTCLK input is required before RESET_BAR is released.

Table 1: Power Supply Power-Up Timing

Parameter	Symbol	Min	Typ	Max	Units
VDD_IO to VDD	t_1	0	–	500	ms
VDD to VDD_PLL	t_2	0	–	500	
VDD_PLL to VAA, VAA_PIX	t_3	0	–	500	
Reset activation	t_4	1	–	–	

Power-Down Sequence

Follow this sequence to power down the sensor. See Figure 22 for detailed timing.

1. Assert RESET_BAR (driven LOW).
2. Remove all power supplies simultaneously or at least within the timing parameters specified in Table 13.

Figure 2: Power Supply Power-Down Sequence

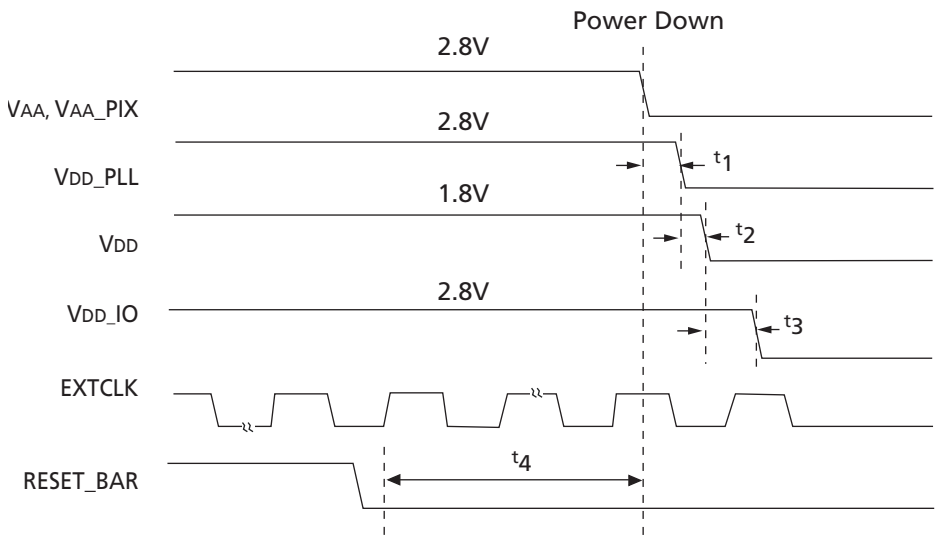


Table 2: Power Supply Power-Down Timing

Parameter	Symbol	Min	Typ	Max	Unit
VAA, VAA_PIX to VDD_PLL	t_1	0	–	500	ms
VDD_PLL to VDD	t_2	0	–	500	
VDD to VDD_IO	t_3	0	–	500	
Reset activation	t_4	1	–	–	

Reset

Two types of reset are available:

1. A hard reset is issued by toggling RESET_BAR.
2. A soft reset is issued by writing commands through the serial interface.

Hard Reset

Assert (LOW) RESET_BAR and apply at least one EXTCLK pulse. All registers return to the factory defaults. When the signal is de-asserted (HIGH), the chip resumes normal operation.

Soft Reset

A soft reset to the sensor has the same affect as the hard reset and can be activated by setting the register field to "1": R0x0D[0] = 1.

All registers except the following will be reset:

- Chip_Enable
- Synchronize_Changes
- Reset
- PLL_m_Factor
- PLL_n_Divider

When the field is returned to "0," the chip resumes normal operation.

Signal State During Reset

Table 14 shows the state of the signal interface during reset (when RESET_BAR is asserted) and during standby (after exit from Reset and before any registers within the sensor have been changed from their default power-up values).

Table 3: Signal State During Reset

Signal Name	Signal Type	Reset Signal State
SCLK	Input	Input
RESET_BAR	Input	Input
EXTCLK	Input	Input
TRIGGER	Input	Input
TEST	Input	Input
SDATA	I/O	Input
STROBE	Output	Tri-state
DOUT[11:0]	Output	Output
PIXCLK	Output	High
FRAME_VALID	Input	Input
LINE_VALID	Input	Input

Standby and Chip Enable (Power Save Mode)

The MT9M032 can be put in a low-power standby state from streaming state by programming R0x07[1]. Two standby modes (STBY_A and STBY_B) are selectable through R0x10[13:12]. Conditions are shown in Table 15. When the sensor is put in standby, all internal clocks are gated, and analog circuitry is put in a state that it draws minimal power.

The two-wire serial interface remains minimally active so that the Chip_Enable bit can subsequently be cleared. READs cannot be performed and only the Chip_Enable register is writable.

If the sensor was in continuous mode when put in standby, it resumes from where it was when standby was deactivated. For maximum power savings in standby mode, EXTCLK should not be toggling. When standby mode is entered, the PLL is disabled automatically or powered down. It must be manually re-enabled when leaving standby as needed.

Note: STBY_B is for master mode in the system, which keeps to output sync (FV/LV) signals. STBY_A is for both modes.

To enter standby STBY_A:
Set R0x027[7] = 1
Set R0x094[0] = 1
Set R0x00B = 0x0003
Set R0x007[1] = 0

To enter standby STBY_B:
Set R0x00A[12:13] = 1

To leave standby STBY_A:
Set R0x027[7] = 0
Set R0x094[0] = 0
Set R0x00B = 0x0000
Set R0x007[1] = 1
Set R0x010[1] = 0
Set R0x010[1] = 1

To leave standby STBY_B:
Set R0x00A[12:13] = 0

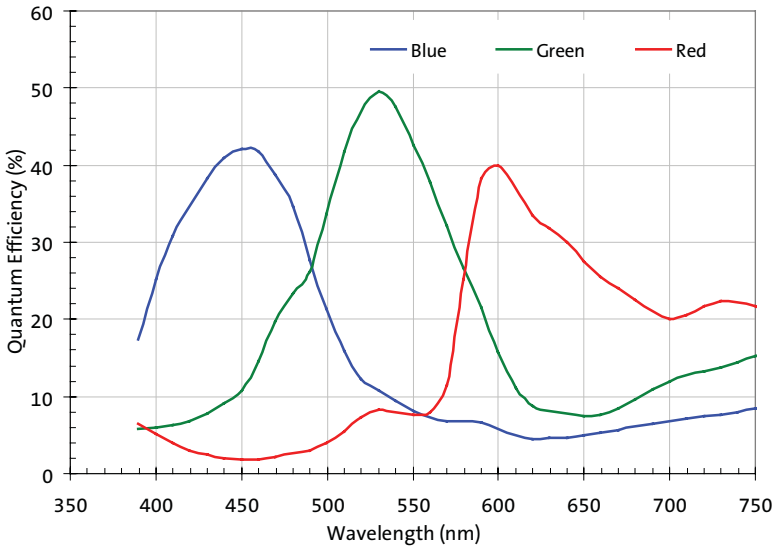
Table 4: Standby Modes

Circuit Type	STBY_A	STBY_B
Analog core	Disable	Disable
Digital data pass array control	Disable	Enable
Digital AC	Disable	Enable
Digital CLK Gen (Gated Clock Ctrl)	Enable (master clock bypass)	Enable
PLL	Disable	Enable

Note: The execution of standby will take place after the completion of the current line by default.

Spectral Characteristics

Figure 3: Typical Color Spectral Characteristics



CRA Characteristics

Figure 4: Chief Ray Angle (CRA) vs. Image Height

CRA vs. Image Height Plot

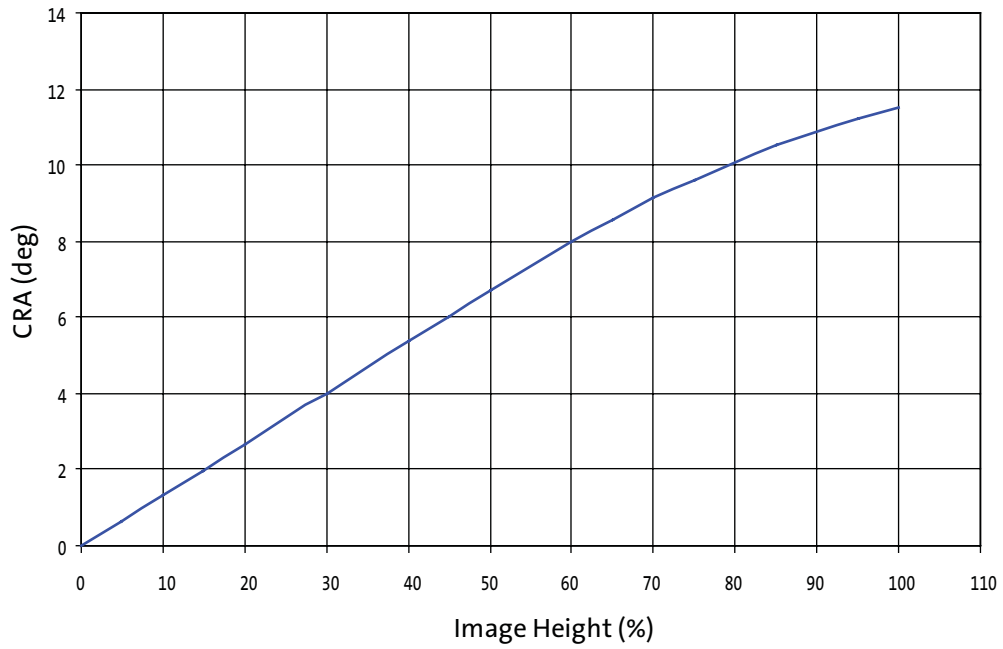


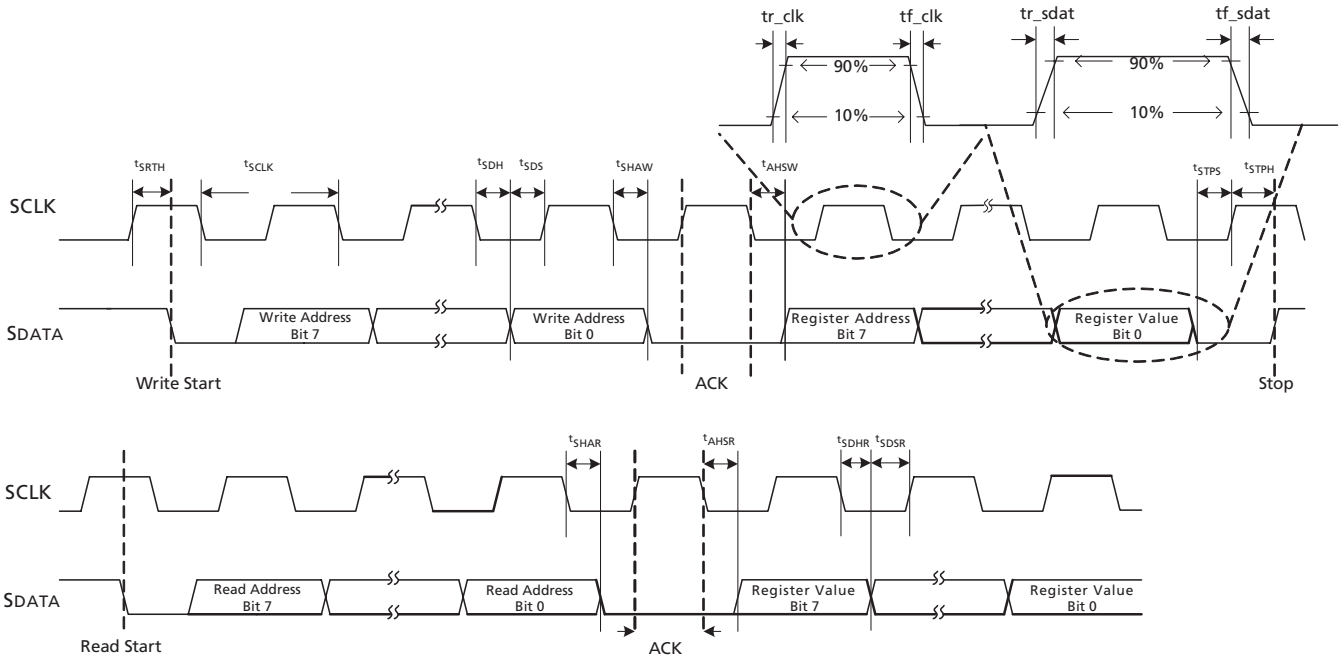
Image Height		CRA
(%)	(mm)	(deg)
0	0	0
5	0.099	0.66
10	0.198	1.32
15	0.297	1.98
20	0.396	2.66
25	0.495	3.33
30	0.594	4.01
35	0.693	4.68
40	0.792	5.36
45	0.891	6.04
50	0.990	6.71
55	1.089	7.36
60	1.188	7.98
65	1.287	8.58
70	1.386	9.13
75	1.485	9.63
80	1.584	10.09
85	1.683	10.51
90	1.782	10.90
95	1.881	11.24
100	1.980	11.53

Electrical Specifications

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 25 and Table 16 on page 8.

Figure 5: Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Table 5: Two-Wire Serial Bus Characteristics

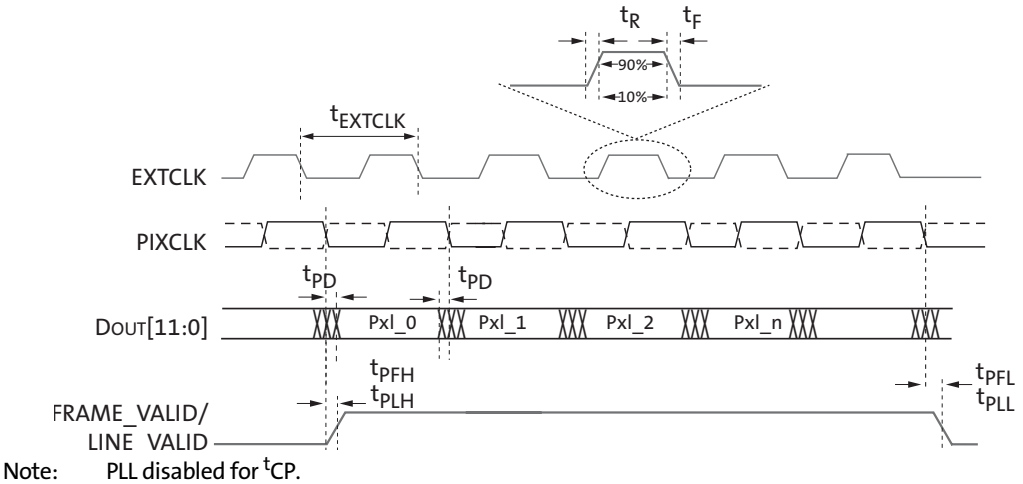
Symbol	Definition	Condition	Min	Typ	Max	Unit
^{f}SCLK	Serial interface input clock frequency	–	–	–	400	kHz
^{t}SCLK	Serial Input clock period	–	–	–	2.5	sec
	SCLK duty cycle	–	40	50	60	%
tr_sclk	SCLK rise time		–	34	–	ns
tf_sclk	SCLK fall time		–	8	–	ns
tr_sdat	SDATA rise time		–	34	–	ns
tf_sdat	SDATA fall time		–	10	–	ns
^{t}SRTH	Start hold time	WRITE/READ	0	10	28	ns
^{t}SDH	SDATA hold	WRITE	0	0	0	ns
^{t}SDS	SDATA setup	WRITE	0	19.9	59.9	ns
^{t}SHAW	SDATA hold to ACK	WRITE	279	281	300	ns
^{t}AHSW	ACK hold to SDATA	WRITE	279	281	300	ns
^{t}STPS	Stop setup time	WRITE/READ	0	0	0	ns
^{t}STPH	Stop hold time	WRITE/READ	0	0	0	ns
^{t}SHAR	SDATA hold to ACK	READ	279	284	300	ns
^{t}AHSR	ACK hold to SDATA	READ	279	284	300	ns
^{t}SDHR	SDATA hold	READ	0	0	0	ns
^{t}SDSR	SDATA setup	READ	0	19.9	59.9	ns
CIN_SI	Serial interface input pin capacitance	–	–	3.5	–	pF
CLOAD_SD	SDATA max load capacitance	–	–	15	–	pF
RSD	SDATA pull-up resistor	–	–	1.5	–	kΩ

I/O Timing

By default, the MT9M032 launches pixel data, FV, and LV with the rising edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV, and LV using the falling edge of PIXCLK.

See Figure 26 and Table 17 on page 9 for I/O timing (AC) characteristics.

Figure 6: Parallel I/O Timing Diagram



Note: PLL disabled for ^{t}CP.

Table 6: I/O Timing Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{EXTCLK}	Input clock frequency	PLL disabled	8	–	16.5	MHz
t_{EXTCLK}	Input clock period	PLL disabled	60.6	–	125	ns
f_{PIXCLK}	Output clock frequency	PLL enabled	8	–	99	MHz
t_{PIXCLK}	Output clock period	PLL enabled	10.10	–	125	ns
t_R[1]	Input clock rise time	54–99 MHz, PIXCLK, HIGH–LOW voltage, midlevel condition	1	–	60	ns
t_F[1]	Input clock fall time		1	–	60	ns
t_{RP}[1]	PIXCLK rise time		2.4	–	3	ns
t_{FP}[1]	PIXCLK fall time		2.2	–	3	ns
	EXTCLK_Dutycycle		40	50	60	%
	PIXCLK_Duty cycle	99 MHz, midlevel condition (V_{DD}, EXTCLK duty cycle were varied)	40	50	60	%
$t_{(PIX\ JITTER)}$[2]	Jitter on PIXCLK	HIGH-LOW voltage, midlevel condition	0.5	0.7	1	ps
t_{JITTER}[2]	Input clock jitter @ 8 MHz		–		–	ps
t_{JITTER}[2]	Input clock jitter @ 16.5 MHz		–		–	ps
t_{CP}	EXTCLK to PIXCLK propagation delay	54–99 MHz PixClk, HIGH–LOW voltage, midlevel condition	12.6	14.4	16	ns
f_{PIXCLK}	PIXCLK frequency		54		99	MHz
t_{PD}	PIXCLK to data valid		0.6	1.5	2.3	ns
t_{PFH}	PIXCLK to FV HIGH		1.3	1.8	2.2	ns
t_{PLH}	PIXCLK to LV HIGH		0.5	0.7	1.0	ns
t_{PFL}	PIXCLK to FV LOW		1.4	2.1	2.6	ns
t_{PLL}	PIXCLK to LV LOW		0.5	0.7	1.0	ns
C_{LOAD}[3]	Output load capacitance		–	6.5	–	pF
C_{IN}[3]	Input pin capacitance		–	2.5	–	pF

Notes:
1. EXTCLK 16.5 MHz (min rise = 5ns, max rise = 6.3 ns) V_{PP} = 2.3V midpoint 1.9V.
2. Value equal to jitter on tester.
3. Based on boards currently used for testing.

DC Electrical Characteristics

The DC electrical characteristics are shown in Table 18.

Table 7: DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Core digital voltage		1.7	1.8	1.9	V
V_{DD_IO}	I/O digital voltage		2.6	2.8	3.1	V
V_{AA}	Analog voltage		2.6	2.8	3.1	V
V_{AA_PIX}	Pixel supply voltage		2.6	2.8	3.1	V
V_{DD_PLL}	PLL supply voltage		2.6	2.8	3.1	V
V_{IH}	Input HIGH voltage	V_{DD_IO}= 2.8V	2.0	–	3.3	V
V_{IL}	Input LOW voltage	V_{DD_IO} = 2.8V	–0.3	–	0.8	V
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{DD_IO} or D_{GND}	0.0176	0.5305	1.1425	µA
V_{OH}	Output HIGH voltage	At specified I_{OH}	2.17	2.68	3.05	V
V_{OL}	Output LOW voltage	At specified I_{OL}	0.2	0.28	0.39	V
I_{OH}	Output HIGH current	At specified V_{OH}				mA
I_{OL}	Output LOW current	At specified V_{OL}				mA
I_{OZ}	Tri-state output leakage current	V_{IN} = V_{DD_IO} or GND	–	143	250	mA
I_{DD}	Digital operating current	Streaming, full resolution	20	28.0	30	mA
I_{DD_IO}	I/O digital operating current	Streaming, full resolution	25	27.3	50	mA
I_{AA}	Analog operating current	Streaming, full resolution	60	65.0	100	mA
I_{AA_PIX}	Pixel supply current	Streaming, full resolution	0	2.6705	4	mA
I_{DD_PLL}	PLL supply current	Streaming, full resolution	1	3.0	5	mA
$I_{STBY\_A\_OFF}$	Soft standby current	–	0	0.48	1.6	mA
$I_{STBY\_A\_ON}$		–	0	1.93	3.2	mA
$I_{STBY\_B\_OFF}$		–	0	6.53	8.8	mA
$I_{STBY\_B\_ON}$		–	0	40.65	55.7	mA

Table 8: Power Consumption
(at 30 fps, full resolution, 25°C)

Symbol	Parameter	Typ Current (mA)	Typ Voltage (V)	Power Parallel (mW)
P_{VDD}	Digital operating power	28.0	1.8	50.4
P_{VDDIO1}	I/O digital operating power	7.7	2.8	21.6
P_{VDDIO2} (parallel)	I/O power parallel	19.6	2.8	86.5
P_{VAA}	Analog operating power	65.0	2.8	182.0
P_{VAAPIX}	PLL supply power	5.6	2.8	15.7
P_{VDDPLL}	PLL supply power	3.0	2.8	8.4
P_{TOTAL}	Total power			364.6

Caution **Stresses greater than those listed in Table 20 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

Table 9: Absolute Maximum Values

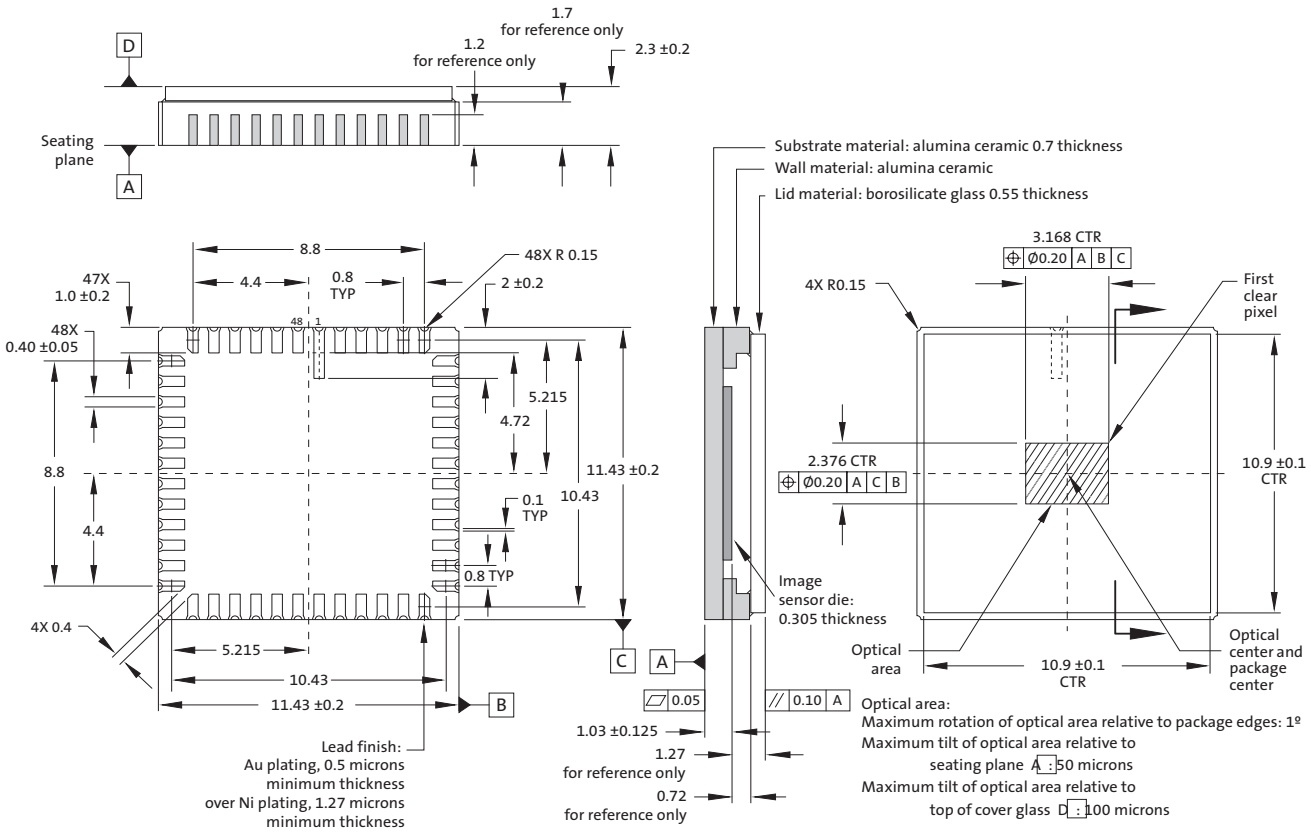
Symbol	Parameter	Condition	Min	Max	Unit
V_{DD_MAX}	Core digital voltage		–0.3	1.9	V
$V_{DD\_IO\_MAX}$	I/O digital voltage		–0.3	3.1	V
V_{AA_MAX}	Analog voltage		–0.3	3.1	V
$V_{AA\_PIX\_MAX}$	Pixel supply voltage		–0.3	3.1	V
$V_{DD\_PLL\_MAX}$	PLL supply voltage		–0.3	3.1	V
V_{IN_MAX}	Input HIGH voltage		–0.3	V_{DD_IO} + 0.3	V
I_{DD_MAX}	Digital operating current	Worst case current		28.3	mA
$I_{DD\_IO\_MAX}$	I/O digital operating current	Worst case current		54.4	mA
I_{AA_MAX}	Analog operating current	Worst case current		103	mA
$I_{AA\_PIX\_MAX}$	Pixel supply current	Worst case current		11.6	mA
$I_{DD\_PLL\_MAX}$	PLL supply current	Worst case current		7.3	mA
$I_{DD\_LVDS\_MAX}$	LVDS operating current	Worst case current			
T_{OP}	Operating temperature	Measure at junction	–30	70	°C
T_{STG}	Storage temperature		–40	85	°C

Note: This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Package Dimensions

The 48-pin CLCC package mechanical drawing is shown in Figure 27.

Figure 7: 48-Pin CLCC Package Outline



Note: All dimensions in millimeters.

Revision History

Rev. E 2/12

- Updated trademarks
- Applied new Aptina template

Rev. D 6/10

- Updated Table 16, “Two-Wire Serial Bus Characteristics,” on page 8

Rev. C 4/3/09

- Updated to Production and to Aptina template
- Updated part numbers in Table 1, “Available Part Numbers,” on page 1
- Deleted last paragraph on p. 18
- Added paragraph to “Slave Address” on page 12
- Added Table 6, “Device Addresses,” on page 12
- Added “PLL Setup Sample Code for Parallel Mode After Power-Up (with input clock frequency 13.5 MHz)” on page 33
- Added Step 4 to “Power-Up Sequence” on page 1
- Deleted “Power-Up Initial Commands” section
- Deleted “Divide by 7 Sample Code” section
- Updated Figure 23: “Typical Color Spectral Characteristics,” on page 5
- Added “CRA Characteristics” on page 6
- Updated Table 16, “Two-Wire Serial Bus Characteristics,” on page 8
- Updated Figure 26: “Parallel I/O Timing Diagram,” on page 8
- Updated Table 17, “I/O Timing Characteristics,” on page 9
- Updated Table 18, “DC Electrical Characteristics,” on page 10

Rev. B 10/29/2007

- Updated "Features" on page 1
- Updated "Applications" on page 1
- Updated Table 1, “Available Part Numbers,” on page 1
- Updated Table 2, “Key Performance Parameters,” on page 1
- Updated "Functional Overview" on page 1
- Updated Table 3, “Signal Descriptions,” on page 3
- Updated Figure 2: “48-Pin CLCC 10 x 10 Package Pinout Diagram (Top View),” on page 4
- Updated "Output Data Timing" on page 9
- Updated Table 8, “Core Registers – Register Description,” on page 20
- Updated "Analog Gain" on page 30
- Updated "PLL-Generated Master Clock" on page 32
- Updated "PLL Setup" on page 32
- Updated Table 9, “Frequency Parameters,” on page 33
- Added "Reset" on page 3
- Updated "Standby and Chip Enable (Power Save Mode)" on page 4
- Updated Table 15, “Standby Modes,” on page 4, and Table 17, “I/O Timing Characteristics,” on page 9Table 18, “DC Electrical Characteristics,” on page 10
- Update Figure 27: “48-Pin CLCC Package Outline,” on page 12

Rev. A 05/30/2007

- Initial release.