

## Introduction

The OSD335x C-SiP System-In-Package (SiP) is a self-contained computing system ideal to power the latest embedded applications. It integrates the powerful 1GHz Sitara™ ARM® Cortex®-A8 AM335x Processor from Texas Instruments, up to 1 Gigabyte (GB) of DDR3L memory, up to 16 Gigabytes (GB) of embedded Multimedia Card (eMMC) non-volatile memory, a low power, low jitter MEMS Oscillator, 4 Kilobytes (KB) EEPROM, TPS65217C PMIC, TL5209 LDO, and resistors, capacitors, and inductors into a single 27mm x 27mm easy to use IC package.

With this level of integration, the OSD335x C-SiP has everything needed to build a complete embedded computing platform. It allows designers to focus on the key aspects of their system without spending time on the complications associated with getting the processing core working. It also reduces the overall size and complexity of the design while simplifying the supply chain. The OSD335x C-SiP can significantly decrease the time to market for any embedded computing products.

## Features

- TI AM335x, TPS65217C, TL5209, DDR3, EEPROM, eMMC, MEMS Oscillator and passive components integrated into a single package
- TI AM335x Features:
  - ARM® Cortex®-A8 up to 1GHz
  - 8 channel 12-bit SAR ADC
  - Ethernet 10/100/1000 x 2
  - USB 2.0 HS OTG + PHY x2
  - MMC, SD and SDIO x3
  - LCD Controller
  - SGX 3D Graphics Engine
  - PRU Subsystem



OSD335x C-SiP Block Diagram

- Access to all\* AM335x Peripherals: CAN, SPI, UART, I2C, GPIO, etc.
- Up to 1GB DDR3
- Up to 16GB eMMC
- Low Power, Low Jitter MEMS Oscillator
- PWR In: AC Adapter, USB or Single cell (1S) Li-Ion / Li-Po Battery
- PWR Out: 1.8V, 3.3V and SYS
- Selectable I/O Voltage: 1.8V or 3.3V

## Benefits

- Integrates over 100 components
- Compatible with AM335x development tools and software
- Significantly reduces design time
- 45% reduction in board space vs discrete implementation
- Decreases layout complexity
- Wide BGA ball pitch allows for low-cost assembly
- Simplifies component sourcing
- Increased reliability through reduced number of components

## Package

- 400 Ball BGA (27mm X 27mm)
- 20 X 20 grid, 1.27mm pitch
- Temp Range: 0 to 85°C, -40 to 85°C

\* Access to All IO except those used for communicating with the eMMC

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# OSD335x C-SiP Family

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## 1 Revision History

Revision Number	Revision Date	Changes	Author
1	3/19/2019	Initial Release	Greg Sheridan, Erik Welsh, Eshtaartha Basu
2	3/20/2019	Added VIN_BAT Information; Removed RTC-only information	Erik Welsh

## 2 Block Diagram

The OSD335x C-SiP devices consist of 7 main components serving 6 distinct functions. The main processor is a 1GHz Texas Instruments Sitara™ AM335x ARM® Cortex®-A8. The power system has 2 devices from Texas Instruments, the TPS65217C Power Management IC (PMIC) and the TL5209 LDO. The system memory includes up to 1GB DDR3. A combination of a 4KB EEPROM and up to 16GB of Embedded Multimedia Card (eMMC) provide nonvolatile memory for configuration and storage. Finally, a low power, low jitter, highly stable MEMS CMOS Oscillator is used for the primary clock input. Figure 2-1 shows a detailed block diagram of the OSD335x C-SiP and breaks out the key functions of the AM335x processor.

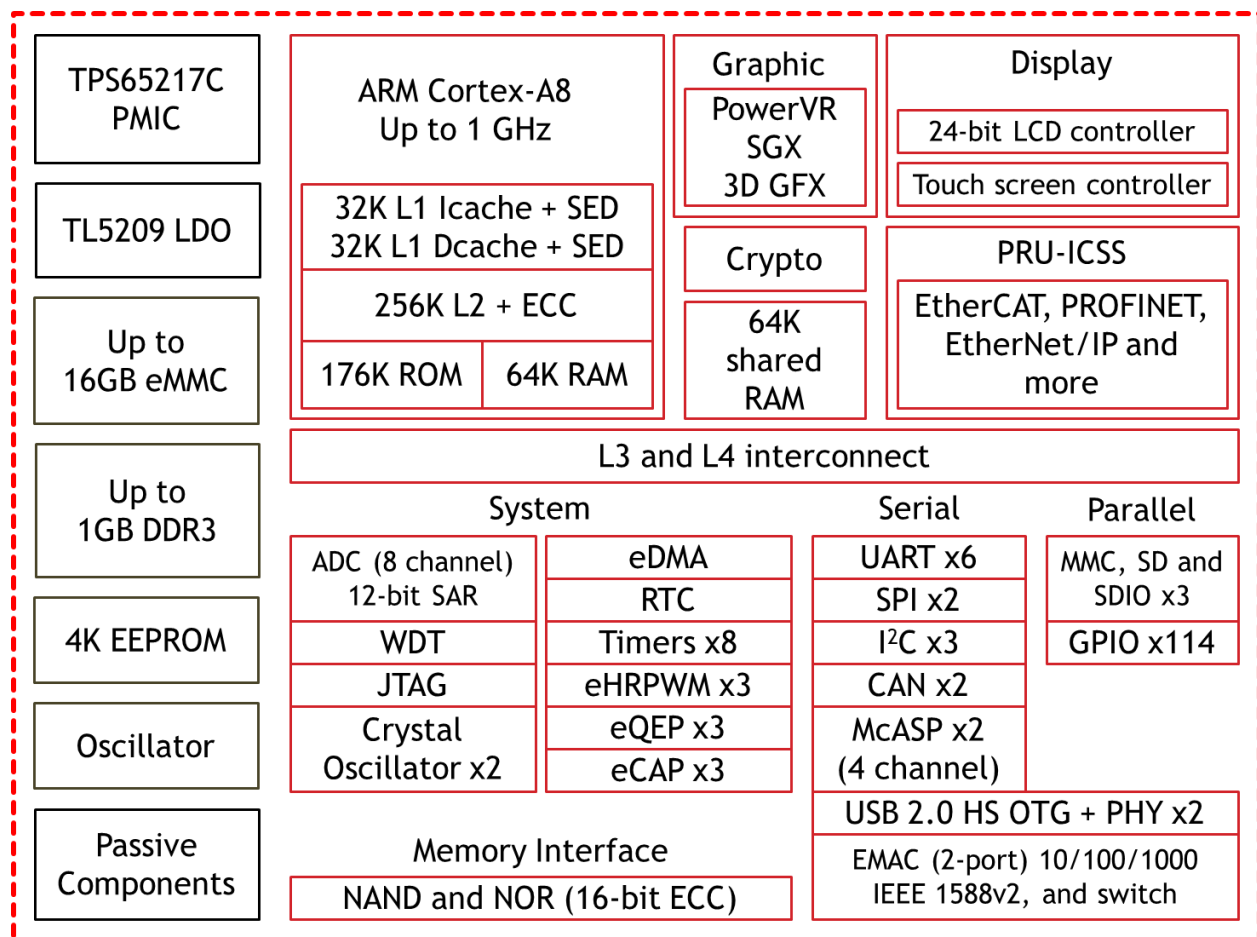


Figure 2-1 - OSD335x C-SiP Detailed Block Diagram

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## 2.1 Passives

Besides the five major components, the OSD335x C-SiP also integrates capacitors, resistors, inductors, and ferrite beads (Passives). Table 2-2 and Table 2-3 lists the equivalent capacitance and resistance integrated into the OSD335x C-SiP. This includes the approximate bulk capacitance on input and output power rails as well as all pull-up resistor locations and values. The OSD335x C-SiP does not require any external decoupling / bypass capacitors in most applications. However, it does require additional bulk capacitance on one of the output power rails.

### 2.1.1 Additional Required Bulk Capacitance

The following output power rails require additional bulk capacitance to avoid in-rush / power up issues.

Table 2-1 - OSD335x C-SiP Required Additional Capacitors (Approximate Bulk Capacitance)

From	To	Device	Description	Type	Value
SYS_VOUT	DGND	TPS65217C	SYS_VOUT output capacitance	C	~50uF

### 2.1.2 Integrated Bulk Capacitance

The following input and output power rails have bulk capacitance integrated within the SiP. This table is for informative purposes only.

Table 2-2 - OSD335x C-SiP Capacitors (Approximate Bulk Capacitance)

From	To	Device	Description	Type	Value
VIN_AC	DGND	TPS65217C	VIN_AC input capacitance	C	10uF
VIN_USB	DGND	TPS65217C	VIN_USB input capacitance	C	10uF
VIN_BAT	DGND	TPS65217C	VIN_BAT input capacitance	C	10uF
SYS_VOUT	DGND	TPS65217C	SYS_VOUT output capacitance	C	20uF
SYS_VDD1_3P3V	DGND	TL5209	SYS_VDD1_3P3V output capacitance	C	2.2uF
SYS_VDD2_3P3V	DGND	TPS65217C	SYS_VDD2_3P3V output capacitance	C	2.2uF
SYS_VDD3_3P3V	DGND	TPS65217C	SYS_VDD3_3P3V output capacitance	C	10uF
SYS_VDD_1P8V	DGND	TPS65217C	SYS_VDD_1P8V output capacitance	C	10uF
SYS_RTC_1P8V	DGND	TPS65217C	SYS_RTC_1P8V output capacitance	C	2.2uF
CAP_VDD_RTC	DGND	AM335x	CAP_VDD_RTC capacitance	C	1uF
EMMC_VCC	DGND	eMMC	EMMC_VCC input capacitance	C	2.2uF
EMMC_VCCQ	DGND	eMMC	EMMC_VCCQ input capacitance	C	2.2uF

### 2.1.3 Integrated Resistors

The following pins have pull-up or pull-down resistors integrated within the SiP. This table is for informative purposes only.

Table 2-3 - OSD335x C-SiP Resistors (Pull-ups / Pull-downs)

From	To	Device	Description	Type	Value
<b>PMIC_PWR_EN</b>	SYS_RTC_1P8V	TPS65217C	PWR_EN pull-up	R	100K Ohm
<b>EXT_WAKEUP</b>	SYS_RTC_1P8V	AM335x	EXT_WAKEUP input pull-up	R	4.7K Ohm
<b>EXTINTIN</b>	VDDSHV6	AM335x	nNMI pull-up	R	4.7K Ohm
<b>I2C0_SCL</b>	VDDSHV6	AM335x	I2C0_SCL pull-up	R	4.7K Ohm
<b>I2C0_SDA</b>	VDDSHV6	AM335x	I2C0_SDA pull-up	R	4.7K Ohm
<b>LCD_DATA14</b>	VDDSHV6	AM335x	SYSBOOT[14] pull-up	R	100K Ohm
<b>LCD_DATA15</b>	GND	AM335x	SYSBOOT[15] pull-down	R	100K Ohm
<b>PWRONRSTN_OD</b>	VDDSHV6	SN74LVC07G	Open-drain buffered output of PWRONRSTN pull-up	R	10K Ohm
<b>EEPROM_WP</b>	VDDSHV6	EEPROM	EEPROM WP pull-up	R	4.7K Ohm
<b>EMMC_RSTN</b>	EMMC_VCCQ	eMMC	eMMC reset pull-up	R	10K Ohm
<b>SYS_VDD1_CTL</b>	SYS_VDD3_3P3V	TL5209	Enable pull-up	R	100K Ohm
<b>OSC0_CTL</b>	SYS_VDD_1P8V	Oscillator	Enable pull-up	R	10K Ohm

### 3 Product Number Information

Figure 3-1 shows an example of an orderable product number for the OSD335x C-SiP family. This section explains the different sections of the product number. It will also list the valid entries and their meaning for each designator.

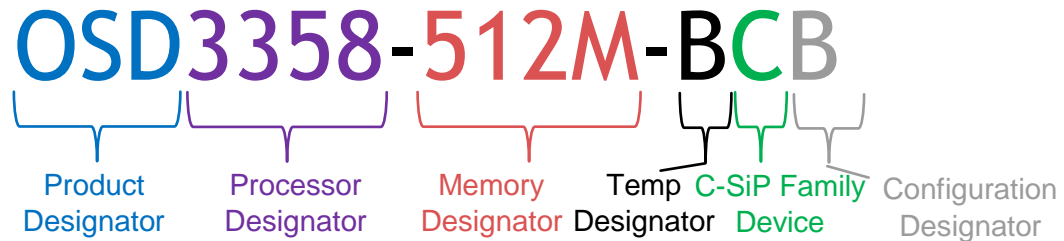


Figure 3-1. Example Product Number

**Product Designator** – Three letters that designate the family of device.

Table 3-1 - Family Designator

Family Designator	Product Line
OSD	OSD Product Line.

**Processor Designator** – A set of letters and numbers that designate the specific processor in the device. Table 3-2 shows the valid values for the Processor Designator.

Table 3-2 - Processor Designators

Processor Designator	Processor
3358	Texas Instruments AM3358

**Memory Designator** – A set of letters and numbers that designate the DDR3 memory size in the device. Table 3-3 shows the valid values for the Memory Designator.

Table 3-3 - Memory Designator

Memory Designator	DDR Memory Size
1G	1GB DDR3
512M	512 MB DDR3



**Temp Designator** – A letter or number that designates the temperature range of the device. Table 3-4 shows the valid values for the Temp Designator.

*Table 3-4 - Temp Designator*

Temp Designator	Temperature Range
B	Commercial: 0 to 85°C
I	Industrial: -40 to 85°C

**Configuration Designator** – A letter or number that designates the set of features in the device. Table 3-5 shows the valid values for the Configuration Designator unique for the OSD335x C-SiP Family.

*Table 3-5 - Trim Designator*

Trim Designator	Device Options
B	24MHz Oscillator, 4KB EEPROM, 4GB eMMC

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## 4 Reference Documents

### 4.1 Data Sheets

Below are links to the data sheets for the key devices used in the OSD335x C-SiP. Please refer to them for specifics on that device. The remainder of this document will describe how the devices are used in the OSD335x C-SiP system. It will also highlight any differences between the performance stated in the device specific datasheet and what should be expected from its operation in the OSD335x C-SiP.

- Processor      AM335X      <http://www.ti.com/product/am3358/datasheet>
- PMIC            TPS62517C   <http://www.ti.com/product/TPS65217/datasheet>
- LDO             TL509        <http://www.ti.com/product/TL5209/datasheet>
- EEPROM        24LC32A     <http://www.microchip.com/wwwproducts/en/24LC32A>

### 4.2 Other References

This section contains links to other reference documents that could be helpful when using the OSD335x C-SiP device. Some are referenced in this document.

- TI AN-2029 – Handling & Process recommendations  
<http://www.ti.com/lit/snoa550>
- OSD335x C-SiP Pin Assignments and Application Differences from TI AM3358  
[https://octavosystems.com/app\\_notes/osd335x-c-sip-family-pin-assignments/](https://octavosystems.com/app_notes/osd335x-c-sip-family-pin-assignments/)
- OSD335x C-SiP Layout Guide  
[https://octavosystems.com/app\\_notes/osd335x-c-sip-layout-guide/](https://octavosystems.com/app_notes/osd335x-c-sip-layout-guide/)
- AM335x DDR PHY register configuration for DDR3 using Software Leveling  
[http://processors.wiki.ti.com/index.php/AM335x\\_DDR\\_PHY\\_register\\_configuration\\_for\\_DDR3\\_using\\_Software\\_Leveling](http://processors.wiki.ti.com/index.php/AM335x_DDR_PHY_register_configuration_for_DDR3_using_Software_Leveling)
- AM335x Power Estimation Tool  
[http://processors.wiki.ti.com/index.php/AM335x\\_Power\\_Estimation\\_Tool](http://processors.wiki.ti.com/index.php/AM335x_Power_Estimation_Tool)
- Powering the AM335x with the TPS62517x  
<http://www.ti.com/lit/slvu551>
- OSD3358-SM Reference, Evaluation and Development Platform  
[https://octavosystems.com/octavo\\_products/osd3358-sm-red/](https://octavosystems.com/octavo_products/osd3358-sm-red/)
- AM335x and AMIC110 Sitara Processors Technical Reference Manual  
<http://www.ti.com/lit/SPRUH73>

## 5 Ball Map

The pins on the OSD335x C-SiP belong to 4 distinct categories, AM335x Signals, TPS65217C signals, control signals for internal components and Power Domains. The signal names for the AM335x and the TPS65217C have been named so they can be easily cross-referenced to the corresponding pin in the TI Datasheet.

All AM335x signals on the OSD335x C-SiP Ball Map match the signal names of the default functions in the AM335x datasheet.

All the TPS65217C signals have the prefix PMIC\_ then the TPS65217C signal name from the TI Datasheet.

***NOTE: This is true except for the signal PMIC\_POWER\_EN which is an AM335x signal.***

The arrangement of the signals has been optimized for easy escape of the BGA. Table 5-1 through Table 5-5 show the ball map for the OSD335x C-SiP.

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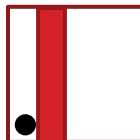
Table 5-1 - OSD335x C-SiP Ball Map Top View (Columns A-D)

	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>
<b>20</b>	DGND	VIN_USB	VIN_AC	VIN_BAT
<b>19</b>	PMIC_NRESET	VIN_USB	VIN_AC	VIN_BAT
<b>18</b>	PMIC_PB_IN	VIN_USB	VIN_AC	VIN_BAT
<b>17</b>	GPMC_AD8	WARMRSTN	PWRONRSTN_OD	DGND
<b>16</b>	GPMC_AD11	GPMC_AD10	GPMC_AD9	DGND
<b>15</b>	GPMC_AD14	GPMC_AD13	GPMC_AD12	DGND
<b>14</b>	GPMC_CLK	GPMC_CSN3	GPMC_AD15	PMIC_LDO_PGOOD
<b>13</b>	GPMC_A0	GPMC_A1	GPMC_A2	RTC_PWRONRSTN
<b>12</b>	GPMC_A3	GPMC_A4	GPMC_A5	PMIC_PGOOD
<b>11</b>	GPMC_A6	GPMC_A7	GPMC_A8	PWRONRSTN
<b>10</b>	GPMC_A9	GPMC_A10	GPMC_A11	PMIC_PWR_EN
<b>9</b>	GPMC_WPN	GPMC_WAIT0	GPMC_BEN1	PMIC_POWER_EN
<b>8</b>	NC	NC	NC	NC
<b>7</b>	NC	NC	NC	NC
<b>6</b>	NC	NC	NC	NC
<b>5</b>	NC	NC	NC	DGND
<b>4</b>	EMMC_RSTN	NC	NC	DGND
<b>3</b>	NC	NC	NC	NC
<b>2</b>	NC	NC	NC	NC
<b>1</b>	DGND	NC	NC	NC



Table 5-2 - OSD335x C-SiP Ball Map Top View (Columns E-H)

	<b>E</b>	<b>F</b>	<b>G</b>	<b>H</b>
<b>20</b>	PMIC_TS	NC	NC	NC
<b>19</b>	PMIC_BAT_SENSE	PMIC_MUX_IN	NC	NC
<b>18</b>	NC	SYS_VDD1_CTL	NC	NC
<b>17</b>	DGND	DGND	PMIC_NWAKEUP	EXT_WAKEUP
<b>16</b>	DGND	DGND	DGND	DGND
<b>15</b>	DGND	SYS_VOUT	SYS_VOUT	SYS_VDD1_3P3V
<b>14</b>	DGND	SYS_VOUT	SYS_VOUT	SYS_VDD1_3P3V
<b>13</b>	DGND	SYS_VDD2_3P3V	SYS_VDD2_3P3V	NC
<b>12</b>	DGND	SYS_VDD2_3P3V	SYS_VDD2_3P3V	NC
<b>11</b>	DGND	DGND	NC	NC
<b>10</b>	DGND	DGND	NC	NC
<b>9</b>	DGND	EMMC_VCC	EMMC_VCC	NC
<b>8</b>	DGND	EMMC_VCC	EMMC_VCC	EMMC_VCCQ
<b>7</b>	DGND	NC	NC	EMMC_VCCQ
<b>6</b>	DGND	NC	NC	NC
<b>5</b>	DGND	DGND	DGND	DGND
<b>4</b>	DGND	NC	NC	NC
<b>3</b>	NC	NC	NC	USB1_DRVVBUS
<b>2</b>	NC	NC	NC	USB1_DM
<b>1</b>	NC	NC	NC	USB1_VBUS



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Table 5-3 - OSD335x C-SiP Ball Map Top View (Columns J-M)

	<b>J</b>	<b>K</b>	<b>L</b>	<b>M</b>
<b>20</b>	NC	GPMC_CSN0	GPMC_BEN0_CLE	LCD_DATA14
<b>19</b>	NC	GPMC_OEN_REN	GPMC_ADV_N_ALE	LCD_DATA13
<b>18</b>	NC	GPMC_WEN	LCD_DATA15	LCD_DATA12
<b>17</b>	PMIC_NINT	EXTINTN	NC	NC
<b>16</b>	DGND	DGND	DGND	DGND
<b>15</b>	SYS_VDD1_3P3V	DGND	DGND	DGND
<b>14</b>	SYS_VDD1_3P3V	SYS_RTC_1P8V	SYS_RTC_1P8V	VDDS
<b>13</b>	DGND	SYS_RTC_1P8V	SYS_RTC_1P8V	VDDS_RTC
<b>12</b>	DGND	DGND	SYS_VDD3_3P3V	VDDSHV6
<b>11</b>	DGND	SYS_VDD3_3P3V	SYS_VDD3_3P3V	VDDSHV1
<b>10</b>	DGND	SYS_VDD3_3P3V	SYS_VDD3_3P3V	VDDSHV2
<b>9</b>	DGND	DGND	SYS_VDD3_3P3V	VDDSHV3
<b>8</b>	EMMC_VCCQ	DGND	SYS_VDD3_3P3V	VDDSHV5
<b>7</b>	EMMC_VCCQ	DGND	SYS_VDD3_3P3V	VDDSHV4
<b>6</b>	NC	DGND	DGND	OSC0_TP
<b>5</b>	DGND	DGND	DGND	DGND
<b>4</b>	NC	NC	NC	NC
<b>3</b>	USB1_CE	USB0_DRVBUS	USB0_CE	RMII1_REF_CLK
<b>2</b>	USB1_DP	USB0_DM	USB0_DP	EEPROM_WP
<b>1</b>	USB1_ID	USB0_VBUS	USB0_ID	OSC0_CTL

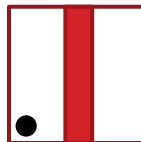
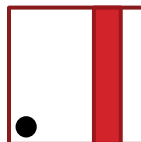


Table 5-4 - OSD335x C-SiP Ball Map Top View (Columns N-T)

	<b>N</b>	<b>P</b>	<b>R</b>	<b>T</b>
<b>20</b>	LCD_DATA11	LCD_DATA8	LCD_DATA5	LCD_DATA2
<b>19</b>	LCD_DATA10	LCD_DATA7	LCD_DATA4	LCD_DATA1
<b>18</b>	LCD_DATA9	LCD_DATA6	LCD_DATA3	LCD_DATA0
<b>17</b>	NC	NC	NC	DGND
<b>16</b>	DGND	DGND	DGND	DGND
<b>15</b>	DGND	DGND	NC	DGND
<b>14</b>	SYS_VDD_1P8V	DGND	NC	DGND
<b>13</b>	SYS_VDD_1P8V	DGND	VPP	DGND
<b>12</b>	SYS_VDD_1P8V	DGND	DGND	DGND
<b>11</b>	SYS_VDD_1P8V	SYS_VDD_1P8V	DGND	DGND
<b>10</b>	SYS_VDD_1P8V	SYS_VDD_1P8V	DGND	DGND
<b>9</b>	SYS_VDD_1P8V	DGND	DGND	DGND
<b>8</b>	SYS_VDD_1P8V	DGND	NC	DGND
<b>7</b>	SYS_VDD_1P8V	DGND	NC	DGND
<b>6</b>	DGND	DGND	NC	DGND
<b>5</b>	DGND	DGND	DGND	DGND
<b>4</b>	NC	NC	NC	DGND
<b>3</b>	MII1_TXD1	MII1_TX_EN	MII1_CRCS	MII1_RXD0
<b>2</b>	MII1_TXD0	MII1_TXD3	MII1_COL	MII1_RX_ER
<b>1</b>	MII1_TX_CLK	MII1_TXD2	MII1_RX_DV	MII1_RX_CLK



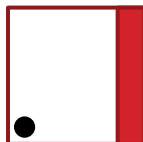
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Table 5-5 - OSD335x C-SiP Ball Map Top View (Columns U-Y)

	<b>U</b>	<b>V</b>	<b>W</b>	<b>Y</b>
<b>20</b>	LCD_PCLK	LCD_AC_BIAS_EN	TRSTN	DGND
<b>19</b>	LCD_HSYNC	EMU1	TMS	TCK
<b>18</b>	LCD_VSYNC	EMU0	TDO	TDI
<b>17</b>	DGND	MCASP0_AXR1	MCASP0_AHCLKR	MCASP0_ACLKX
<b>16</b>	DGND	MCASP0_AHCLKX	MCASP0_AXR0	MCASP0_FSX
<b>15</b>	RTC_KALDO_ENN	ECAP0_IN_PWM0_OUT	MCASP0_FSR	MCASP0_ACLKR
<b>14</b>	VDDS_RTC	XDMA_EVENT_INTR1	XDMA_EVENT_INTR0	OSC1_OUT
<b>13</b>	VDD_CORE	CAP_VDD_RTC	OSC1_GND	OSC1_IN
<b>12</b>	PMIC_MUX_OUT	AIN7	VREFP	SYS_ADC_1P8V
<b>11</b>	NC	AIN6	AIN5	AIN4
<b>10</b>	VDDS_PLL	AIN2	AIN1	AIN0
<b>9</b>	VDDS_DDR	AIN3	VREFN	AGND_ADC
<b>8</b>	PMIC_SCL	I2C0_SCL	UART1_CTSN	UART1_RTSN
<b>7</b>	PMIC_SDA	I2C0_SDA	UART1_TXD	UART1_RXD
<b>6</b>	VDD_MPU	UART0_CTSN	UART0_TXD	UART0_RXD
<b>5</b>	DGND	UART0_RTSN	SPI0_D0	SPI0_SCLK
<b>4</b>	DGND	SPI0_CS1	SPI0_D1	SPI0_CS0
<b>3</b>	MII1_RXD3	MMC0_DAT1	MMC0_CLK	MMC0_DAT0
<b>2</b>	MII1_RXD2	MMC0_DAT2	MMC0_CMD	MMC0_DAT3
<b>1</b>	MII1_RXD1	MDIO	MDC	DGND





## 5.1 Ball Description

Table 5-6 lists all the unique balls of the OSD335x C-SiP and gives their primary, i.e. pin mux mode 0, function. Most pins have multiple functions muxed together which can be selected by setting the appropriate pin muxing mode. The table also lists the equivalent pin number for the signal on the OSD335x C-SiP package and the AM335x ZCZ package. For more detail please refer to the appropriate datasheet in section 4.1. Also, please refer to the AM335x datasheet Table 4-1 for more information on the different pin muxing modes.

Table 5-6 - OSD335x C-SiP Ball Descriptions

Pin Name	Description	Pin Number	
		OSD335x C-SiP	AM335x (ZCZ)
AGND_ADC	Analog Ground (VSSA_ADC in AM335x)	Y9	E8
AIN0	Analog Input / Output	Y10	B6
AIN1	Analog Input / Output	W10	C7
AIN2	Analog Input / Output	V10	B7
AIN3	Analog Input / Output	V9	A7
AIN4	Analog Input / Output	Y11	C8
AIN5	Analog Input	W11	B8
AIN6	Analog Input	V11	A8
AIN7	Analog Input	V12	C9
CAP_VDD_RTC	RTC Supply Voltage Input	V13	D6
DGND	Digital Ground (VSS in AM335x)	See Ball Map for all DGND instances	See VSS pin in AM335x datasheet.
ECAP0_IN_PWM0_OUT	Enhanced Capture 0 Input or PWM0 Output	V15	C18
EEPROM_WP	EEPROM Write Protect Pin	M2	N/A
EMMC_RSTN	eMMC RESETN Input	A4	N/A
EMMC_VCC	eMMC VCC Input (3.3V)	F9, F8, G9, G8	N/A
EMMC_VCCQ	eMMC VCC I/O Input (3.3V)	H8, H7, J8, J7	N/A
EMU0	Miscellaneous Emulation Pin	V18	C14
EMU1	Miscellaneous Emulation Pin	V19	B14
EXTINTN	AM335x External Interrupt to ARM Cortex-A8	K17	B18
EXT_WAKEUP	AM335x EXT_WAKEUP Input	H17	C5
GPMC_A0	GPMC Address	A13	R13
GPMC_A1	GPMC Address	B13	V14
GPMC_A2	GPMC Address	C13	U14
GPMC_A3	GPMC Address	A12	T14
GPMC_A4	GPMC Address	B12	R14
GPMC_A5	GPMC Address	C12	V15
GPMC_A6	GPMC Address	A11	U15
GPMC_A7	GPMC Address	B11	T15
GPMC_A8	GPMC Address	C11	V16
GPMC_A9	GPMC Address	A10	U16
GPMC_A10	GPMC Address	B10	T16
GPMC_A11	GPMC Address	C10	V17
GPMC_AD8	GPMC Address and Data	A17	U10
GPMC_AD9	GPMC Address and Data	C16	T10
GPMC_AD10	GPMC Address and Data	B16	T11
GPMC_AD11	GPMC Address and Data	A16	U12
GPMC_AD12	GPMC Address and Data	C15	T12
GPMC_AD13	GPMC Address and Data	B15	R12
GPMC_AD14	GPMC Address and Data	A15	V13
GPMC_AD15	GPMC Address and Data	C14	U13
GPMC_ADVN_ALE	GPMC Address Valid / Address Latch Enable	L19	R7
GPMC_BEN0_CLE	GPMC Byte Enable 0 / Command Latch Enable	L20	T6
GPMC_BEN1	GPMC Byte Enable 1	C9	U18
GPMC_CLK	GPMC Clock	A14	V12
GPMC_CSN0	GPMC Chip Select	K20	V6
GPMC_CSN3	GPMC Chip Select	B14	T13

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<b>GPMC_OEN_REN</b>	GPMC Output Enable / Read Enable	K19	T7
<b>GPMC_WAIT0</b>	GPMC Wait 0	B9	T17
<b>GPMC_WEN</b>	GPMC Write Enable	K18	U6
<b>GPMC_WPN</b>	GPMC Write Protect	A9	U17
<b>I2C0_SCL</b>	I2C Clock	V8	C16
<b>I2C0_SDA</b>	I2C Data	V7	C17
<b>LCD_AC_BIAS_EN</b>	LCD AC Bias Enable Chip Select	V20	R6
<b>LCD_DATA0</b>	LCD Data Bus	T18	R1
<b>LCD_DATA1</b>	LCD Data Bus	T19	R2
<b>LCD_DATA2</b>	LCD Data Bus	T20	R3
<b>LCD_DATA3</b>	LCD Data Bus	R18	R4
<b>LCD_DATA4</b>	LCD Data Bus	R19	T1
<b>LCD_DATA5</b>	LCD Data Bus	R20	T2
<b>LCD_DATA6</b>	LCD Data Bus	P18	T3
<b>LCD_DATA7</b>	LCD Data Bus	P19	T4
<b>LCD_DATA8</b>	LCD Data Bus	P20	U1
<b>LCD_DATA9</b>	LCD Data Bus	N18	U2
<b>LCD_DATA10</b>	LCD Data Bus	N19	U3
<b>LCD_DATA11</b>	LCD Data Bus	N20	U4
<b>LCD_DATA12</b>	LCD Data Bus	M18	V2
<b>LCD_DATA13</b>	LCD Data Bus	M19	V3
<b>LCD_DATA14</b>	LCD Data Bus	M20	V4
<b>LCD_DATA15</b>	LCD Data Bus	L18	T5
<b>LCD_HSYNC</b>	LCD Horizontal Sync	U19	R5
<b>LCD_PCLK</b>	LCD Pixel Clock	U20	V5
<b>LCD_VSYNC</b>	LCD Vertical Sync	U18	U5
<b>MCASP0_ACLKR</b>	McASP0 Receive Bit Clock	Y15	B12
<b>MCASP0_ACLKX</b>	McASP0 Transmit Bit Clock	Y17	A13
<b>MCASP0_AHCLKR</b>	McASP0 Receive Master Clock	W17	C12
<b>MCASP0_AHCLKX</b>	McASP0 Transmit Master Clock	V16	A14
<b>MCASP0_AXR0</b>	McASP0 Serial Data	W16	D12
<b>MCASP0_AXR1</b>	McASP0 Serial Data	V17	D13
<b>MCASP0_FSR</b>	McASP0 Receive Frame Sync	W15	C13
<b>MCASP0_FSX</b>	McASP0 Transmit Frame Sync	Y16	B13
<b>MDC</b>	MDIO Clock	W1	M18
<b>MDIO</b>	MDIO Data	V1	M17
<b>MII1_COL</b>	MII Collision	R2	H16
<b>MII1_CRS</b>	MII Carrier Sense	R3	H17
<b>MII1_RX_CLK</b>	MII Receive Clock	T1	L18
<b>MII1_RX_DV</b>	MII Receive Data Valid	R1	J17
<b>MII1_RX_ER</b>	MII Receive Data Error	T2	J15
<b>MII1_RXD0</b>	MII Receive Data	T3	M16
<b>MII1_RXD1</b>	MII Receive Data	U1	L15
<b>MII1_RXD2</b>	MII Receive Data	U2	L16
<b>MII1_RXD3</b>	MII Receive Data	U3	L17
<b>MII1_TX_CLK</b>	MII Transmit Clock	N1	K18
<b>MII1_TX_EN</b>	MII Transmit Enable	P3	J16
<b>MII1_TXD0</b>	MII Transmit Data	N2	K17
<b>MII1_TXD1</b>	MII Transmit Data	N3	K16
<b>MII1_TXD2</b>	MII Transmit Data	P1	K15
<b>MII1_TXD3</b>	MII Transmit Data	P2	J18
<b>MMC0_CLK</b>	MMC/SD/SDIO Clock	W3	G17
<b>MMC0_CMD</b>	MMC/SD/SDIO Command	W2	G18
<b>MMC0_DAT0</b>	MMC/SD/SDIO Data	Y3	G16
<b>MMC0_DAT1</b>	MMC/SD/SDIO Data	V3	G15
<b>MMC0_DAT2</b>	MMC/SD/SDIO Data	V2	F18
<b>MMC0_DAT3</b>	MMC/SD/SDIO Data	Y2	F17
<b>NC</b>	Do Not Connect	See Ball Map for all NC instances	N/A
<b>OSC0_CTL</b>	High Frequency Oscillator enable (Pulled High)	M1	N/A
<b>OSC0_TP</b>	Internal Oscillator Test Point	M6	N/A
<b>OSC1_GND</b>	Real Time Clock Oscillator Ground (VSS_RTC)	W13	A5
<b>OSC1_IN</b>	Real Time Clock Oscillator Input (RTC_XTALIN)	Y13	A6

<b>OSC1_OUT</b>	Real Time Clock Oscillator Output (RTC_XTALOUT)	Y14	A4
<b>PMIC_BAT_SENSE</b>	TPS65217C BAT_SENSE Input	E19	N/A
<b>PMIC_LDO_PGOOD</b>	TPS65217C LDO_PGOOD Output	D14	N/A
<b>PMIC_MUX_IN</b>	TPS65217C MUX_IN Input	F19	N/A
<b>PMIC_MUX_OUT</b>	TPS65217C MUX_OUT Output	U12	N/A
<b>PMIC_NINT</b>	TPS65217C NINT Output	J17	N/A
<b>PMIC_NRESET</b>	TPS65217C NRESET Input	A19	N/A
<b>PMIC_NWAKEUP</b>	TPS65217C NWAKEUP Output	G17	N/A
<b>PMIC_PB_IN</b>	TPS65217C PB_IN Input	A18	N/A
<b>PMIC_PGOOD</b>	TPS65217C PGOOD Output	D12	N/A
<b>PMIC_POWER_EN</b>	AM335x PMIC_POWER_EN Output	D9	C6
<b>PMIC_PWR_EN</b>	TPS65217C PWR_EN Input	D10	N/A
<b>PMIC_SCL</b>	TPS65217C SCL Input	U8	N/A
<b>PMIC_SDA</b>	TPS65217C SDA Input / Output	U7	N/A
<b>PMIC_TS</b>	TPS65217C TS Input	E20	N/A
<b>PWRONRSTN</b>	Power On Reset Input (Active Low)	D11	B15
<b>PWRONRSTN_OD</b>	Open-Drain buffer output (Pulled High)	C17	N/A
<b>RMII1_REF_CLK</b>	RMII Reference Clock	M3	H18
<b>RTC_KALDO_ENN</b>	Enable input for internal CAP_VDD_RTC voltage regulator (Active Low)	U15	B4
<b>RTC_PWRONRSTN</b>	RTC Reset Input (Active Low)	D13	B5
<b>SPI0_CS0</b>	SPI Chip Select	Y4	A16
<b>SPI0_CS1</b>	SPI Chip Select	V4	C15
<b>SPI0_D0</b>	SPI Data	W5	B17
<b>SPI0_D1</b>	SPI Data	W4	B16
<b>SPI0_SCLK</b>	SPI Clock	Y5	A17
<b>SYS_ADC_1P8V</b>	Output Power Supply, Analog, 1.8VDC	Y12	N/A
<b>SYS_RTC_1P8V</b>	Output Power Supply, RTC, 1.8VDC	K14, K13, L14, L13	N/A
<b>SYS_VDD_1P8V</b>	Output Power Supply, Digital, 1.8VDC	N14, N13, N12, N11, N10, N9, N8, N7, P11, P10	N/A
<b>SYS_VDD1_CTL</b>	SYS_VDD1_3P3V enable (Pulled High)	F18	N/A
<b>SYS_VDD1_3P3V</b>	Output Power Supply, Primary, 3.3VDC	H15, H14, J15, J14	N/A
<b>SYS_VDD2_3P3V</b>	Output Power Supply, Secondary, 3.3VDC	F13, F12, G13, G12	N/A
<b>SYS_VDD3_3P3V</b>	Output Power Supply, I/O, 3.3VDC	K11, K10, L12, L11, L10, L9, L8, L7	N/A
<b>SYS_VOUT</b>	TPS65217C SYS Output	F15, F14, G15, G14	N/A
<b>TCK</b>	JTAG Test Clock	Y19	A12
<b>TDI</b>	JTAG Test Data Input	Y18	B11
<b>TDO</b>	JTAG Test Data Output	W18	A11
<b>TMS</b>	JTAG Test Mode Select	W19	C11
<b>TRSTN</b>	JTAG Test Reset	W20	B10
<b>UART0_CTSN</b>	UART Clear to Send	V6	E18
<b>UART0_RTSN</b>	UART Request to Send	V5	E17
<b>UART0_RXD</b>	UART Receive Data	Y6	E15
<b>UART0_TXD</b>	UART Transmit Data	W6	E16
<b>UART1_CTSN</b>	UART Clear to Send	W8	D18
<b>UART1_RTSN</b>	UART Request to Send	Y8	D17
<b>UART1_RXD</b>	UART Receive Data	Y7	D16
<b>UART1_TXD</b>	UART Transmit Data	W7	D15
<b>USB0_CE</b>	USB0 Charger Enable Output	L3	M15
<b>USB0_DM</b>	USB0 Data (-)	K2	N18
<b>USB0_DP</b>	USB0 Data (+)	L2	N17
<b>USB0_DRVVBUS</b>	USB0 VBUS Control Output	K3	F16
<b>USB0_ID</b>	USB0 OTG ID	L1	P16
<b>USB0_VBUS</b>	USB0 VBUS	K1	P15
<b>USB1_CE</b>	USB1 Charger Enable Output	J3	P18
<b>USB1_DM</b>	USB1 Data (-)	H2	R18
<b>USB1_DP</b>	USB1 Data (+)	J2	R17
<b>USB1_DRVVBUS</b>	USB1 VBUS Control Output	H3	F15
<b>USB1_ID</b>	USB1 OTG ID	J1	P17
<b>USB1_VBUS</b>	USB1 VBUS	H1	T18

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VDD_CORE	Internal Power Supply Test Point	U13	N/A
VDD_MPU	Internal Power Supply Test Point	U6	N/A
VDDS_DDR	Internal Power Supply Test Point	U9	N/A
VDDS_PLL	Internal Power Supply Test Point	U10	N/A
VDDS_RTC	Supply voltage for RTC domain	M13, U14	D7
VDDS	Supply voltage for 1.8V IO domain	M14	E6, E14, F9, K13, N6, P9, P14
VDDSHV1	Supply voltage for the dual-voltage IO domain	M11	P7, P8
VDDSHV2	Supply voltage for the dual-voltage IO domain	M10	P10, P11
VDDSHV3	Supply voltage for the dual-voltage IO domain	M9	P12, P13
VDDSHV4	Supply voltage for the dual-voltage IO domain	M7	H14, J14
VDDSHV5	Supply voltage for the dual-voltage IO domain	M8	K14, L14
VDDSHV6	Supply voltage for the dual-voltage IO domain	M12	E10, E11, E12, E13, F14, G14, N5, P5, P6
VIN_AC	TPS65217C AC Input	C20, C19, C18	N/A
VIN_BAT	TPS65217C BAT Input / Output	D20, D19, D18	N/A
VIN_USB	TPS65217C USB Input	B20, B19, B18	N/A
VPP	Reserved	R13	M5
VREFN	Analog Negative Reference Input	W9	A9
VREFP	Analog Positive Reference Input	W12	B9
WARMRSTN	Warm Reset (Active Low)	B17	A10
XDMA_EVENT_INTR0	External DMA Event or Interrupt 0	W14	A15
XDMA_EVENT_INTR1	External DMA Event or Interrupt 1	V14	D14

## 5.2 Internal Use Only AM335x Signal Pins

The following signal pins of the AM335x ZCZ package are for internal use only within the OSD335x and are not made accessible to the user. These pins are connected to the eMMC module within the OSD335x C-SiP.

Table 5-7 - Internal Use Only AM335x Pins

Pin Name	Description	Pin Number	
		OSD335x C-SiP	AM335x (ZCZ)
GPMC_AD0	GPMC Address and Data	N/A	U7
GPMC_AD1	GPMC Address and Data	N/A	V7
GPMC_AD2	GPMC Address and Data	N/A	R8
GPMC_AD3	GPMC Address and Data	N/A	T8
GPMC_AD4	GPMC Address and Data	N/A	U8
GPMC_AD5	GPMC Address and Data	N/A	V8
GPMC_AD6	GPMC Address and Data	N/A	R9
GPMC_AD7	GPMC Address and Data	N/A	T9
GPMC_CSN1	GPMC Chip Select	N/A	U9
GPMC_CSN2	GPMC Chip Select	N/A	V9

### 5.3 Not Connected Balls

The OSD335x C-SiP ball map contains balls which are marked NC (No Connect). These balls must remain unconnected on the system PCB since they may be used for other purposes in future versions of the OSD335x C-SiP.

### 5.4 Reserved Signals



There is a subset of signals that are available on the OSD335x C-SiP ball map but **should not be** used externally to the device. These signals are used internally to the OSD335x C-SiP and using them could significantly affect the performance of the device. They are provided for test purposes only. The list of signals that should not be used can be found in Table 5-8.

Table 5-8 - Reserved Signals

Reserved Signals
VPP
VDD_CORE
VDD_MPU
VDDS_DDR
VDDS_PLL

## 6 OSD335x C-SiP Components

The OSD335x C-SiP integrates the Texas Instruments ARM® Cortex®-A8 Sitara™ AM335x processor along with the TI TPS65217C PMIC, the TI TL5209 LDO, up to 1 GB of DDR3 Memory, a 4KB EEPROM and up to 16GB of eMMC memory for non-volatile storage, a MEMS Oscillator for the primary clock input, and the resistors, capacitors, and inductors into a single design-in-ready package. The following section contains any specific device information needed for the integrated components to design your system with the OSD335x C-SiP. Specifics on the Power Management System will be covered in Section 7.

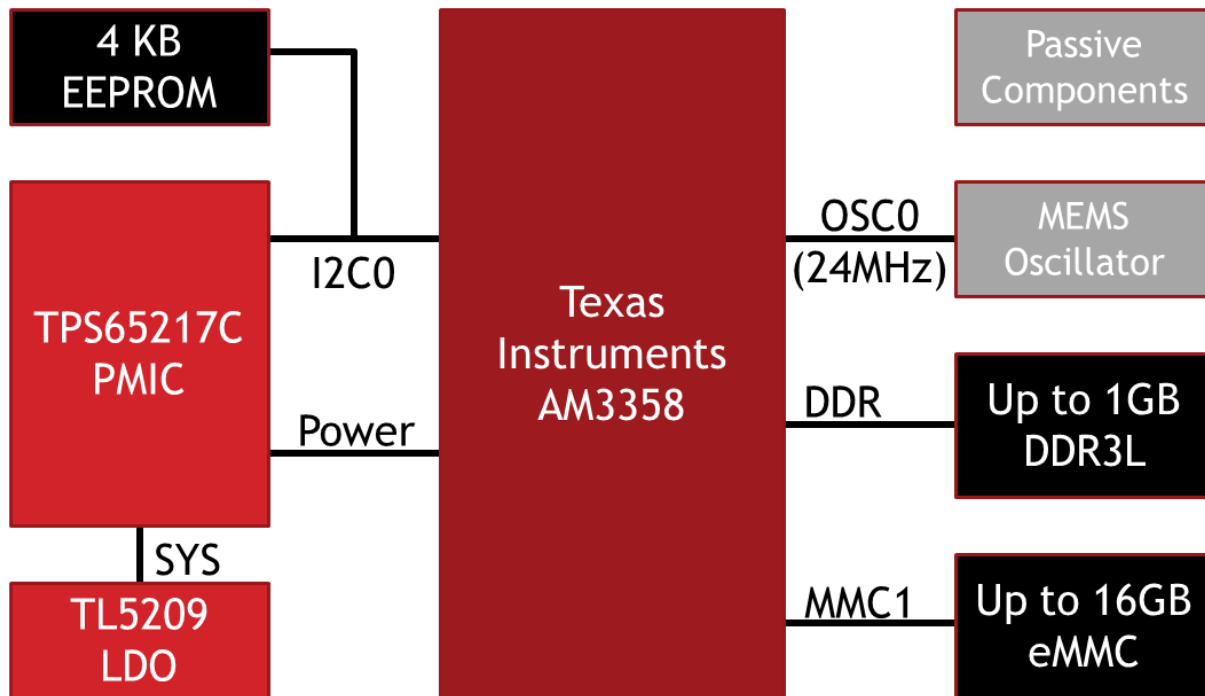


Figure 6-1 - OSD335x C-SiP Internal Connections Block Diagram

## 6.1 AM335x Processor

The heart of the OSD335x C-SiP is the Texas Instruments ARM® Cortex®-A8 Sitara™ AM335x processor. The processor in the OSD335x C-SiP is configured to perform identically to a standalone device. Please refer to the data sheet in the Reference Documents section for details on using the AM335x processor.

### 6.1.1 I/O Voltages



The OSD335x C-SiP allows the I/O voltage domains (VDDSHVx) of the AM335x to be set to either 1.8V or 3.3V. The VDDSHVx pins of the OSD335x C-SiP (ie VDDSHV1 thru VDDSHV6), which can be found in Table 5-6, must be connected to either a 1.8V or 3.3V power source in order to provide power to the I/Os. Recommendations on how to connect the I/O voltage domain pins is in the OSD335x C-SiP Layout Guide in the Reference Documents section.

See the AM335x datasheet in the Reference Documents section for more information on the pins associated with each I/O voltage domain.

### 6.1.2 Reset Circuitry

The OSD335x C-SiP contains a SN74LVC1G07 open-drain buffer whose input is PWRONRSTN and whose output PWRONRSTN\_OD is pulled to VDDHSV6 via a resistor (see Table 2-3 for more information). The PMIC\_PGOOD, PWRONRSTN, PWRONRSTN\_OD, and WARMRSTN signals can be connected as recommended in the AM335x Technical Reference Manual (see “External Buffer for nRESETIN\_OUT” figure). This component is not required to be used, or can be used in conjunction with an external reset supervisor. Figure 6-2 shows the AM335x reset connections brought out to pins of the OSD335x C-SiP.

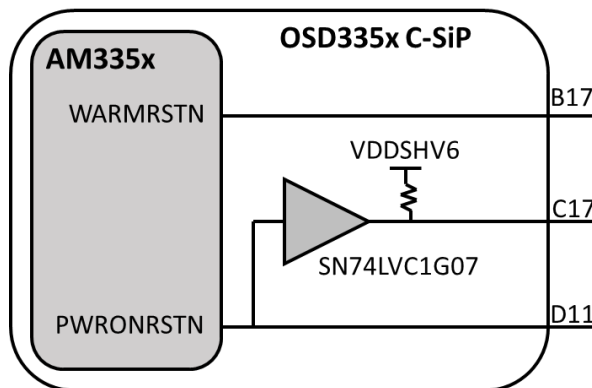


Figure 6-2 - OSD335x C-SiP Reset Circuitry

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## 6.2 DDR3 Memory

The OSD335x C-SiP integrates a DDR3 memory into the device and handles all the connections needed between the AM335x and the DDR3. You will still have to set the proper registers to configure the AM335x DDR PHY to work correctly with the memory included in the OSD335x C-SiP. Typically, this would require you to run through the procedure outlined in the AM335x DDR PHY register configuration for DDR3 using Software Leveling referred to in the Reference Documents section of this document. This procedure has been run for the OSD335x C-SiP and a list of the recommended values for the registers is provided in Table 6-1. It is recommended that you use this set of values for optimal performance.

Table 6-1 - AM335x DDR EMIF, PHY and Control Module Register Settings

Register Name	Peripheral	Recommended Value
DDR_CMDx_IOCTL <sup>(1)</sup>	Control Module	0x0000018B
DDR_DATAx_IOCTL <sup>(2)</sup>	Control Module	0x0000018B
SDRAM_CONFIG	EMIF	0x61C05332
SDRAM_CONFIG_2	EMIF	0x00000000
SDRAM_REF_CTRL	EMIF	0x00000C30
SDRAM_TIM_1	EMIF	0x0AAAD4DB
SDRAM_TIM_2	EMIF	0x266B7FDA
SDRAM_TIM_3	EMIF	0x501F867F
ZQ_CONFIG	EMIF	0x50074BE4
DDR_PHY_CTRL_1	EMIF	0x00100007
CMDx_REG_PHY_CTRL_SLAVE_RATIO_0 <sup>(1)</sup>	DDR PHY	0x00000080
CMDx_REG_PHY_INVERT_CLKOUT_0 <sup>(1)</sup>	DDR PHY	0x00000000
DATAx_REG_PHY_RD_DQS_SLAVE_RATIO_0 <sup>(2)</sup>	DDR PHY	0x0000003A
DATAx_REG_PHY_WR_DQS_SLAVE_RATIO_0 <sup>(2)</sup>	DDR PHY	0x00000045
DATAx_REG_PHY_FIFO_WE_SLAVE_RATIO_0 <sup>(2)</sup>	DDR PHY	0x00000095
DATAx_REG_PHY_WR_DATA_SLAVE_RATIO_0 <sup>(2)</sup>	DDR PHY	0x0000007F

<sup>(1)</sup> "CMDx" refers to registers where x is in [0, 1, 2]

<sup>(2)</sup> "DATAx" refers to registers where x is in [0, 1]

Settings in Table 6-1 are recommended and supported. Other values may work but are not guaranteed. If you want to rerun the calibration yourself the seed values provided in Table 6-2 should be used.

Table 6-2 - AM335x DDR PHY Calibration Seed Values

DATAx_PHY_RD_DQS_SLAVE_RATIO	40
DATAx_PHY_FIFO_WE_SLAVE_RATIO	64
DATAx_PHY_WR_DQS_SLAVE_RATIO	0



### 6.3 MEMS Oscillator

The OSD335x C-SiP integrates a low power, low jitter MEMS Oscillator that provides the main input clock to the AM335x on OSC0. Oscillator parameters can be found in Table 6-3.

*Table 6-3 - MEMS Oscillator Parameters*

Parameter	Min	Typ	Max	Units	Notes
Active Supply Current		3.0	5.0	mA	
Standby Supply Current			50	μA	
Frequency Stability			±25	ppm	All temp ranges
Aging			±5	ppm	First year @ 25C
			±1	ppm	Per year after first year
Period Jitter, RMS			15	ps <sub>RMS</sub>	
Cycle-to-Cycle Jitter			100	ps	
Frequency		24		MHz	

The MEMS Oscillator is the primary clock source for the AM335x. The boot mode resistors (SYSBOOT[15:14]) have already been set appropriately to match the oscillator frequency within the device (i.e. a value of 0b01 to signify a 24 MHz input). See Table 2-3 for more information on boot mode resistor values.

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### 6.4 eMMC

The OSD335x C-SiP contains an Embedded Multimedia Card (eMMC) device connected to the MMC1 interface of the AM335x (See Table 5-7 for more information on the pins used to connect the eMMC). The AM335x supports version 4.3 of the MMC specification which is also supported by the eMMC. This large non-volatile storage medium can be used as the primary storage medium and boot device for the AM335x. It can hold an operating system such as Linux and/or be used for data storage.

The size of the eMMC is defined per the configuration outlined in Section 3. See the Minimum Connections section for required connections to use the eMMC.

#### 6.4.1 Powering the eMMC

Both the EMMC\_VCC and EMCC\_VCCQ power inputs should be connected to SYS\_VDD1\_3P3V.

#### 6.4.2 Booting from the eMMC

The eMMC is connected to the MMC1 interface of the AM335x. This interface is a boot source, meaning an operating system can be loaded onto the eMMC making it a completely self-contained computing device. To use the integrated eMMC as a boot source the boot resistors (SYSBOOT[4:0]) need to be set the following way:

Table 6-4 - eMMC Boot Modes

SYSBOOT[4:0]	Boot Sequence			
	1st	2nd	3rd	4th
11100b	MMC1	MMC0	UART0	USB0

This table does not represent all the options for the boot mode resistors. For more information on the Boot Mode resistors and the different boot mode options please refer to Booting Section in the AM335x and AMIC110 Sitara Processors Technical Reference Manual in the Other References Section.



It is not required that the integrated eMMC be used to boot the device. The OSD335x C-SiP supports all of the boot modes outlined in the AM335x and AMIC110 Sitara Processors Technical Reference Manual.

## 6.5 EEPROM

The OSD335x C-SiP contains a 4KB EEPROM for non-volatile storage of configuration information. The EEPROM is connected to I2C0 at the 7-bit I2C address 0x50 (0b1010000). Please refer to the data sheet in the Reference Documents section for details on using the EEPROM.

### 6.5.1 EEPROM Contents

EEPROM address space 0x000 to 0xEFF is empty and can be used for board specific information during system boot. The final 256 bytes of the EEPROM (0xF00 to 0xFFF) are reserved for device specific information. The reserved space contents of the EEPROM can be found in Table 6-5

*Table 6-5 - EEPROM Contents Programmed by Octavo Systems*

Name	Description	Size (bytes)	Start address	End address	Contents
RSVD	Reserved for Future Use	256	0xF00	0xFFF	All 0xFF

### 6.5.2 EEPROM Write Protection

By default, the EEPROM is write protected (ie. the EEPROM\_WP pin is pulled high as seen in Table 2-2). To program values into the EEPROM, it is required to drive the EEPROM\_WP pin to a logic low. See the OSD335x C-SiP Layout Guide in the Reference Documents section for layout / manufacturing recommendations for the EEPROM\_WP pin.



## 7 Power Management

The power management portion of the OSD335x C-SiP consists of two devices, the TPS65217C (PMIC) and the TL5209 (LDO). The PMIC provides the necessary power rails to the AM335x and the DDR3 while the LDO is not used inside the SiP. Both devices provide power supply outputs that may be used to power circuitry external to the OSD335x C-SiP. This section describes how to power the OSD335x C-SiP in a system and the outputs that can be used.

### 7.1 Input Power

The OSD335x C-SiP may be powered by any combination of the following input power supplies. Please refer to the TPS65217C datasheet for details.



The maximum risetime for input rails VIN\_AC and VIN\_USB (defined as time for the input voltage to rise from 100 mV to 4.5 V) is 50 ms. The device may fail to power up properly if this requirement is not met.

#### 7.1.1 VIN\_AC

The OSD335x C-SiP may be powered by an external AC Adaptor at 5.0 VDC.

#### 7.1.2 VIN\_USB

The OSD335x C-SiP may be powered by a USB port at 5.0 VDC.

#### 7.1.3 VIN\_BAT

The OSD335x C-SiP may be powered by a single cell (1S) Li-Ion or Li-Polymer Battery nominally at 3.7 VDC.



Due to the dropout behavior of the LDO TL5209, the output voltage rail SYS\_VDD1\_3P3V cannot be used once VIN\_BAT drops below 3.5V. Please refer to the TL5209 datasheet for details.



When VIN\_BAT is not used, it must be connected to PMIC\_BAT\_SENSE.

### 7.2 Output Power

The OSD335x C-SiP produces the following output power supplies.

#### 7.2.1 SYS\_VOUT: Switched VIN\_AC, VIN\_USB, or VIN\_BAT

The OSD335x C-SiP contains a shared supply to power the AM335x, DDR3, and TL5209 which is also used to power external circuitry. This is supplied by the TPS65217C SYS output. The SYS output is a switched connection to one of the input power supplies selected by the TPS65217C as described in the datasheet for that device.



SYS\_VOUT requires ~50uF of additional capacitance to maintain stability. This must be added externally.

### 7.2.2 SYS\_VDD1\_3P3V

The OSD335x C-SiP contains a dedicated 3.25 VDC supply<sup>1</sup> to power external circuitry. This is supplied by the TL5209, powered by the TPS65217C SYS output, and enabled by the TPS65217C LDO4.



Due to the dropout behavior of the LDO TL5209, the output voltage rail SYS\_VDD1\_3P3V cannot be used once VIN\_BAT drops below 3.5V. Please refer to the TL5209 datasheet for details.

### 7.2.3 SYS\_VDD2\_3P3V

The OSD335x C-SiP contains a dedicated 3.3 VDC supply to power external circuitry. This is supplied by the TPS65217C LDO2.

### 7.2.4 SYS\_VDD3\_3P3V

The OSD335x C-SiP contains a shared 3.3 VDC supply that can be used to power the AM335x I/O domains (VDDSHVx). This is supplied by the TPS65217C LDO4.

### 7.2.5 SYS\_RTC\_1P8V

The OSD335x C-SiP contains a shared 1.8 VDC supply to power the AM335x RTC which may also be used to power external circuitry. This is supplied by the TPS65217C LDO1.



Please note that the AM335x in the OSD335x is powered by TPS65217 PMIC **version C**. RTC-Only mode cannot be supported at this time.

### 7.2.6 SYS\_VDD\_1P8V

The OSD335x C-SiP contains a shared 1.8 VDC supply that may be used to power the AM335x I/O domains (VDDSHVx) and external circuitry. It also supplies power to the AM335x SRAM, PLLs and USB. This is supplied by the TPS65217C LDO3.

### 7.2.7 SYS\_ADC\_1P8V

The OSD335x C-SiP contains a shared 1.8 VDC supply to power the AM335x ADC which may also be used to power external analog circuitry. This is supplied by the TPS65217C LDO3 and filtered for analog applications.

## 7.3 Internal Power



The OSD335x C-SiP has internal power supplies that are not available to power external circuitry. To do so will prevent the OSD335x C-SiP from functioning properly. The power supplies are accessible externally for monitoring purposes only.

### 7.3.1 VDDS\_DDR

The OSD335x C-SiP contains a dedicated 1.5 VDC supply to power the AM335x DDR3 interface and the DDR3 device. This is supplied by the TPS65217C DCDC1.

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<sup>1</sup> The LDO has an accuracy of 1 – 2% depending on the ambient temperature which will also affect the nominal voltage. See the TL5209 datasheet for more information.

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### 7.3.2 VDD\_MPU

The OSD335x C-SiP contains a dedicated 1.1 VDC supply to power the AM335x MPU domain. This is supplied by the TPS65217C DCDC2.

### 7.3.3 VDD\_CORE

The OSD335x C-SiP contains a dedicated 1.1 VDC supply to power the AM335x CORE domain. This is supplied by the TPS65217C DCDC3.

### 7.3.4 VDDS\_PLL

The OSD335x C-SiP contains a filtered 1.8 VDC supply to power the AM335x PLLs and oscillators. This is supplied by the TPS65217C LDO3.

## 7.4 Total Current Consideration



The total current consumption of all power rails must not exceed the recommended input currents described in Table 8-2. This includes power consumption within the SiP from the AM335x and the DDR3, as well as all external loads on the output power rails from Section 7.2.

The power consumed by the AM335x can be estimated using the *AM335x Power Estimation Tool* found in the Reference Documents section of this document. When estimating power consumption, the efficiencies and types of the OSD335x C-SiP internal power supplies must be considered. Refer to the “*Connections Diagram for TPS65217C and AM335x*” section of *Powering the AM335x with the TPS65217x* found in the Reference Documents section of this document for more information on the power supplies providing power to the AM335x.

## 7.5 Minimum Connections

In order to use the OSD335x C-SiP, a minimum set of connections must be made between pins of the OSD335x C-SiP for proper operation. These include pins for: eMMC power, IO voltage domains, Processor – PMIC interface, RTC.

### 7.5.1 Minimum eMMC power connections

The eMMC power inputs EMMC\_VCC and EMMC\_VCCQ should be connected to SYS\_VDD1\_3P3V.

### 7.5.2 Minimum IO voltage domain connections

The IO pins of AM335x are divided into 6 pin groups. The IO voltage levels of a pin group can be configured by connecting the voltage domain pins to the required voltage level. Table 7-1 lists recommended connections for each VDDSHV pin according to the voltage level required. These connections are required for IO pins of OSD335x C-SiP to function properly.

*Table 7-1 - VDDSHVx connections for OSD335x C-SiP*

Voltage Domain	Pin	Voltage Level	Recommended pin connection
<b>VDDSHV1</b>	M11	3.3V	L11
		1.8V	N11
<b>VDDSHV2</b>	M10	3.3V	L10
		Must be 3.3V to support eMMC.	
<b>VDDSHV3</b>	M9	3.3V	L9
		1.8V	N9
<b>VDDSHV4</b>	M7	3.3V	L7
		1.8V	N7
<b>VDDSHV5</b>	M8	3.3V	L8
		1.8V	N8
<b>VDDSHV6</b>	M12	3.3V	L12
		1.8V	N12

### 7.5.3 Minimum Processor-PMIC interface Connections

Table 7-2 lists the signals required to coordinate the operation of the AM335x and TPS65217C. Figure 7-1 and Figure 7-2 illustrate the required connections between the AM335x and the TPS65217C with the RTC subsystem disabled and the RTC subsystem enabled without the RTC-only power mode, respectively. These connections are the minimum required to operate the device in corresponding mode. The accessibility of these signals enables other uses of reset, power control, power status, interrupt, wakeup, and serial communication signals.

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Figure 7-1 and Figure 7-2 illustrate the interface between the AM335x and TPS65217C.

Table 7-2 - AM335x and TPS65217C Signal Descriptions

Signal	Description	Notes
PMIC_POWER_EN	PMIC Power Enable from AM335x	
PMIC_PWR_EN	PMIC Power Enable to TPS65217C	1
I2C0_SCL	I2C0 SCL from AM335x	1
PMIC_SCL	I2C SCL to TPS65217C	
I2C0_SDA	I2C0 SDA from AM335x	1
PMIC_SDA	I2C SDA to TPS65217C	
PMIC_PGOOD	PGOOD from TPS65217C	
PWRONRSTN	PWRONRSTN to AM335x	
PMIC_LDO_PGOOD	LDO_PGOOD from TPS65217C	
RTC_PWRONRSTN	RTC_PWRONRSTN to AM335x	
PMIC_NINT	NINT from TPS65217C	
EXTINTN	EXTINTN to AM335x	1
PMIC_NWAKEUP	NWAKEUP from TPS65217C	
EXT_WAKEUP	EXT_WAKEUP to AM335x	1

1. See Table 2-2 for pull up on this signal

When the RTC is disabled, the following signal connections should be used:

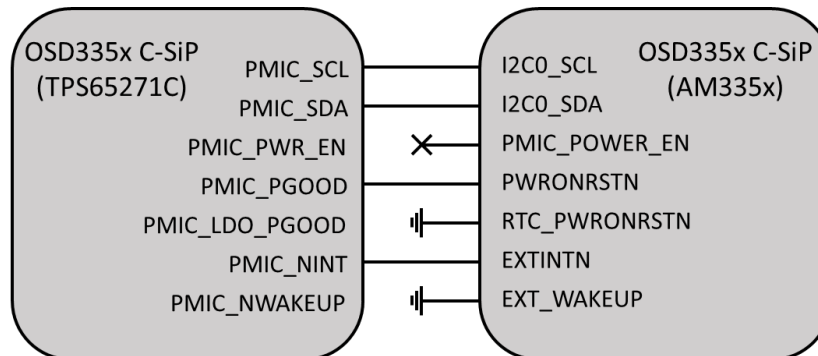


Figure 7-1 - OSD335x C-SiP Minimum Signal Connections with RTC disabled



When the RTC is enabled and the RTC-only power mode does not need to be supported, the following signal connections should be used:

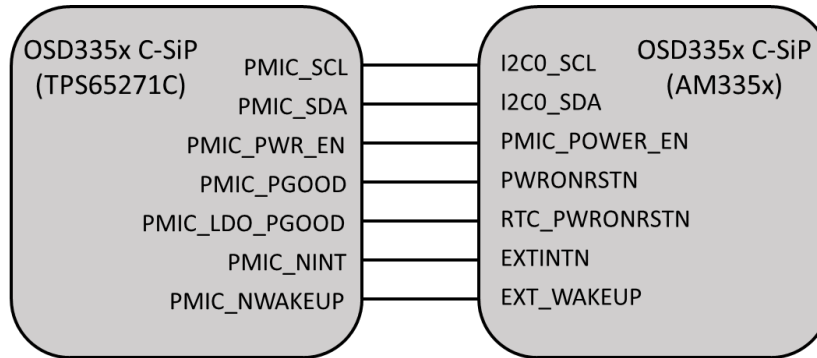


Figure 7-2 - OSD335x C-SiP Minimum Signal Connections with RTC enabled

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## 7.5.4 Minimum RTC Power Connections

Table 7-3 lists RTC power domain signals required to operate the OSD335x C-SiP. In addition to the required connections described in Section 7.5.3, Figure 7-4, Figure 7-5, and Figure 7-5 illustrate power connections with RTC subsystem enabled and disabled. These connections are also included in the minimum required circuitry to operate the device.

Table 7-3. OSD335x C-SiP RTC Signal Descriptions

Signal	Description	Notes
<b>CAP_VDD_RTC</b>	Supply voltage for the RTC core domain	
<b>RTC_KALDO_ENN</b>	Active low enable input for internal CAP_VDD_RTC voltage regulator	
<b>RTC_PWRONRSTN</b>	RTC_PWRONRSTN to AM335x	2
<b>PMIC_POWER_EN</b>	PMIC Power Enable from AM335x	
<b>EXT_WAKEUP</b>	EXT_WAKEUP to AM335x	1
<b>VDDS_RTC</b>	Supply for RTC power domain	
<b>VDDS</b>	Supply for 1.8V IO voltage domain	2

1. See Table 2-2 for pull up on this signal
2. RTC\_PWRONRSTN must be pulled up by the same power source as VDDS\_RTC when being powered externally.

When the RTC is disabled, the following connections should be used for the internal LDO:

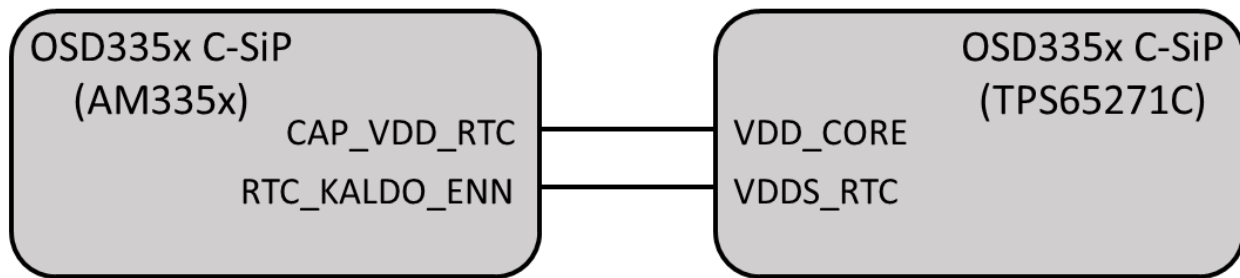


Figure 7-3 - Additional connections for OSD335x C-SiP with RTC disabled

When the RTC is enabled, the following connections should be used for the internal LDO:

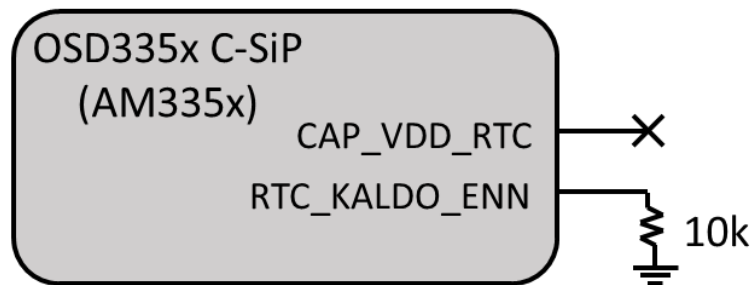
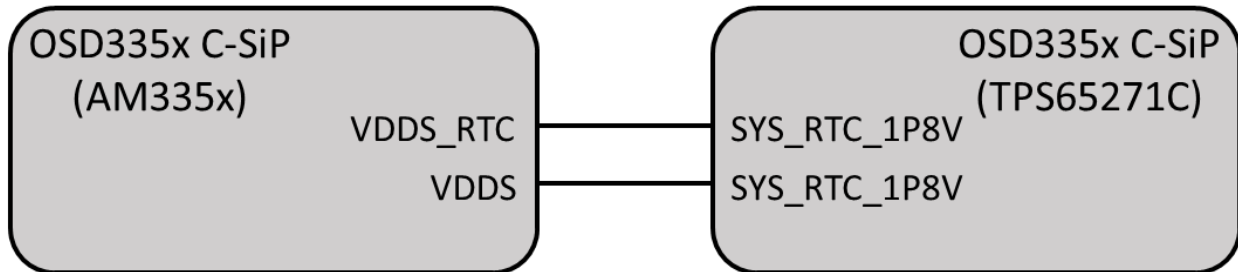


Figure 7-4 - Additional connections for OSD335x C-SiP with RTC enabled

When the RTC is disabled or the RTC is enabled and the RTC-only power mode does not need to be supported, the following connections should be used:



*Figure 7-5 - VDDS\_RTC and VDDS Power Connections for RTC-only Power Mode Disabled*

## 8 Electrical & Thermal Characteristics

Table 8.1 lists electrical and thermal characteristic parameters of OSD335x C-SiP.

Table 8-1. OSD335x C-SiP Absolute Maximum Ratings over operating free-air temperature range (unless noted) <sup>(1) (2)</sup>

		Value	Unit
Supply voltage range (with respect to VSS)	VIN_BAT	-0.3 to 7	V
	VIN_USB, VIN_AC	-0.3 to 7	
Input/Output voltage range (with respect to VSS)	All pins unless specified separately	-0.3 to 3.6	V
Terminal current	SYS_VOUT, VIN_USB, VIN_BAT	3000	mA
T <sub>c</sub> Operating case temperature	Commercial (B)	0 to 85	°C
	Industrial (I)	-40 to 85	°C
T <sub>stg</sub> Storage temperature		-40 to 125	°C
ESD rating	(HBM) Human body model	±2000	V
	(CDM) Charged device model	±500	

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

Table 8-2. Recommended Operating Conditions over operating free-air temperature range (unless otherwise noted)

	Min	Nom	Max	Unit
Supply voltage, VIN_USB, VIN_AC	4.3		5.8	V
Supply voltage, VIN_BAT	3.5		5.5	V
Input current from VIN_AC			2.0	A
Input current from VIN_USB			1.3	A
VIN_BAT current			2.0	A
Output voltage range for SYS_VDD1_3P3V		3.25		V
Output voltage range for SYS_VDD2_3P3V		3.3		V
Output voltage range for SYS_VDD3_3P3V		3.3		V
Output voltage range for SYS_RTC_1P8V		1.8		V
Output voltage range for SYS_VDD_1P8V		1.8		V
Output voltage range for SYS_ADC_1P8V		1.8		V
Output voltage range for VDDS_DDR <sup>1</sup>		1.5		V
Output voltage range for VDD_MPU <sup>1</sup>		1.1		V
Output voltage range for VDD_CORE <sup>1</sup>		1.1		V
Output voltage range for VDDS_PLL <sup>1</sup>		1.8		V
Output current for SYS_VOUT <sup>2</sup>	0		500	mA
Output current for SYS_VDD1_3P3V <sup>2,3</sup>	0		300	mA
Output current for SYS_VDD2_3P3V <sup>2</sup>	0		100	mA
Output current for SYS_VDD3_3P3V <sup>2</sup>	0		50	mA
Output current for SYS_RTC_1P8V <sup>2</sup>	0		100	mA
Output current for SYS_VDD_1P8V <sup>2</sup>	0		250	mA
Output current for SYS_ADC_1P8V <sup>2</sup>	0		25	mA

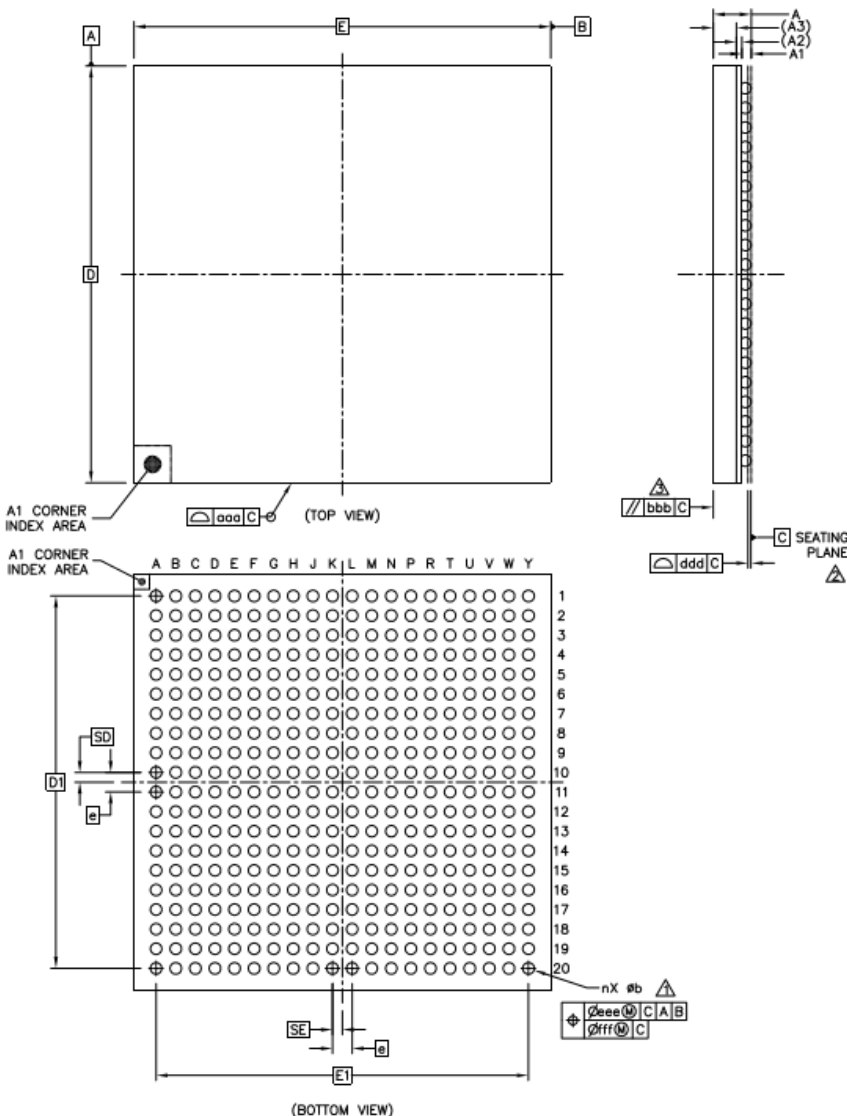
- (1) These voltage rails are for reference only and should not be used to power anything on the PCB.
- (2) Please note that the total input current on VIN\_AC, VIN\_USB or VIN\_BAT must not exceed the recommended maximum value even if individual currents drawn from these power supply outputs are less than or equal to the maximum recommended operating output currents. See section 7.4 for more details.
- (3) Maximum current assumes that eMMC (EMMC\_VCC and EMMC\_VCCQ) are connected to SYS\_VDD1\_3P3V.

## 9 Packaging Information

The OSD335x C-SiP is packaged in a 400 ball, Ball Grid Array (BGA). The package size is 27 X 27 millimeters with a ball pitch of 1.27 millimeters. This section will give you the specifics on the package.

### 9.1 Mechanical Dimensions

The mechanical drawings of the OSD335x C-SiP show pin A1 in the lower left-hand corner when looking at the top view of the device. Pin A1 is in the upper left-hand corner if looking at the balls from the bottom view of the package. The PCB layout should have pin A1 in the lower left-hand corner when looking at the top side of the PCB where the OSD335x C-SiP will be attached.



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	2.6
STAND OFF	A1	0.5	---	0.7
SUBSTRATE THICKNESS	A2	0.35		REF
MOLD THICKNESS	A3	1.5		REF
BODY SIZE	D	27		BSC
	E	27		BSC
BALL DIAMETER		0.75		
BALL OPENING		0.6		
BALL WIDTH	b	0.6	---	0.9
BALL PITCH	e	1.27		BSC
BALL COUNT	n	400		
EDGE BALL CENTER TO CENTER	D1	24.13		BSC
	E1	24.13		BSC
BODY CENTER TO CONTACT BALL	SD	0.635		BSC
	SE	0.635		BSC
PACKAGE EDGE TOLERANCE	aaa	0.2		
MOLD FLATNESS	bbb	0.35		
COPLANARITY	ddd	0.2		
BALL OFFSET (PACKAGE)	eee	0.3		
BALL OFFSET (BALL)	fff	0.15		

NOTES:

- ▲ DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
- ▲ DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- ▲ PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

## 9.2 Reflow Instructions

The reflow profile for this package should be in accordance with the Lead-free process for BGA. A peak reflow temperature is recommended to be 245°C.

Texas Instruments provides a good overview of Handling & Process Recommendations in AN-2029 for this type of device. A link to the document can be found in the Reference Documents section of this document.

## 9.3 Storage Recommendations

The OSD335x Family of devices are sensitive to moisture and need to be handled in specific ways to make sure they function properly during and after the manufacturing process. The OSD335x Family of devices are rated with a Moisture Sensitivity Level (MSL) of 4. This means that they are typically stored in a sealed Dry Pack.



Once the sealed Dry Pack is opened the OSD335x needs to be used within 72 hours to avoid further processing. If the OSD335x has been exposed for more than 72 hours, then it is required that you bake the device for 34 hours at 125°C before using.

Alternatively, the devices could be stored in a dry cabinet with humidity <10% to avoid the baking requirement.

For more information, please refer to the Texas Instruments AN-2029 which can be found in the Reference Documents section of this document.