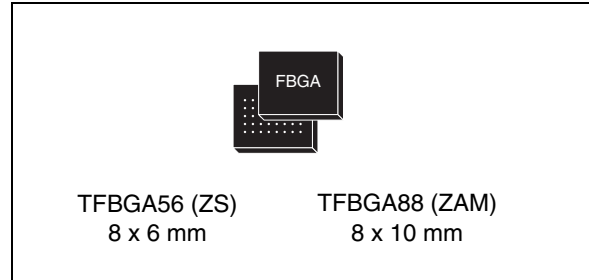


Features

- Multichip package
 - 1 die of 128 Mbits (8 Mbits x16) or 256 Mbits (16 Mbits x16), mux I/O multiple bank, multilevel, burst flash memory
 - 1 die of 32 or 64 Mbits mux I/O, burst PSRAM
- Supply voltage
 - $V_{DDF} = V_{DDP} = V_{DDQF} = 1.7$ to 1.95 V
 - $V_{PPF} = 9$ V for fast program
- Electronic signature
 - Manufacturer code: 20h
 - Device codes (top flash configuration):
M36L0R7050U3/M36L0R7060U3: 882Eh
M36L0R8050U3/M36L0R8060U3: 881Ch
 - Device codes (bottom flash configuration):
M36L0R7050L3/M36L0R7060L3: 882Fh
M36L0R8050L3/M36L0R8060L3: 881Dh

Flash memory

- Synchronous/asynchronous read
 - Synchronous burst read mode: 66 MHz
 - Random access: 70 ns
- Programming time
 - 2.5 μ s typical word program time using buffer enhanced factory program command
- Memory organization
 - Multiple bank memory array: 8-Mbit banks
 - Parameter blocks (top or bottom location)
- Dual operations
 - Program/erase in one bank, read in others
- Block locking
 - All blocks locked at power-up
 - Any combination of blocks can be locked with zero latency
 - $\overline{WP}_F$ for block lock-down
 - Absolute write protection with $V_{PPF} = V_{SS}$



- Security
 - 64-bit unique device number
 - 2112-bit user programmable OTP cells
- Common flash interface (CFI)
- 100,000 program/erase cycles per block

PSRAM

- Access time: 70 ns
- Synchronous modes:
 - Synchronous write: continuous burst
 - Synchronous read: continuous burst or fixed length: 4, 8 or 16 words for 32-Mbit devices; 4, 8, 16 or 32 words for 64-Mbit devices
 - Maximum clock frequency: 83 MHz
- Low-power features
 - Partial array self-refresh (PASR)
 - Deep power-down (DPD) mode
 - Automatic temperature-compensated self-refresh

Table 1. Device summary

M36L0Rx0x0UL3	
M36L0R7050U3	M36L0R7050L3
M36L0R7060U3	M36L0R7060L3
M36L0R8050U3	M36L0R8050L3
M36L0R8060U3	M36L0R8060L3

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1 Description

The M36L0R7050U3, M36L0R7050L3, M36L0R7060U3, M36L0R7060L3, M36L0R8050U3, M36L0R8050L3, M36L0R8060U3, and M36L0R8060L3 combine two memory devices in a multichip package:

- a 128 or 256 Mbit, multiple bank flash memory, the M58LRxxxKCD
- a 32 or 64 Mbit PSRAM, the M69KM048AA or M69KM096AA, respectively.

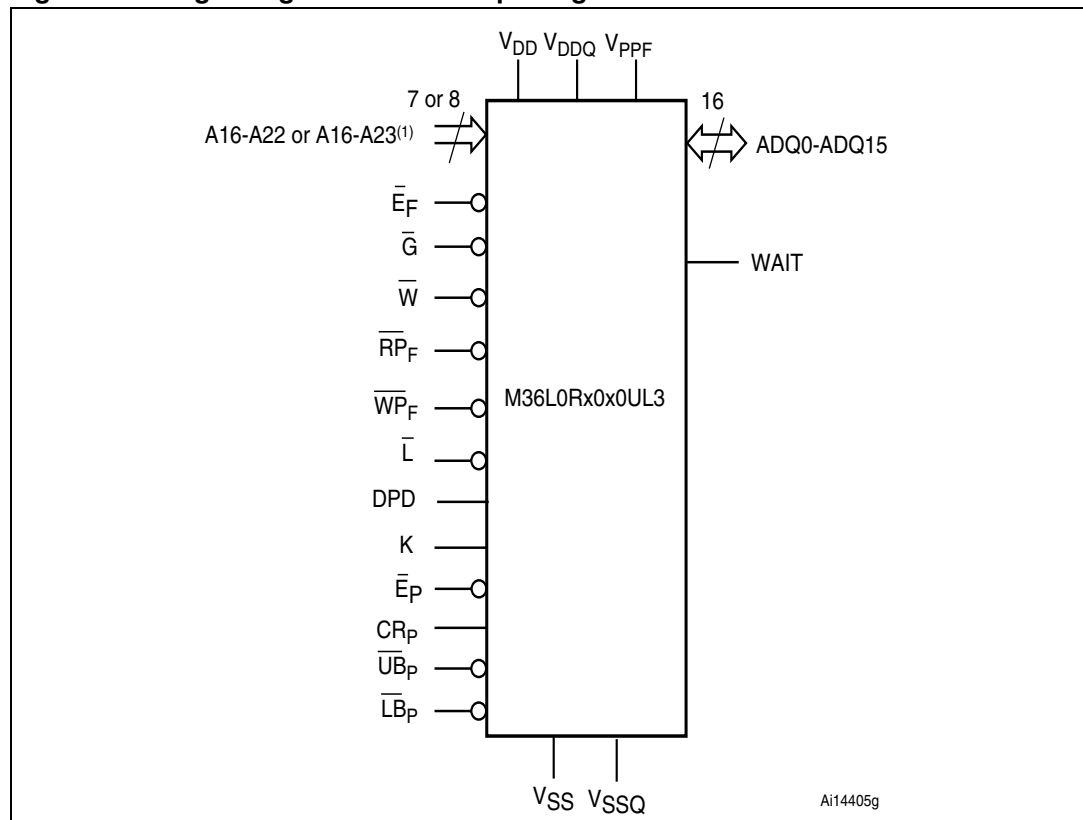
Collectively, this family of devices is referred to as the M36L0Rx0x0UL3.

The purpose of this document is to describe how the two memory components operate with respect to each other. It must be read in conjunction with the M58LRxxxKCD and M69KM048AA or M69KM096AA datasheets, where all specifications required to operate the flash memory and PSRAM components are fully detailed. These datasheets are available from your local Numonyx distributor.

Recommended operating conditions do not allow more than one memory to be active at the same time.

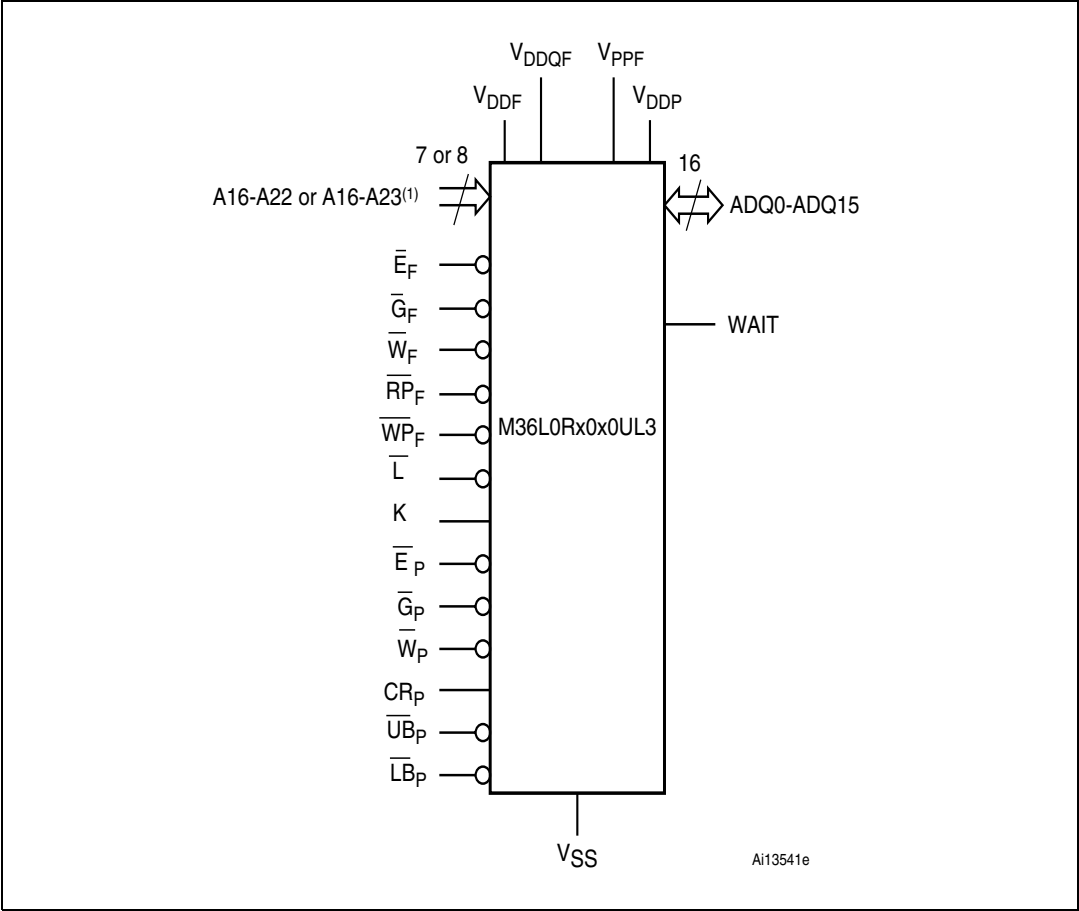
The memory is offered in either the stacked TFBGA56 (8 x 6 mm, 8 x 6 ball array, 0.5 mm pitch) or the stacked TFBGA88 (8 x 10 mm, 8 x 10 ball array, 0.8 mm pitch) package.

Figure 1. Logic diagram - TFBGA56 package



1. A16-A22 for the M36L0R7050UL3 and M36L0R7060UL3, and A16-A23 for the M36L0R8050UL3 and M36L0R8060UL3.

Figure 2. Logic diagram - TFBGA88 package



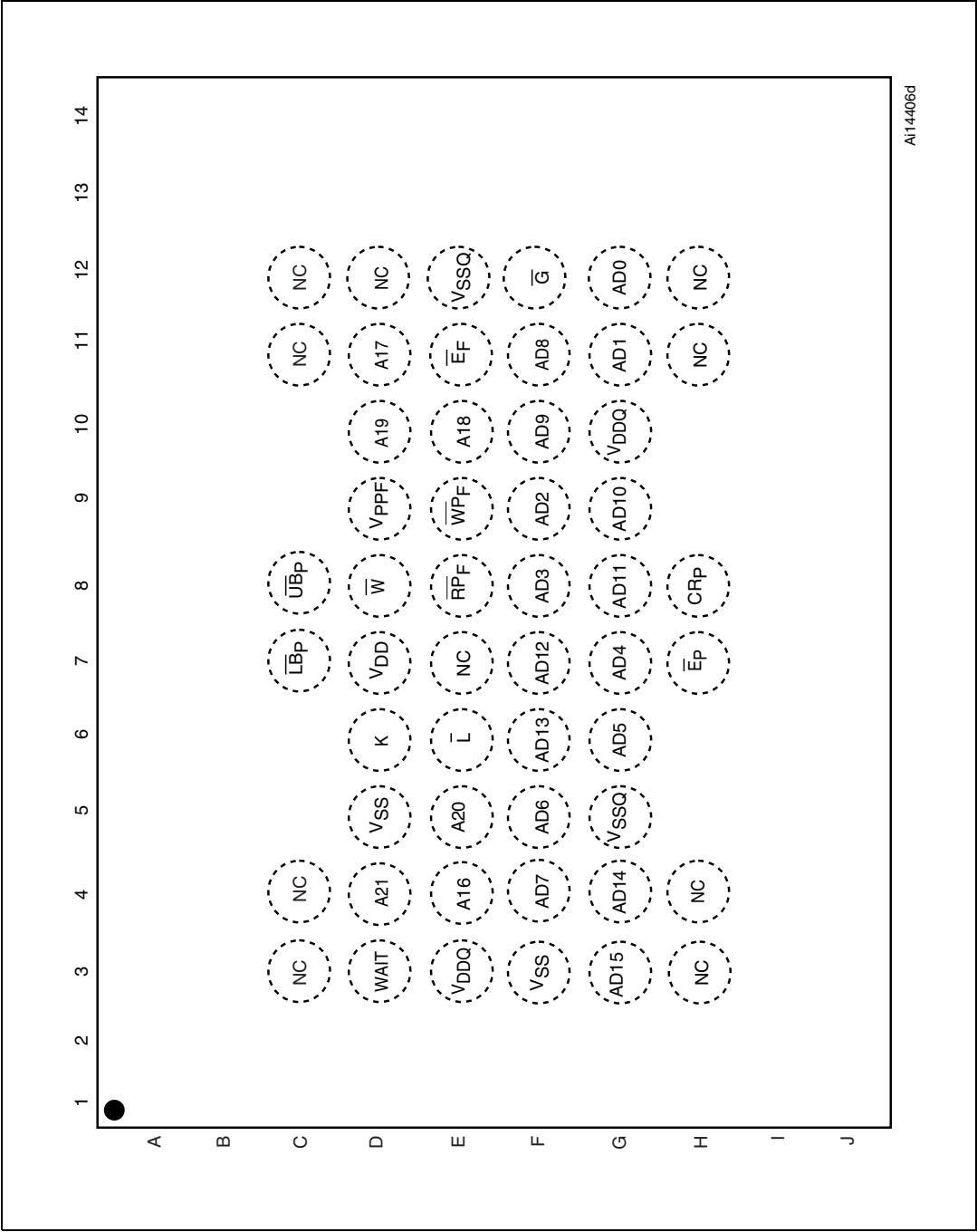
1. A16-A22 for the M36L0R7050UL3 and M36L0R7060UL3, and A16-A23 for the M36L0R8050UL3 and M36L0R8060UL3.

Table 2. Signal names

Name	Function	Direction
Common to both packages		
A16-A23 ⁽¹⁾	Address inputs	Inputs
ADQ0-ADQ15	Flash memory and PSRAM common data input/outputs, address inputs or command inputs	Inputs/outputs
$\overline{L}$	Flash memory and PSRAM Latch Enable input	Input
K	Flash memory and PSRAM Burst Clock	Input
WAIT	Flash memory and PSRAM Wait Data in burst mode	Output
$\overline{E}_F$	Flash memory Chip Enable input	Input
$\overline{WP}_F$	Flash memory Write Protect input	Input
$\overline{RP}_F$	Flash memory Reset input	Input
$\overline{E}_P$	PSRAM Chip Enable input	Input
$\overline{UB}_P$	PSRAM Upper Byte Enable input	Input
$\overline{LB}_P$	PSRAM Lower Byte Enable input	Input
CR _P	PSRAM Configuration Register Enable input	Input
V _{PPF}	Flash memory optional supply voltage for fast program and erase	Power supply
V _{SS}	Flash memory and PSRAM shared ground	Ground
V _{SSQ}	Flash memory and PSRAM shared ground.	Ground
NC	Not connected internally	
Only in TFBGA56 package		
DPD	Deep power-down	Input
$\overline{G}$	Flash memory and PSRAM Output Enable input	Input
$\overline{W}$	Flash memory and PSRAM Write Enable input	Input
V _{DD}	Flash memory and PSRAM shared power supply	Power supply
V _{DDQ}	Flash memory and PSRAM shared power supply for I/O buffers	Power supply
Only in TFBGA88 package		
$\overline{G}_F$	Flash memory Output Enable input	Input
$\overline{W}_F$	Flash memory Write Enable input	Input
$\overline{G}_P$	PSRAM Output Enable input	Input
$\overline{W}_P$	PSRAM Write Enable input	Input
V _{DDF}	Flash memory power supply	Power supply
V _{CCP}	PSRAM supply voltage is the core supply voltage.	Power supply

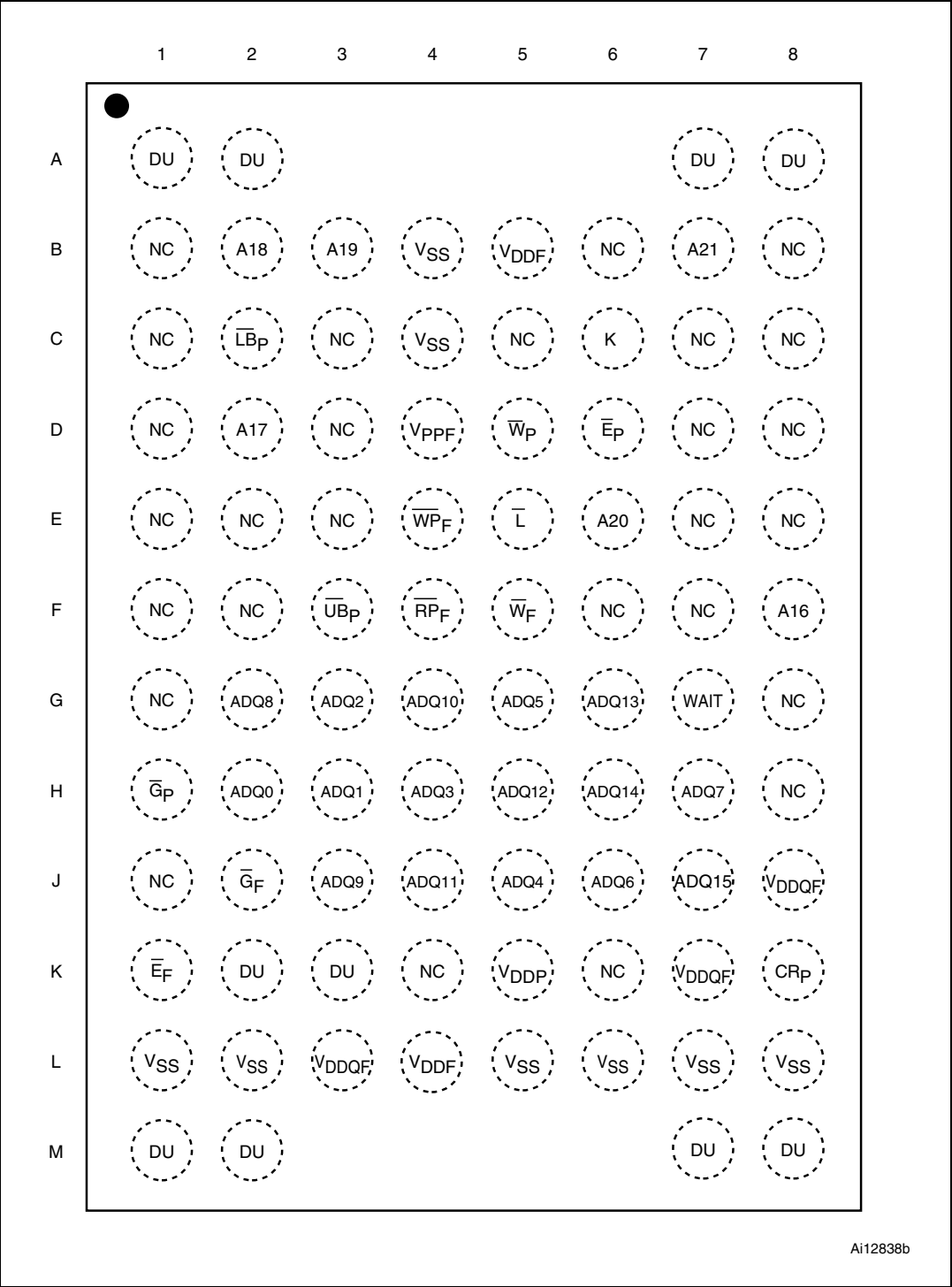
1. In the TFBGA56 package, address inputs A16-A18 in the PSRAM are used in conjunction with ADQ0 to ADQ15 to select the cells in the memory array that are accessed during read and write operations. However, in the TFBGA88 package, it is address inputs A16-A19.

Figure 3. TFBGA56 package connections (top view through package)



AI14406d

Figure 4. TFBGA88 package connections (top view through package)



2 Signal descriptions

See [Figure 1: Logic diagram - TFBGA56 package](#) and [Table 2: Signal names](#) for a brief overview of the signals connected to this device.

2.1 Signals common to both packages

2.1.1 Address inputs (ADQ0-ADQ15 and A16-A23)

ADQ0-ADQ15 and A16-A20 (for the M36L0R7050UL3 and M36L0R8050UL3) or A16-A21 (for the M36L0R7060UL3 and M36L0R8060UL3) are common to the flash memory and PSRAM components.

In the flash memory, the address inputs select the cells in the array to access during bus read operations. During bus write operations they control the commands sent to the command interface of the program/erase controller.

In the PSRAM, the address inputs A16-A20 (/A21) are used in conjunction with ADQ0 to ADQ15 to select the cells in the memory array that are accessed during read and write operations.

2.1.2 Data inputs/outputs (ADQ0-ADQ15)

The data inputs/outputs output the data stored at the selected address during a bus read operation or input a command or the data to be programmed during a bus write operation.

2.1.3 Latch Enable ($\bar{L}$)

The Latch Enable input is common to the flash memory and PSRAM components.

For details of how the Latch Enable signal behaves, please refer to the datasheets of the respective memory components: M69KM048AA or M69KM096AA for the PSRAM and M58LRxxxKCD for the flash memory.

2.1.4 Clock (K)

The Clock input is common to the flash memory and PSRAM components.

For details of how the Clock signal behaves, please refer to the datasheets of the respective memory components: M69KM048AA or M69KM096AA for the PSRAM and M58LRxxxKCD for the flash memory.

2.1.5 Wait (WAIT)

The Wait output is common to the flash memory and PSRAM components.

For details of how the WAIT signal behaves, please refer to the datasheets of the respective memory components: M69KM048AA or M69KM096AA for the PSRAM and M58LRxxxKCD for the flash memory.

2.1.6 Flash memory Chip Enable ($\overline{E}_F$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at V_{IL} and Reset is at V_{IH} the device is in active mode. When Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance, and the power consumption is reduced to the standby level.

It is not allowed to set both $\overline{E}_F$ and $\overline{E}_P$ to V_{IL} at the same time.

2.1.7 Flash memory Write Protect ($\overline{WP}_F$)

Write Protect is an input that provides additional hardware protection for each block. When Write Protect is at V_{IL} , the lock-down is enabled and the protection status of the locked-down blocks cannot be changed. When Write Protect is at V_{IH} , the lock-down is disabled and the locked-down blocks can be locked or unlocked (refer to the M58LRxxxKCD datasheet).

2.1.8 Flash memory Reset ($\overline{RP}_F$)

The Reset input provides a hardware reset of the memory. When Reset is at V_{IL} , the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the reset supply current I_{DD2} . Refer to the M58LRxxxKCD datasheet for the value of I_{DD2} . After Reset all blocks are in the locked state and the Configuration Register is reset. When Reset is at V_{IH} the device is in normal operation. Exiting reset mode the device enters asynchronous read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3 V logic without any additional circuitry. It can be tied to V_{RPH} (refer to the M58LRxxxKCD datasheet).

2.1.9 PSRAM Chip Enable ($\overline{E}_P$)

Chip Enable, $\overline{E}_P$ activates the device when driven Low (asserted). When de-asserted (V_{IH}), the device is disabled and goes automatically in low-power standby mode or deep power-down mode, according to the Refresh Configuration Register (RCR) settings.

It is not allowed to set both $\overline{E}_F$ and $\overline{E}_P$ to V_{IL} at the same time.

2.1.10 PSRAM Upper Byte Enable ($\overline{UB}_P$)

The Upper Byte Enable, $\overline{UB}_P$ gates the data on the upper byte of the address inputs/data inputs/outputs (ADQ8-ADQ15) to or from the upper part of the selected address during a write or read operation.

2.1.11 PSRAM Lower Byte Enable ($\overline{LB}_P$)

The Lower Byte Enable, $\overline{LB}_P$ gates the data on the lower byte of the address inputs/data input/outputs (ADQ0-ADQ7) to or from the lower part of the selected address during a write or read operation.

If both $\overline{LB}_P$ and $\overline{UB}_P$ are disabled (High), the device disables the data bus from receiving or transmitting data. Although the device seems to be deselected, it remains in an active mode as long as $\overline{E}_P$ remains Low.

2.1.12 PSRAM Configuration Register Enable (CR_P)

When this signal is driven High, V_{IH} , bus read or write operations access either the value of the RCR or the Bus Configuration Register (BCR) according to the value of A19.

2.1.13 V_{PPF} flash memory program supply voltage

V_{PPF} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0 V to V_{DDQF}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PP_{LK}} gives absolute protection against program or erase, while V_{PPF} in the V_{PP1} range enables these functions (see the M58LRxxxKCD datasheet for the relevant values). V_{PPF} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PPF} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PPF} must be stable until the program/erase algorithm is completed.

2.1.14 V_{SS} ground

V_{SS} ground is the common flash memory and PSRAM ground. It is the reference for the core supplies. It must be connected to the system ground.

2.1.15 V_{SSQ} ground

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQF}. V_{SSQ} must be connected to V_{SS}.

Note: Each device in a system should have V_{DDF}, V_{DDQF} and V_{PP} decoupled with a 0.1 μF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See [Figure 8: AC measurement load circuit](#). The PCB track widths should be sufficient to carry the required V_{PP} program and erase currents.

2.2 Signals only in TFBGA56 package

2.2.1 Deep power-down (DPD)

The deep power-down input puts the device in deep power-down mode. When the device is in standby mode and the Enhanced Configuration Register bit ECR15 is set, asserting the deep power-down input causes the memory to enter deep power-down mode.

When the device is in deep power-down mode, the memory cannot be modified and the data is protected.

The polarity of the DPD pin is determined by ECR14. The deep power-down input is active Low by default.

2.2.2 Output Enable ($\overline{G}$)

The Output Enable input is common to the Flash memory and PSRAM components. For details on the Output Enable signal, please refer to the datasheets of the respective memory components: M69KM024A or M69KM048AB for the PSRAM and M58WR0xxKUL for the Flash memory.

2.2.3 Write Enable ($\overline{W}$)

The Write Enable Input is common to the Flash memory and PSRAM components. For details on the Write Enable signal, please refer to the datasheets of the respective memory components: M69KM024A or M69KM048AB for the PSRAM and M58WR0xxKUL for the Flash memory.

2.2.4 V_{DD} supply voltage

V_{DD} is common to both Flash memory and PSRAM components and provides the power supply to the internal core. It is the main power supply for all memory operations (read, program, and erase).

2.2.5 V_{DDQ} supply voltage

V_{DDQ} is common to both Flash memory and PSRAM components and provides the power supply to the I/O pins. It enables all outputs to be powered independently of V_{DD} . V_{DDQ} can be tied to V_{DD} or use a separate supply.

2.3 Signals only in TFBGA88 package

2.3.1 Flash memory Output Enable ($\overline{G}_F$)

The Output Enable input controls data outputs during the bus read operation of the flash memory.

2.3.2 Flash memory Write Enable ($\overline{W}_F$)

The Write Enable input controls the bus write operation of the flash memory's command interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable, whichever occurs first.

2.3.3 PSRAM Output Enable ($\overline{G}_P$)

When held Low, V_{IL} , the Output Enable, $\overline{G}_P$ enables the bus read operations of the memory.

2.3.4 PSRAM Write Enable ($\overline{W}_P$)

Write Enable, $\overline{W}_P$ controls the bus write operation of the memory. When asserted (V_{IL}), the device is in write mode and write operations can be performed either to the configuration registers or to the memory array.

2.3.5 V_{DDF} flash memory supply voltage

V_{DDF} provides the power supply to the internal core of the flash memory. It is the main power supply for all flash memory operations (read, program and erase).

2.3.6 V_{CCP} PSRAM supply voltage

The V_{CCP} supply voltage is the core supply voltage.

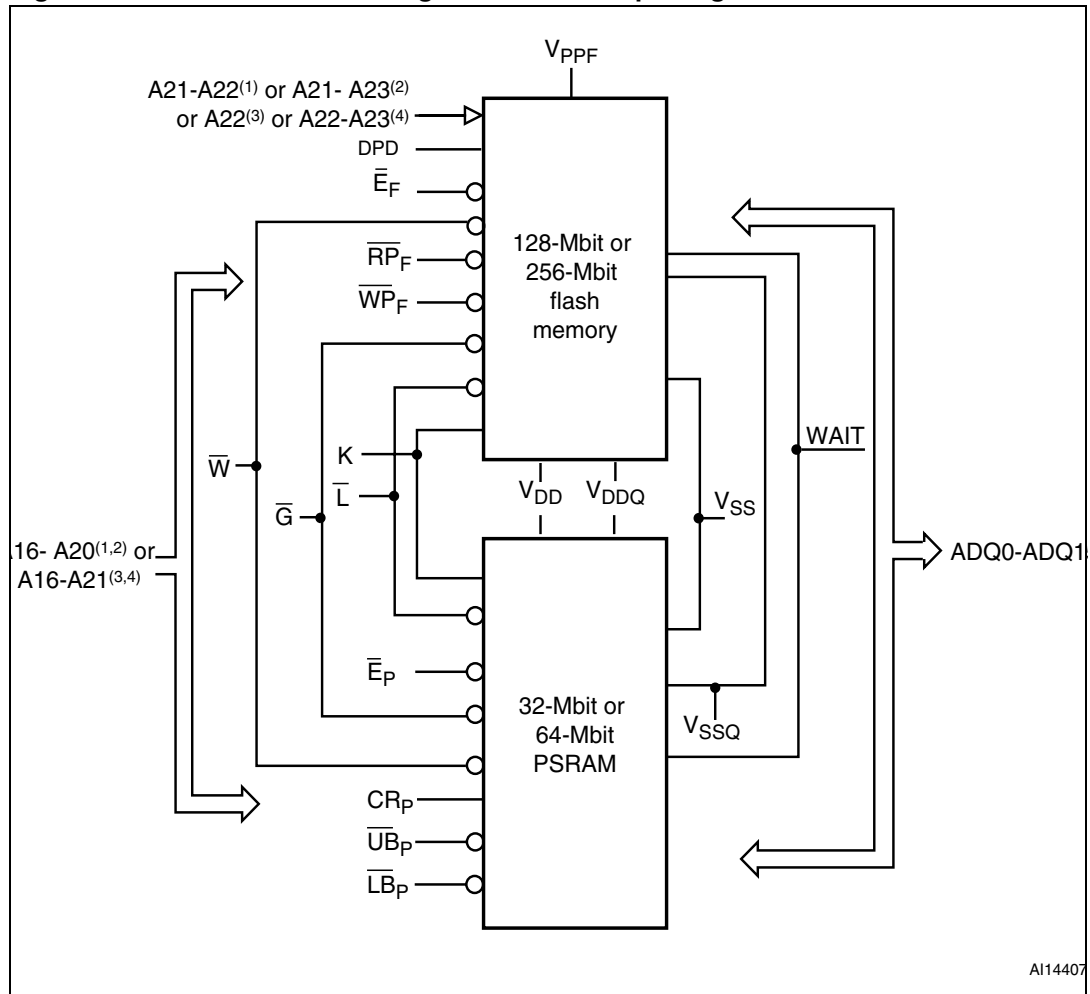
3 Functional description

The PSRAM and flash memory components have separate power supplies but share the same grounds. They are distinguished by two Chip Enable inputs: $\bar{E}_F$ for the flash memory and $\bar{E}_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is simultaneous read operations on one of the flash memory and the PSRAM components which would result in a data bus contention.

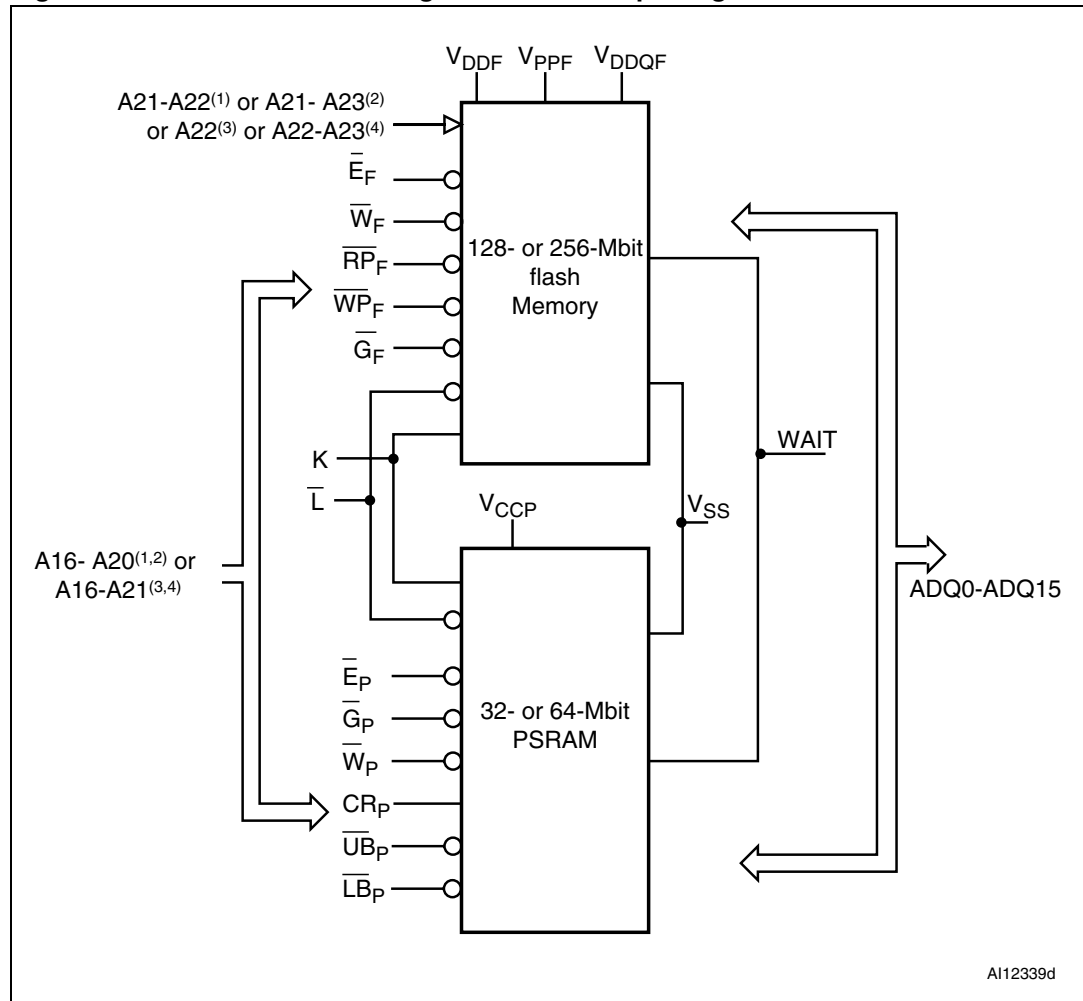
Therefore, it is recommended to put the other devices in the high impedance state when reading the selected device.

Figure 5. Functional block diagram - TFBGA56 package



1. Address inputs corresponding to the M36L0R7050UL3 devices.
2. Address inputs corresponding to the M36L0R8050UL3 devices.
3. Address input corresponding to the M36L0R7060UL3 devices.
4. Address input corresponding to the M36L0R8060UL3 devices.

Figure 6. Functional block diagram - TFBGA88 package



1. Address inputs corresponding to the M36L0R7050UL3 devices.
2. Address inputs corresponding to the M36L0R8050UL3 devices.
3. Address input corresponding to the M36L0R7060UL3 devices.
4. Address input corresponding to the M36L0R8060UL3 devices.

Table 3. TFBGA56 package operating modes - standard asynchronous operation

Operation ⁽¹⁾⁽²⁾		$\overline{E}_F$	$\overline{R}P_F$	WAIT ⁽³⁾	$\overline{G}$	$\overline{W}$	$\overline{L}$	$\overline{U}B_P$	$\overline{L}B_P$	CR_P	$\overline{E}_P$	ADQ0-ADQ7	ADQ8-ADQ15
Flash memory	Bus read	V_{IL}	V_{IH}		V_{IL}	V_{IH}	V_{IH}	Any PSRAM mode is allowed.				Data output	
	Bus write	V_{IL}	V_{IH}		V_{IH}	V_{IL}	V_{IH}					Data input	
	Address latch	V_{IL}	V_{IH}		V_{IH}	X	V_{IL}					Data output or Hi-Z ⁽⁴⁾	
	Output disable	V_{IL}	V_{IH}		V_{IH}	V_{IH}	V_{IH}	Any PSRAM mode is allowed.				Hi-Z	
	Standby	V_{IH}	V_{IH}	Hi-Z	X	X	X					Hi-Z	
	Reset	X	V_{IL}	Hi-Z	X	X	X					Hi-Z	
PSRAM	Word read	The Flash memory must be disabled.			V_{IL}	V_{IH}		V_{IL}	V_{IL}	V_{IL}	V_{IL}	Address in/ data out valid	
	Word write				V_{IH}	V_{IL}		V_{IL}	V_{IL}	V_{IL}		Address in/ data in valid	
	Output disable/no operation	Any Flash memory mode is allowed.			V_{IH}	V_{IH}	X	X	X	V_{IL}		High-Z	
	Deep power-down ⁽⁵⁾				X	X	X	X	X	X	V_{IH}	High-Z	
	Standby				X	X	X	X	X	X	V_{IH}	High-Z	

1. The Clock signal, K, must remain Low when the PSRAM is operating in asynchronous mode.
2. X = 'don't care'
3. In the Flash memory the WAIT signal polarity is configured using the Set Configuration Register command.
4. See the M58WR0xxKUL datasheet.
5. The device enters deep power-down mode by driving the Chip Enable signal $\overline{E}_P$ from Low to High, with bit 4 of the RCR set to "0". The device remains in deep power-down mode until $\overline{E}_P$ goes Low again and is held Low for $t_{ELEH(DP)}$.

Table 4. TFBGA88 package operating modes - standard asynchronous operation

Operation ⁽¹⁾⁽²⁾		$\overline{E}_F$	$\overline{G}_F$	$\overline{W}_F$	$\overline{R}_P$	WAIT ⁽³⁾	$\overline{L}$	$\overline{E}_P$	$\overline{W}_P$	$\overline{G}_P$	$\overline{U}_P$	$\overline{L}_P$	CR _P	A19	A18	Other Address inputs	ADQ0-ADQ7	ADQ8-ADQ15
Flash memory	Bus Read	V _{IL}	V _{IL}	V _{IH}	V _{IH}		V _{IH}	The PSRAM must be disabled.									Data output	
	Bus Write	V _{IL}	V _{IH}	V _{IL}	V _{IH}		V _{IH}										Data input	
	Address Latch	V _{IL}	V _{IH}	X	V _{IH}		V _{IL}										Address input	
	Output Disable	V _{IL}	V _{IH}	V _{IH}	V _{IH}		V _{IH}	Any PSRAM mode is allowed.									Hi-Z	
	Standby	V _{IH}	X	X	V _{IH}	Hi-Z	X										Hi-Z	
	Reset	X	X	X	V _{IL}	Hi-Z	X										Hi-Z	
PSRAM	Word Read	The flash memory must be disabled.						V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IL}	Address In Valid		Address In/ Data Out Valid			
	Word Write							V _{IL}	V _{IH}	V _{IL}	V _{IL}	V _{IL}	Address In Valid		Address In/ Data In Valid			
	Read Configuration Register (CR controlled method) ⁽⁴⁾							V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IH}	00(RCR) 10(BCR) X1(DIDR)	X	Address In/ BCR, RCR or DIDR Content Valid			
	Program Configuration Register (CR controlled) ⁽⁵⁾						V _{IL}	V _{IH}	X	X	00(RCR) 10(BCR) ⁽⁶⁾		BCR/ RCR Data	Address In Valid				
	Output Disable/No operation	Any flash memory mode is allowed.					X	V _{IH}	X	X	X	V _{IL}	X	X	X	High-Z		
	Deep Power-down ⁽⁷⁾							V _{IH}	X	X	X	X	X	X	X	High-Z		
	Standby							V _{IH}	X	X	X	X	X	V _{IL}	X	X	High-Z	

1. The Clock signal, K, must remain Low when the PSRAM is operating in asynchronous mode.
2. X = 'don't care'
3. In the flash memory the WAIT signal polarity is configured using the Set Configuration Register command.
4. Operating mode available in the M36L0R7060UL3 and M36L0R8050UL3 only (see the M69KM096AA datasheet).
5. BCR and RCR only.
6. A18 and A19 are used to select the BCR, the RCR or the DIDR.
7. The device enters Deep Power-down mode by driving the Chip Enable signal, $\overline{E}$, from Low to High, with bit 4 of the RCR set to '0'. The device remains in Deep Power-down mode until $\overline{E}$ goes Low again and is held Low for $t_{LEH(DP)}$.

4 Maximum ratings

Stressing the device above the rating listed in [Table 5: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient operating temperature	-25	85	°C
T_{BIAS}	Temperature under bias	-25	85	°C
T_{STG}	Storage temperature	-55	125	°C
V_{IO}	Input or output voltage	-0.2	2.45	V
V_{DDF} V_{DDQF} V_{CCP}	Core and input/output supply voltages	-0.2	2.45	V
V_{PPF}	Flash program voltage	-0.2	10	V
I_O	Output short circuit current		100	mA
t_{VPPFH}	Time for V_{PPF} at V_{PPFH}		100	hours

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables are derived from tests performed under the measurement conditions summarized in [Table 6: Operating and AC measurement conditions](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 6. Operating and AC measurement conditions

Parameter	Flash memory		PSRAM		Unit
	Min	Max	Min	Max	
V_{DD} supply voltage	1.7	1.95	–	–	V
V_{DDQ} supply voltage	1.7	1.95	–	–	V
V_{PPF} supply voltage (factory environment)	8.5	9.5	–	–	V
V_{PPF} supply voltage (application environment)	–0.4	$V_{DDQ} + 0.4$	–	–	V
Ambient operating temperature	–25	85	–25	85	°C
Load capacitance (C_L)	30		30		pF
Output circuit resistors (R_1, R_2)	16.7		16.7		k Ω
Input rise and fall times		5		2	ns
Input pulse voltages	0 to V_{DDQ}		0 to $V_{DD}/2$		V
Input and output timing ref. voltages	$V_{DDQ}/2$		$V_{DD}/2$		V

Figure 7. AC measurement I/O waveform

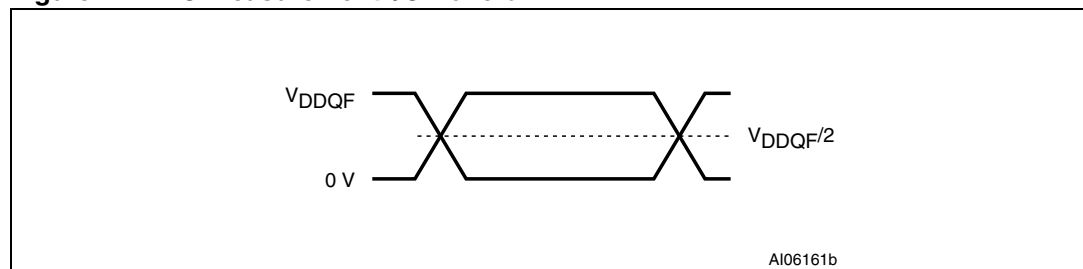


Figure 8. AC measurement load circuit

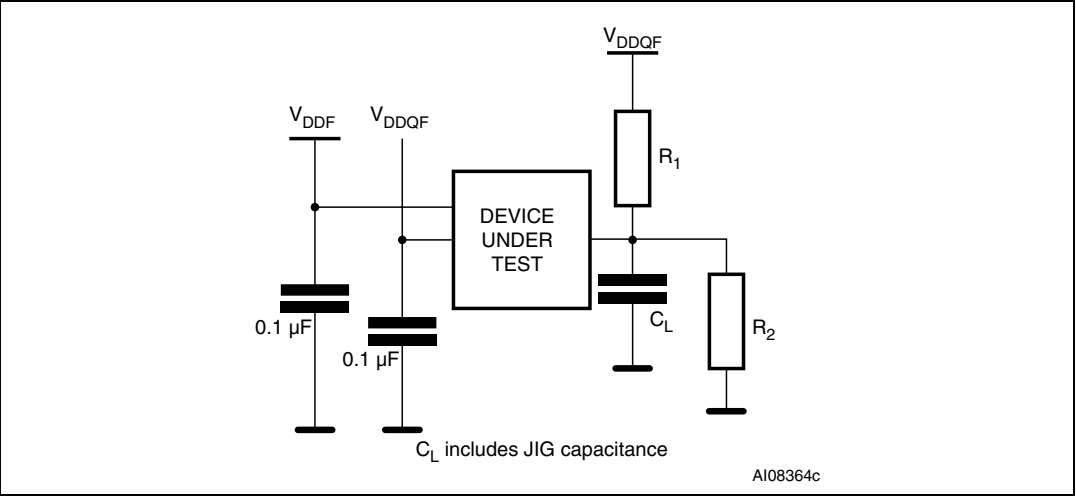


Table 7. Device capacitance

Symbol	Parameter	Test Condition	Min	Max ⁽¹⁾	Unit
C_{IN}	Input capacitance	$V_{IN} = 0\text{ V}$		14	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0\text{ V}$		18	pF

1. Sampled only, not 100% tested.

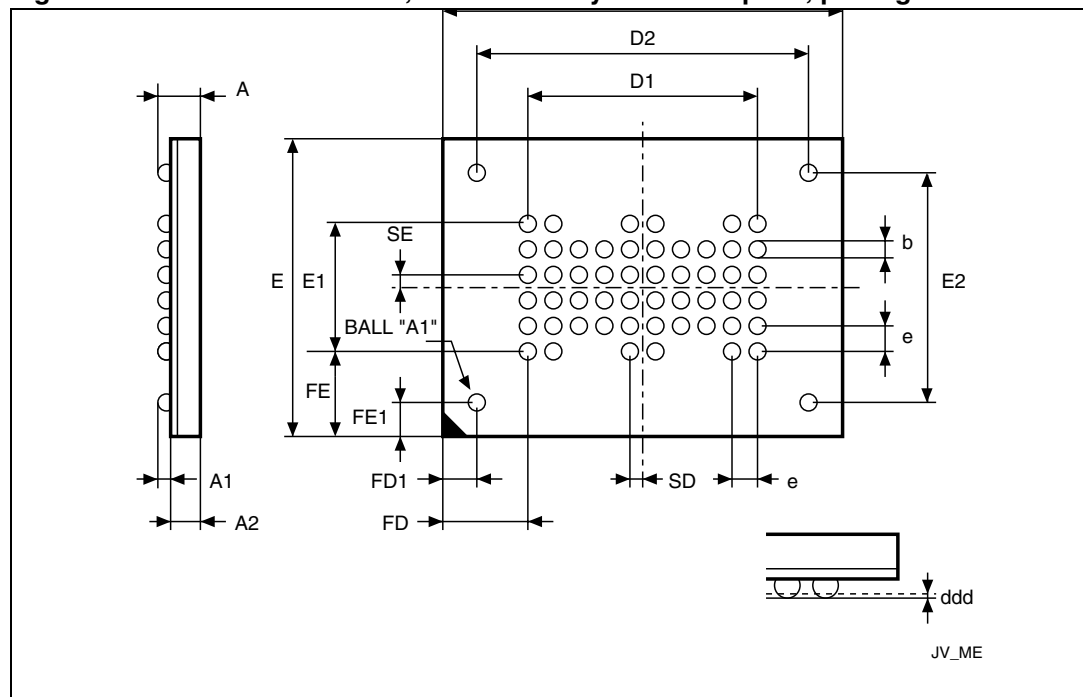
Please refer to the M58LRxxxKCD and M69KM048AA or M69KM096AA datasheets for further DC and AC characteristics values and illustrations.

6 Package mechanical

To meet environmental requirements, Numonyx offers these devices in ECOPACK® packages, which have a lead-free second-level interconnect. In compliance with JEDEC Standard JESD97, the category of second-level interconnect is marked on the package and on the inner box label.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK specifications are available at: www.numonyx.com.

Figure 9. TFBGA56 8 x 6 mm, 8 x 6 ball array - 0.50 mm pitch, package outline

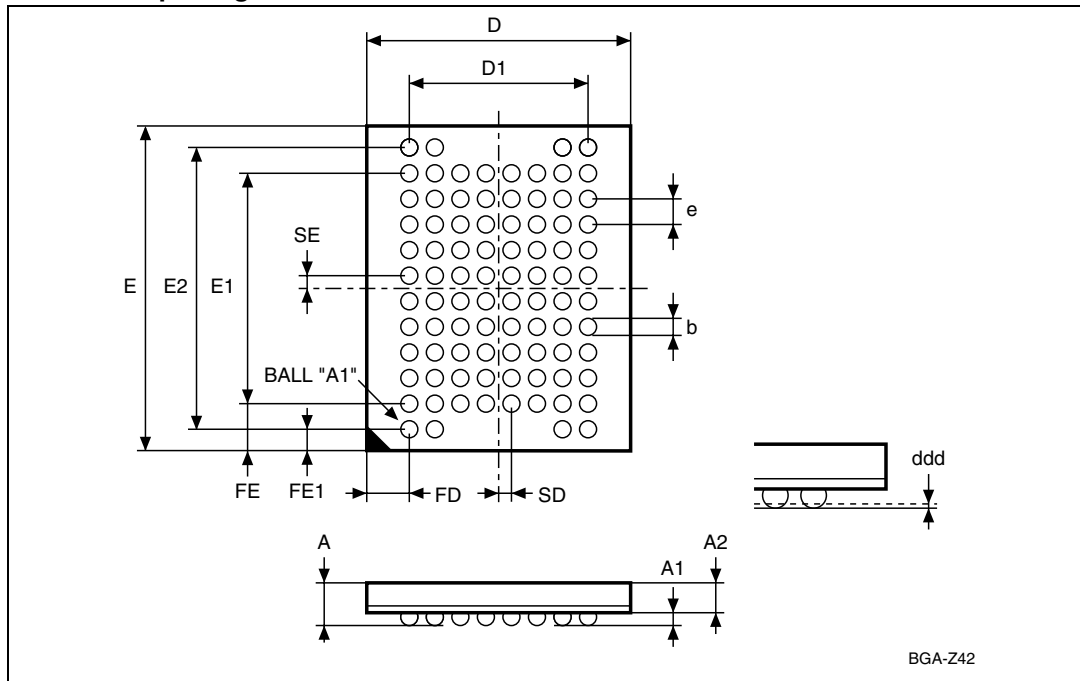


1. Drawing is not to scale.

Table 8. Stacked TFBGA56 8 x 6 mm - 8 x 6 active ball array, 0.50 mm pitch, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.15			0.006	
A2	0.79			0.031		
b	0.30	0.25	0.35	0.012	0.010	0.014
D	8.00	7.90	8.10	0.315	0.311	0.319
D1	4.50			0.177		
D2	6.50			0.256		
ddd			0.08			0.003
E	6.00	5.90	6.10	0.236	0.232	0.240
E1	2.50			0.098		
E2	4.50			0.177		
e	0.50	–	–	0.020	–	–
FD	1.75			0.069		
FD1	0.75			0.030		
FE	1.75			0.069		
FE1	0.75			0.030		

Figure 10. Stacked TFBGA88 8 x 10 mm, 8 x 10 active ball array - 0.8 mm pitch, package outline



1. Drawing is not to scale.

Table 9. TFBGA88 8 x 10 mm - 8 x 10 active ball array, 0.8 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.047
A1		0.200			0.008	
A2	0.850			0.033		
b	0.350	0.300	0.400	0.014	0.012	0.016
D	8.000	7.900	8.100	0.315	0.311	0.319
D1	5.600			0.220		
ddd			0.100			0.004
E	10.000	9.900	10.100	0.394	0.390	0.398
E1	7.200			0.283		
E2	8.800			0.346		
e	0.800	–	–	0.031	–	–
FD	1.200			0.047		
FE	1.400			0.055		
FE1	0.600			0.024		
SD	0.400			0.016		
SE	0.400			0.016		

7 Part numbering

Table 10. Ordering information scheme

Example:

	M36	L	0	R	8	0	5	0	L	3	ZS	F
Device type												
M36 = multichip package (flash + RAM)												
Flash 1 architecture												
L = multilevel, multiple bank, burst mode												
Flash 2 architecture												
0 = no die												
Operating voltage												
$R = V_{DDF} = V_{DDP} = V_{DDQF} = 1.7 \text{ V to } 1.95 \text{ V}$												
Flash 1 density												
7 = 128 Mbit 8 = 256 Mbit												
Flash 2 density												
0 = no die												
RAM 1 density												
5 = 32 Mbit 6 = 64 Mbit												
RAM 2 density												
0 = no die												
Parameter block location												
U = top boot block flash L = bottom boot block flash												
Product version												
3 = 65 nm flash technology and multilevel design, 70 ns speed class; RAM, 70 ns speed mux I/O												
Package												
ZAM = stacked TFBGA88 8 x 10 mm - 8 x 10 active ball array, 0.8 mm pitch ZS = stacked TFBGA56 8 x 6 mm - 8 x 6 active ball array, 0.5 mm pitch												
Packing option												
E = Ecopack® package, standard packing F = Ecopack® package, tape and reel packing												

Note: *Devices are shipped from the factory with the memory content bits, in valid blocks, erased to '1'. For further information on any aspect of this device, please contact your nearest Numonyx sales office.*

8 Revision history

Table 11. Document revision history

Date	Revision	Changes
07-Aug-2007	1	Initial release.
28-Mar-2008	2	Added 256-Mbit density and all associated data throughout the document. Applied Numonyx branding.

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