M36W0R6040T3 M36W0R6040B3
M36W0R6050T3 M36W0R6050B3

64-Mbit (4 Mbits ×16, multiple bank, burst) Flash memory and 16-Mbit (1 Mbit ×16) or 32-Mbit (2 Mbits x16) PSRAM MCP

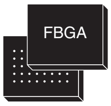
Preliminary Data

Features

- Multichip package
  - 1 die of 64 Mbits (4 Mbits x16) flash memory
  - 1 die of 16 Mbits (1 Mbit x16) or 32 Mbits (2 Mbit x 16) pseudo SRAM
- Supply voltage
  - $V_{DDF} = V_{DDP} = V_{DDQ} = 1.7$ V to 1.95 V
- Low power consumption
- Electronic signature
  - Manufacturer code: 20h
  - Device codes (top flash configuration), M36W0R6040T3 and M36W0R6050T3: 8810h
  - Device codes (bottom flash configuration), M36W0R6040B3 and M36W0R6050B3: 8811h
  - ECOPACK® packages available

Flash memory

- Programming time
  - 10 µs by word typical for fast factory program
  - Double/quadruple word program option
  - Enhanced factory program options
- Memory blocks
  - Multiple bank memory array: 4 Mbit banks
  - Parameter blocks (top or bottom location)
- Synchronous/asynchronous read
  - Synchronous burst read mode: 66 MHz
  - Asynchronous/synchronous page read mode
  - Random access times: 70 ns
- Synchronous burst read suspend



Stacked TFBGA88 (ZAQ)
8 × 10 mm

- Dual operations
  - Program erase in one bank while read in others
  - No delay between read and write operations
- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked
  - $\overline{WP}$ for block lock-down
- Security
  - 128-bit user programmable OTP cells
  - 64-bit unique device number
- Common flash interface (CFI)
- 100 000 program/erase cycles per block
- ECOPACK® package available

PSRAM

- Access time: 70 ns
- Low standby current: 110 µA
- Deep power down current: 10 µA

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Description

The M36W0R6040x3 and M36W0R6050x3 combine two memory devices in a multichip package:

- a 64-Mbit, multiple bank flash memories, the M58WR064KT/B.
- a 16- or 32-Mbit pseudo SRAM, the M69AR024B or M69KB048B, respectively.

Recommended operating conditions do not allow more than one memory to be active at the same time.

The purpose of this document is to describe how the two memory components operate with respect to each other. It must be read in conjunction with the datasheets of the M58WR064KT/B and M69AR024B or M69KB048B, respectively, which fully detail all the specifications required to operate the flash memory and PSRAM components.

The memory is offered in a stacked TFBGA88 (8 × 10 mm, 8 × 10 ball array, 0.8 mm pitch) package, and is supplied with all the bits erased (set to ‘1’).

Figure 1. Logic diagram

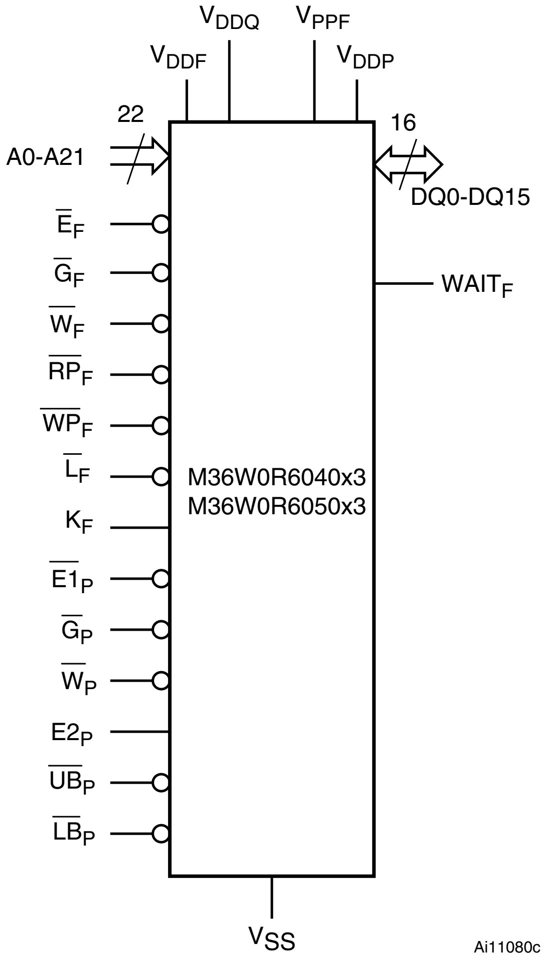
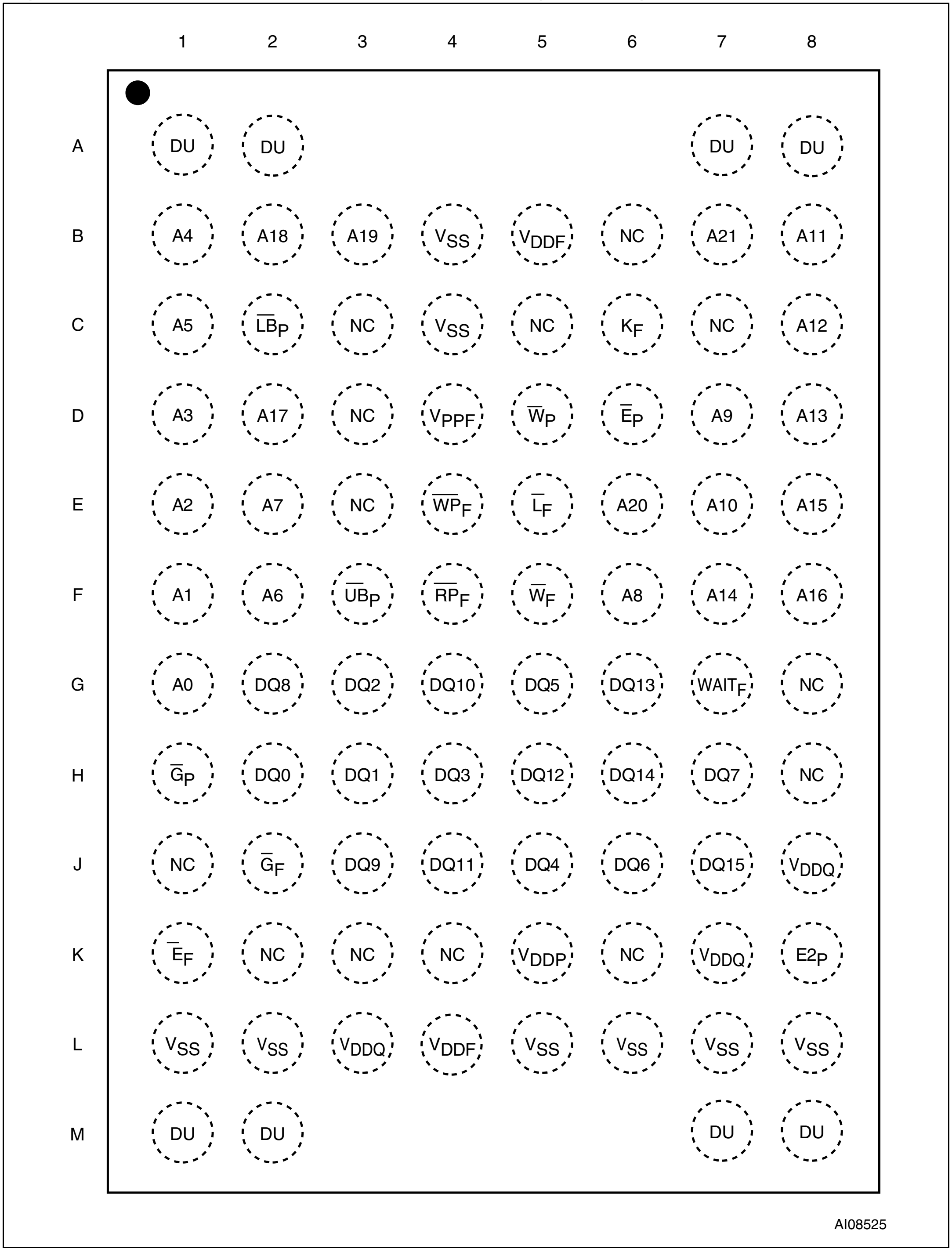


Table 1. Signal names(1) (2)

Name	Function
A0-A19	Common address inputs
DQ0-DQ15	Common data input/output
V_{DDF}	Flash Memory power supply
V_{DDQ}	Common flash and PSRAM power supply for I/O buffers
V_{PPF}	Common flash optional supply voltage for fast program and erase
V_{SS}	Ground
V_{DDP}	PSRAM power supply
NC	Not connected internally
DU	Do not use as internally connected
Flash memory control functions	
A21-A20	Address inputs for the flash memory only
L_F	Latch Enable input
$\overline{E}_F$	Chip Enable input
$\overline{G}_F$	Output Enable input
$\overline{W}_F$	Write Enable input
$\overline{RP}_F$	Reset input
$\overline{WP}_F$	Write Protect input
K_F	Burst Clock
$WAIT_F$	Wait Data in burst mode
PSRAM control functions	
$\overline{E1}_P$	Chip Enable input
$\overline{G}_P$	Output Enable input
$\overline{W}_P$	Write Enable input
$E2_P$	Power-down input
$\overline{UB}_P$	Upper Byte Enable input
$\overline{LB}_P$	Lower Byte Enable input

1. A16-A19 (for a 16-Mbit PSRAM) or A16-A20 (for a 32-Mbit PSRAM) are common to the flash memory and the PSRAM.
2. A20-A21 (if the MCP contains a 16-Mbit PSRAM) or A21 (if the MCP contains a 32-Mbit PSRAM) are address input(s) for the flash memory component only.

Figure 2. TFBGA connections (top view through package)



	1	2	3	4	5	6	7	8
A	DU	DU					DU	DU
B	A4	A18	A19	V_{SS}	V_{DDF}	NC	A21	A11
C	A5	$\overline{LB}_P$	NC	V_{SS}	NC	K_F	NC	A12
D	A3	A17	NC	V_{PPF}	$\overline{W}_P$	$\overline{E}_P$	A9	A13
E	A2	A7	NC	$\overline{WP}_F$	$\overline{L}_F$	A20	A10	A15
F	A1	A6	$\overline{UB}_P$	$\overline{RP}_F$	$\overline{W}_F$	A8	A14	A16
G	A0	DQ8	DQ2	DQ10	DQ5	DQ13	$WAIT_F$	NC
H	$\overline{G}_P$	DQ0	DQ1	DQ3	DQ12	DQ14	DQ7	NC
J	NC	$\overline{G}_F$	DQ9	DQ11	DQ4	DQ6	DQ15	V_{DDQ}
K	$\overline{E}_F$	NC	NC	NC	V_{DDP}	NC	V_{DDQ}	$E2_P$
L	V_{SS}	V_{SS}	V_{DDQ}	V_{DDF}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
M	DU	DU					DU	DU

2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names* for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-A21)

Addresses A0-A21 are common inputs for the flash Memory and PSRAM components. The address inputs select the cells in the memory array to access during bus read operations. During bus write operations they control the commands sent to the command interface of the flash memory program/erase controller, and they select the cells to access in the PSRAM.

The flash memory is accessed through the Chip Enable signal ($\overline{E}_F$) and through the Write Enable ($\overline{W}_F$) signal, while the PSRAM is accessed through two Chip Enable signals ($\overline{E1}_P$ and $E2_P$) and the Write Enable signal ($\overline{W}_P$).

Addresses A20-A21 (for the M36W0R6040x3) or A21 (for the M36W0R6050x3) are inputs for the flash memory component only. The flash memory is accessed through the Chip Enable signals ($\overline{E}_F$) and through the Write Enable ($\overline{W}_F$) signal.

2.2 Data input/output (DQ0-DQ15)

For the flash memory, the data I/O outputs the data stored at the selected address during a bus read operation or inputs a command or the data to be programmed during a write bus operation.

For the PSRAM, the upper byte data inputs/outputs carry the data to or from the upper part of the selected address during a write or read operation, when Upper Byte Enable ($\overline{UB}_P$) is driven Low.

Likewise, the lower byte data inputs/outputs carry the data to or from the lower part of the selected address during a write or read operation, when Lower Byte Enable ($\overline{LB}_P$) is driven Low.

2.3 Flash Chip Enable ($\overline{E}_F$)

The Chip Enable inputs activate the memory control logics, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, and Reset is High, V_{IH}, the device is in active mode. When Chip Enable is at V_{IH} the flash memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

2.4 Flash Output Enable ($\overline{G}_F$)

The Output Enable pins control data outputs during flash memory bus read operations.

2.5 Flash Write Enable ($\overline{W}_F$)

The Write Enable controls the bus write operation of the flash memories' command interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable, whichever occurs first.

2.6 Flash Write Protect ($\overline{WP}_F$)

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is Low, V_{IL}, lock-down is enabled and the protection status of the locked-down blocks cannot be changed. When Write Protect is at High, V_{IH}, lock-down is disabled and the locked-down blocks can be locked or unlocked. (Refer to the lock status table in the M58WR064KT/B datasheet).

2.7 Flash Reset ($\overline{RP}_F$)

The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the Reset supply current I_{DD2}. Refer to the M58WR064KT/B datasheet, for the value of I_{DD2}. After Reset all blocks are in the locked state and the Configuration Register is reset. When Reset is at VIH, the device is in normal operation. Upon exiting reset mode the device enters asynchronous read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3 V logic without any additional circuitry. It can be tied to VRPH (refer to the M58WR064KT/B datasheet).

2.8 Flash Latch Enable ($\overline{L}_F$)

Latch Enable latches the address bits on its rising edge. The address latch is transparent when Latch Enable is Low, V_{IL}, and it is inhibited when Latch Enable is High, V_{IH}. Latch Enable can be kept Low (also at board level) when the Latch Enable function is not required or supported.

2.9 Flash Clock (K_F)

The Clock input synchronizes the flash memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at V_{IL}. Clock is 'don't care' during asynchronous read and in write operations.

2.10 Flash Wait ($WAIT_F$)

WAIT is a flash output signal used during synchronous read to indicate whether the data on the output bus are valid. This output is high impedance when flash Chip Enable is at V_{IH} or flash Reset is at V_{IL}. It can be configured to be active during the wait cycle or one clock cycle in advance. The $WAIT_F$ signal is not gated by Output Enable.

2.11 PSRAM Chip Enable ($\overline{E1}_P$)

When asserted (Low), the Chip Enable, $\overline{E1}_P$, activates the memory state machine, address buffers and decoders, allowing read and write operations to be performed. When de-asserted (High), all other pins are ignored, and the device is put, automatically, in low-power standby mode.

2.12 PSRAM Chip Enable ($E2_P$)

The Chip Enable, $E2_P$, puts the device in deep power-down mode when it is driven Low. This is the lowest power mode.

2.13 PSRAM Output Enable ($\overline{G}_P$)

The Output Enable, $\overline{G}_P$, provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

2.14 PSRAM Write Enable ($\overline{W}_P$)

The Write Enable, $\overline{W}_P$, controls the bus write operation of the memory.

2.15 PSRAM Upper Byte Enable ($\overline{UB}_P$)

The Upper Byte Enable, $\overline{UB}_P$, gates the data on the upper byte data inputs/outputs (DQ8-DQ15) to or from the upper part of the selected address during a write or read operation.

2.16 PSRAM Lower Byte Enable ($\overline{LB}_P$)

The Lower Byte Enable, $\overline{LB}_P$, gates the data on the lower byte data inputs/outputs (DQ0-DQ7) to or from the lower part of the selected address during a write or read operation.

2.17 V_{DDF} supply voltage

V_{DDF} provides the power supply to the internal core of the flash memory component. It is the main power supplies for all flash memory operations (read, program, and erase).

2.18 V_{DDP} supply voltage

The V_{DDP} supply voltage supplies the power for all operations (read or write) and for driving the refresh logic, even when the device is not being accessed.

2.19 V_{DDQ} supply voltage

V_{DDQ} provides the power supply for the flash memory and PSRAM I/O pins. This allows all outputs to be powered independently of the flash memory and PSRAM core power supplies: V_{DDF} and V_{DDP}, respectively.

2.20 V_{PPF} program supply voltage

V_{PPF} is both a flash memory control input and a flash memory power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0 V to V_{DDQ}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLKF} provides absolute protection against program or erase, while $V_{PPF} > V_{PP1F}$ enables these functions (see the M58WR064KT/B datasheet for the relevant values). V_{PPF} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PPF} is in the range of V_{PPHF} it acts as a power supply pin. In this condition V_{PPF} must be stable until the program/erase algorithm is completed.

2.21 V_{SS} ground

V_{SS} is the common ground reference for all voltage measurements in the flash (core and I/O buffers) and PSRAM chips.

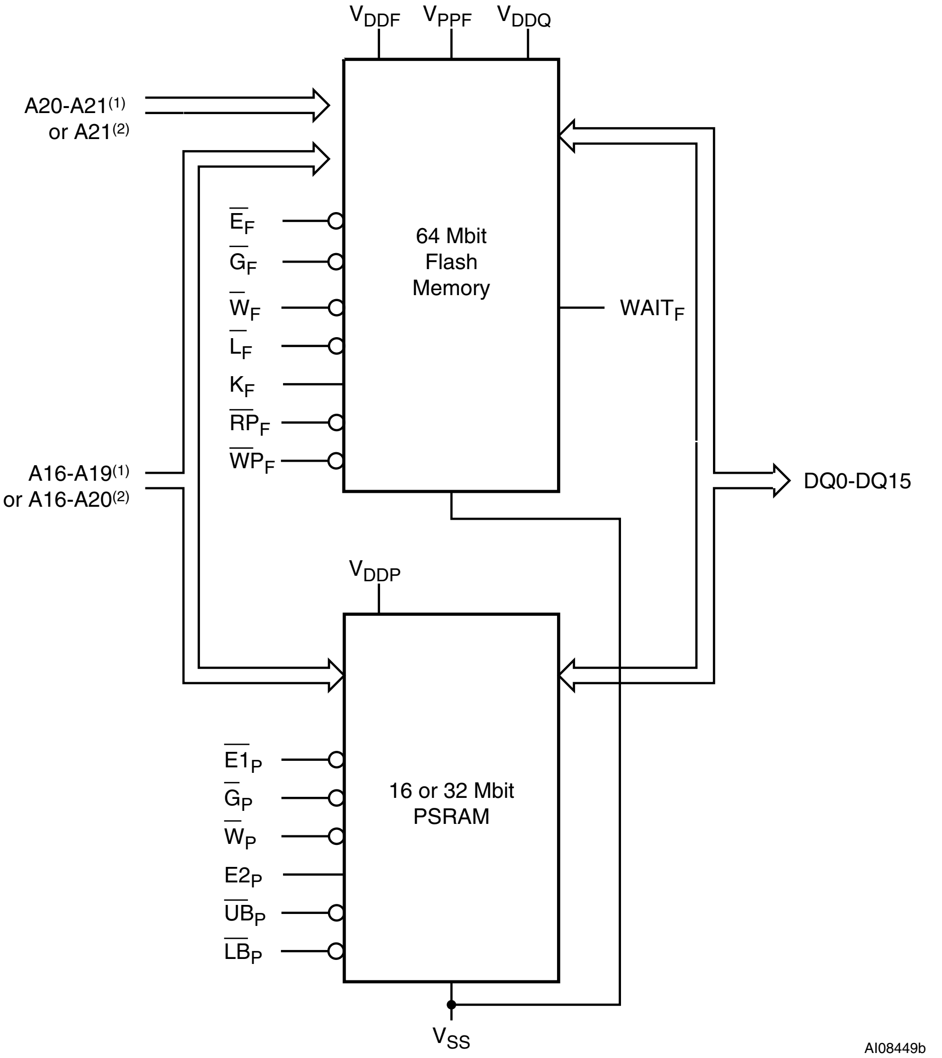
Note: Each flash memory device in a system should have its supply voltage (V_{DDF}) and the program supply voltage V_{PPF} decoupled with a 0.1 µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 5: AC measurement load circuit. The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

3 Functional description

The flash memory and PSRAM components have separate power supplies but share the same grounds. They are distinguished by three Chip Enable inputs: $\overline{E}_F$ for the flash memory and $\overline{E1}_P$ and $E2_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is simultaneous read operations on the flash memory and the PSRAM which would result in a data bus contention. Therefore it is recommended to put the other devices in the high impedance state when reading the selected device.

Figure 3. Functional block diagram



1. Address inputs corresponding to the M36W0R6040T3 and M36W0R6040B3 devices.
2. Address inputs corresponding to the M36W0R6050T3 and M36W0R6050B3 devices.

Table 2. Main operating modes[1]

Operation	$\overline{E}_F$	$\overline{G}_P$	$\overline{W}_P$	$\overline{L}_F$	$\overline{RP}_F$	WAIT$_F$[2]	$\overline{E1}_P$	$\overline{E2}_P$	$\overline{G}_P$	$\overline{W}_P$	$\overline{UB}_P$	$\overline{LB}_P$	DQ15-DQ0
Flash read	V_{IL}	V_{IL}	V_{IH}	V_{IL}[3]	V_{IH}		PSRAM must be disabled						Flash data out
Flash write	V_{IL}	V_{IH}	V_{IL}	V_{IL}[3]	V_{IH}								Flash data in
Flash address latch	V_{IL}	X	V_{IH}	V_{IL}	V_{IH}								Flash data out or Hi-Z[4]
Flash output disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}		Any PSRAM mode is allowed						Flash Hi-Z
Flash standby	V_{IH}	X	X	X	V_{IH}	Hi-Z							Flash Hi-Z
Flash reset	X	X	X	X	V_{IL}	Hi-Z							Flash Hi-Z
PSRAM read	Flash memory must be disabled						V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	PSRAM data out
PSRAM write							V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	PSRAM data in
Output disable	Any flash mode is allowed.						V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	PSRAM Hi-Z
PSRAM standby							V_{IH}	V_{IH}	X	X	X	X	PSRAM Hi-Z
PSRAM deep power-down							X	V_{IL}	X	X	X	X	PSRAM Hi-Z

1. X = ‘don't care’.
2. WAIT signal polarity is configured using the Set Configuration Register command. Refer to M58WR064KT/B datasheet for details.
3. $\overline{L}_F$ can be tied to V_{IH} if the valid address has been previously latched.
4. Depends on $\overline{G}_F$.

4 Maximum ratings

Stressing the device above the rating listed in *Table 3: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient operating temperature	–30	85	°C
T_{BIAS}	Temperature under bias	–40	125	°C
T_{STG}	Storage temperature	–55	125	°C
V_{IO}	Input or output voltage	–0.5	V_{DDQ}+0.6	V
V_{DDF}	Flash memory core supply voltage	–0.2	2.45	V
V_{DDQ}	Input/output supply voltage	–0.2	2.45	V
V_{DDP}	PSRAM supply voltage	–0.2	3.3	V
V_{PPF}	Flash memory program voltage	–0.2	10	V
I_O	Output short circuit current		100	mA
t_{VPPFH}	Time for V_{PPF} at V_{PPFH}		100	hours

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables in this section are derived from tests performed under the measurement conditions summarized in *Table 4*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC measurement conditions

Parameter	Flash memory		PSRAM		Unit
	Min	Max	Min	Max	
V_{DDF} supply voltage	1.7	1.95	–	–	V
V_{DDP} supply voltage	–	–	1.7	1.95	V
V_{DDQ} supply voltage	1.7	1.95	–	–	V
V_{PPF} supply voltage (factory environment)	8.5	9.5	–	–	V
V_{PPF} supply voltage (application environment)	–0.4	V_{DDQ} +0.4	–	–	V
Ambient operating temperature	–30	85	–30	85	°C
Load capacitance (C_L)	30		50		pF
Input rise and fall times	5				ns
Input pulse voltages	0 to V_{DDQ}		0 to V_{DDP}		V
Input and output timing ref. voltages	$V_{DDQ}/2$		$V_{DDP}/2$		V

Figure 4. AC measurement I/O waveform

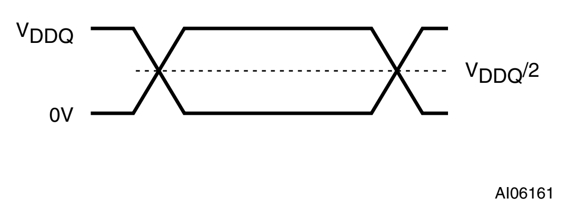


Figure 5. AC measurement load circuit

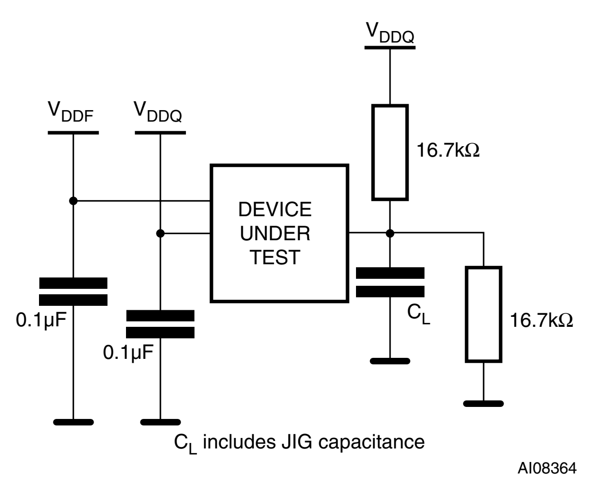


Table 5. Device capacitance[1]

Symbol	Parameter	Test condition	Min	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$ V		13	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$ V		20	pF

1. Sampled only, not 100% tested.

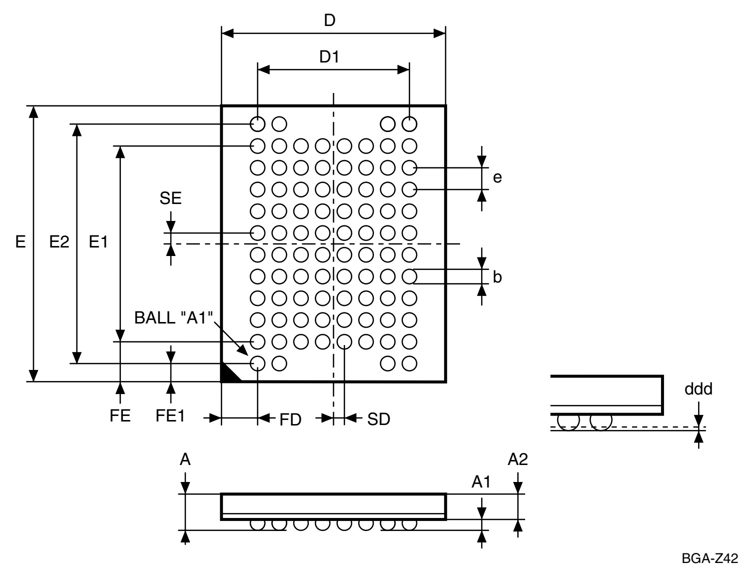
Please refer to the M58WR064KT/B and M69AR024B or M69KB048B datasheets for further DC and AC characteristics values and illustrations.

6 Package mechanical

To meet environmental requirements, Numonyx offers the M36W0R6040x3 and M36W0R6050x3 in ECOPACK® packages, which have a lead-free second-level interconnect. In compliance with JEDEC standard JESD97, the category of second-level interconnect is marked on the package and on the inner box label.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK specifications are available at: *www.numonyx.com*.

Figure 6. Stacked TFBGA88 8 × 10 mm - 8 × 10 active ball array, 0.8 mm pitch, package outline



1. Drawing is not to scale.

Table 6. Stacked TFBGA88 8 × 10 mm - 8 × 10 ball array, 0.8 mm pitch, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.200			0.0079	
A2	0.850			0.0335		
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	5.600			0.2205		
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	7.200			0.2835		
E2	8.800			0.3465		
e	0.800	–	–	0.0315	–	–
FD	1.200			0.0472		
FE	1.400			0.0551		
FE1	0.600			0.0236		
SD	0.400			0.0157		
SE	0.400			0.0157		

7 Part numbering

Table 7. Ordering information scheme

Example: M36 W 0 R 6 0 4 0 T 3 ZAQ E

Device type

M36 = multichip package (multiple flash + RAM)

Flash 1 architecture

W = multiple bank, burst mode

Flash 2 architecture

0 = none present

Operating voltage

R = V_{DDF} = V_{DDQ} =V_{DDP} = 1.7 V to 1.95 V

Flash 1 density

6 = 64 Mbit

Flash 2 density

0 = none present

RAM 1 density

4 = 16 Mbit
5 = 32 Mbit

RAM 0 density

0 = none present

Parameter blocks location

T = top boot block flash
B = bottom boot block flash

Product version

3 = 65 nm flash technology, 70 ns; RAM, 70 ns

Package

ZAQ = stacked TFBGA88 8 × 10 mm - 8 × 10 active ball array, 0.8 mm pitch

Option

E = ECOPACK® package, standard packing
F = ECOPACK® package, tape and reel packing

Devices are shipped from the factory with the memory content bits erased to ’1’. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the STMicroelectronics sales office nearest to you.

8 Revision history

Table 8. Document revision history

Date	Version	Revision Details
06-Dec-2007	1	Initial release.
11-Dec-2007	2	Typing error in *Section 1: Description on page 6*.
20-Feb-2008	3	Removed 0.18 µm from the RAM product version details of *Table 7: Ordering information scheme*.
31-Mar-2008	4	Changed every instance of M69KB048BE to M69KB048B. Applied Numonyx branding.

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