



# NCA9536

4-bit I<sup>2</sup>C and SMBus low-power I/O expander with configurable registers and interrupt

Rev. 1 — 4 March 2026

Product data sheet

## 1. General description

The NCA9536 is a 4-bit bidirectional I/O expander compliant with I<sup>2</sup>C and SMBus protocols, operating over a wide supply range of 1.65 V to 5.5 V. It enables remote GPIO expansion for microcontroller-based systems via a standard two-wire interface (SCL/SDA), supporting clock frequencies up to 1 MHz (Fast-Mode Plus).

Part of Nexperia's advanced I<sup>2</sup>C-bus expander portfolio, the device is optimized for space-constrained applications requiring additional I/O such as LED control, button interfacing, sensor integration, status indication, and signal routing. Its compact form factor and low-power operation make it well-suited for consumer, industrial, and IoT designs.

The NCA9536 provides 4 bits in Configuration Register defining each I/O as input or output, 4 bits in Input Port Register capturing the logic state of input pins, 4 bits in Output Port Register controlling the output logic levels and 4 bits in Polarity Inversion Register allowing inversion of input logic (active HIGH or LOW). In addition, 2 bits in special function register are provided to disable the internal pull-up resistors and to configure P3 as an interrupt (INT) output.

The system controller configures the I/Os via the Configuration Register, accesses real-time data through the Input Port Register, and controls the outputs through the Output Port Registers. The Polarity Inversion Register allows flexible logic interpretation. All registers are accessible via the I<sup>2</sup>C interface.

The NCA9536 supports I<sup>2</sup>C General Call address (0x00), which upon receiving a specific reset command (0x06), to initiate a software-triggered reset. This is ideal for systems lacking hardware reset or requiring simultaneous reset of multiple devices. Additionally, Pin P3 can be configured as an interrupt output (INT), enabling efficient real-time input monitoring for applications like button interfaces or sensor events. Upon power-on reset, all registers are initialized to default states, and the internal state machine is set. The device features a fixed I<sup>2</sup>C-bus address, supporting single-device operation per bus.

## 2. Features

- 4-bit I<sup>2</sup>C-bus GPIO
- Operating power supply voltage range of 1.65 V to 5.5 V
- 5 V tolerant I/Os
- Polarity Inversion register
- Software reset by General Call
- P3 reconfigurable as Interrupt output
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 4 I/O pins which default to 4 inputs with 100 k $\Omega$  internal pull-up resistor
- 0 Hz to 1 MHz clock frequency Fast-mode Plus I<sup>2</sup>C-bus
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Packages offered: SOT1233-2 (X2SON8), TSSOP8 (SOT505-3)
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

| Type number                                                                                                         | Package           |        |                                                                                                                 |                           |
|---------------------------------------------------------------------------------------------------------------------|-------------------|--------|-----------------------------------------------------------------------------------------------------------------|---------------------------|
|                                                                                                                     | Temperature range | Name   | Description                                                                                                     | Version                   |
| <a href="#">NCA9536GX</a><br><a href="#">NCA9536AGX</a><br><a href="#">NCA9536BGX</a><br><a href="#">NCA9536CGX</a> | -40 °C to +125 °C | X2SON8 | plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 x 0.8 x 0.32 mm | <a href="#">SOT1233-2</a> |
| <a href="#">NCA9536DQ</a>                                                                                           | -40 °C to +125 °C | TSSOP8 | plastic, thin shrink small outline package; 8 leads; 0.65 mm pitch; 3 mm x 3 mm x 1.1 mm body                   | <a href="#">SOT505-3</a>  |

4. Marking

Table 2. Marking

| Type number | Marking code |
|-------------|--------------|
| NCA9536GX   | z5           |
| NCA9536AGX  | z6           |
| NCA9536BGX  | z7           |
| NCA9536CGX  | z8           |
| NCA9536DQ   | A9536        |

5. Block diagram

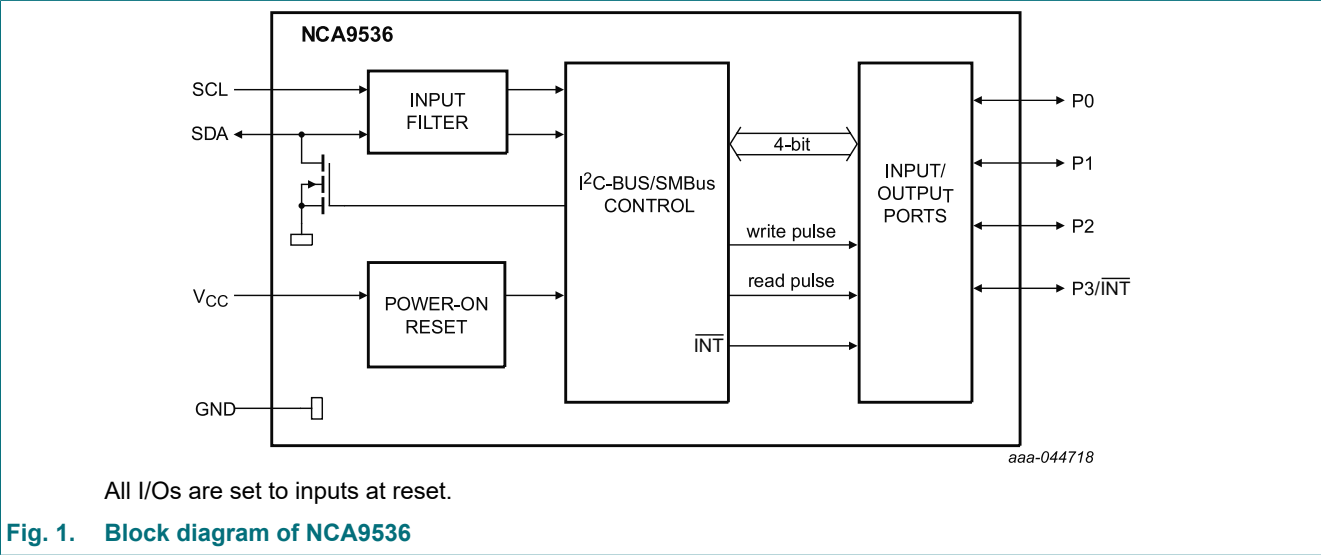


Fig. 1. Block diagram of NCA9536

6. Pinning information

6.1. Pinning

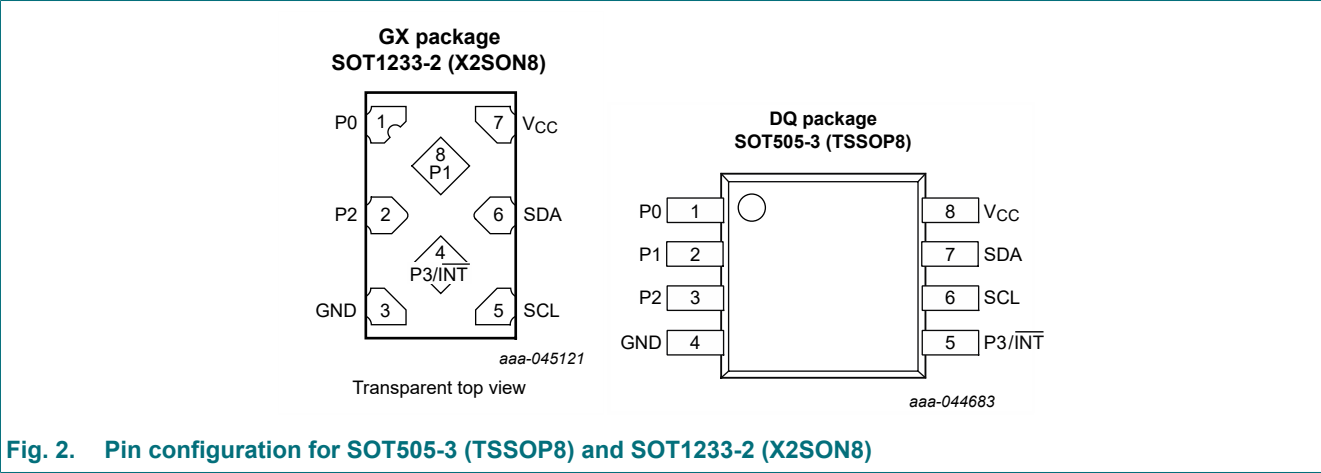


Fig. 2. Pin configuration for SOT505-3 (TSSOP8) and SOT1233-2 (X2SON8)

6.2. Pin description

Table 3. Pin description

| Symbol          | Pin       |          | Description                                                                                                                       |
|-----------------|-----------|----------|-----------------------------------------------------------------------------------------------------------------------------------|
|                 | SOT1233-2 | SOT505-3 |                                                                                                                                   |
| P0              | 1         | 1        | input/output 0                                                                                                                    |
| P2              | 2         | 3        | input/output 2                                                                                                                    |
| GND             | 3         | 4        | supply ground                                                                                                                     |
| P3/INT          | 4         | 5        | input/output 3; When configured as $\overline{\text{INT}}$ , operates as open drain. Internal pull-up resistor enabled by default |
| SCL             | 5         | 6        | serial clock line                                                                                                                 |
| SDA             | 6         | 7        | serial data line                                                                                                                  |
| V <sub>CC</sub> | 7         | 8        | supply voltage                                                                                                                    |
| P1              | 8         | 2        | input/output 1                                                                                                                    |

7. Functional description

Refer to [Fig. 1](#) "Block diagram".

7.1. Registers

7.1.1. Command byte

Table 4. Command byte

| Command | Protocol        | Function                    |
|---------|-----------------|-----------------------------|
| 0x00    | read byte       | Input Port register         |
| 0x01    | read/write byte | Output Port register        |
| 0x02    | read/write byte | Polarity Inversion register |
| 0x03    | read/write byte | Configuration register      |
| 0x50    | read/write byte | Special Function register   |

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

7.1.2. Register 0x00 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 0x03. Writes to this register have no effect.

The default 'X' is determined by the externally applied logic level, normally logic 1 when no external signal externally applied because of the internal pull-up resistors.

Table 5. Register 0x00 - Input Port register bit description

Legend: \* default value

| Bit | Symbol | Access    | Value | Description                                  |
|-----|--------|-----------|-------|----------------------------------------------|
| 7   | I7     | read only | 1*    | not used                                     |
| 6   | I6     | read only | 1*    |                                              |
| 5   | I5     | read only | 1*    |                                              |
| 4   | I4     | read only | 1*    |                                              |
| 3   | I3     | read only | X     | determined by externally applied logic level |
| 2   | I2     | read only | X     |                                              |
| 1   | I1     | read only | X     |                                              |
| 0   | I0     | read only | X     |                                              |

### 7.1.3. Register 0x01 - Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 0x03. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

'Not used' bits can be programmed with either logic 0 or logic 1.

**Table 6. Register 0x01 - Output Port register bit description**

Legend: \* default value

| Bit | Symbol | Access | Value | Description                                                                |
|-----|--------|--------|-------|----------------------------------------------------------------------------|
| 7   | O7     | R/W    | 1*    | not used                                                                   |
| 6   | O6     | R/W    | 1*    |                                                                            |
| 5   | O5     | R/W    | 1*    |                                                                            |
| 4   | O4     | R/W    | 1*    |                                                                            |
| 3   | O3     | R/W    | 1*    | reflects outgoing logic levels of pins defined as outputs by Register 0x03 |
| 2   | O2     | R/W    | 1*    |                                                                            |
| 1   | O1     | R/W    | 1*    |                                                                            |
| 0   | O0     | R/W    | 1*    |                                                                            |

### 7.1.4. Register 0x02 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

'Not used' bits can be programmed with either logic 0 or logic 1.

**Table 7. Register 0x02 - Polarity Inversion register bit description**

Legend: \* default value

| Bit | Symbol | Access | Value | Description                                  |
|-----|--------|--------|-------|----------------------------------------------|
| 7   | N7     | R/W    | 0*    | not used                                     |
| 6   | N6     | R/W    | 0*    |                                              |
| 5   | N5     | R/W    | 0*    |                                              |
| 4   | N4     | R/W    | 0*    |                                              |
| 3   | N3     | R/W    | 0*    | inverts polarity of Input Port register data |
| 2   | N2     | R/W    | 0*    |                                              |
| 1   | N1     | R/W    | 0*    |                                              |
| 0   | N0     | R/W    | 0*    |                                              |

### 7.1.5. Register 0x03 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to V<sub>CC</sub>.

'Not used' bits can be programmed with either logic 0 or logic 1.

**Table 8. Register 0x03 - Configuration register bit description**

Legend: \* default value

| Bit | Symbol | Access | Value | Description                                                                                                                                                                                                         |
|-----|--------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | C7     | R/W    | 1*    | not used                                                                                                                                                                                                            |
| 6   | C6     | R/W    | 1*    |                                                                                                                                                                                                                     |
| 5   | C5     | R/W    | 1*    |                                                                                                                                                                                                                     |
| 4   | C4     | R/W    | 1*    |                                                                                                                                                                                                                     |
| 3   | C3     | R/W    | 1*    | configures the directions of the I/O pins <ul style="list-style-type: none"> <li>0 = corresponding port pin enabled as an output</li> <li>1 = corresponding port pin configured as input (default value)</li> </ul> |
| 2   | C2     | R/W    | 1*    |                                                                                                                                                                                                                     |
| 1   | C1     | R/W    | 1*    |                                                                                                                                                                                                                     |
| 0   | C0     | R/W    | 1*    |                                                                                                                                                                                                                     |

### 7.1.6. Register 0x50 – Special Function register

This register configures the directions of the I/O pins. If "P3 as  $\overline{\text{INT}}$ " bit is set to 1, the function of P3 will change to  $\overline{\text{INT}}$  output. If "PU Disabled" bit is set to 1, all the internal pull-up resistors on the I/O pins are disabled, including the P3 if it is configured as  $\overline{\text{INT}}$  output

'Not used' bits can be programmed with either logic 0 or logic 1.

**Table 9. Register 0x50 - Special Function register bit description**

Legend: \* default value

| Bit | Symbol                              | Access | Value | Description                                                                                                                                                                                                                        |
|-----|-------------------------------------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | S7 (P3 as $\overline{\text{INT}}$ ) | R/W    | 0*    | <ul style="list-style-type: none"> <li>0 = P3/<math>\overline{\text{INT}}</math> pin behaves as a GPIO (P3)</li> <li>1 = P3/<math>\overline{\text{INT}}</math> pin behaves as <math>\overline{\text{INT}}</math> output</li> </ul> |
| 6   | S6 (PU disabled)                    | R/W    | 0*    | <ul style="list-style-type: none"> <li>0 = Internal pull-ups on all IOs are enabled</li> <li>1 = Internal pull-ups on all IOs are disabled</li> </ul>                                                                              |
| 5   | S5                                  | R/W    | 0*    | not used                                                                                                                                                                                                                           |
| 4   | S4                                  | R/W    | 0*    |                                                                                                                                                                                                                                    |
| 3   | S3                                  | R/W    | 0*    |                                                                                                                                                                                                                                    |
| 2   | S2                                  | R/W    | 0*    |                                                                                                                                                                                                                                    |
| 1   | S1                                  | R/W    | 0*    |                                                                                                                                                                                                                                    |
| 0   | S0                                  | R/W    | 0*    |                                                                                                                                                                                                                                    |

## 7.2. Power-On Reset

When power is applied to  $V_{CC}$ , an internal Power-On Reset (POR) holds the NCA9536 in a reset condition until  $V_{CC}$  has reached  $V_{POR}$ . At that point, the reset condition is released and the NCA9536 registers and state machine will initialize to their default states. Thereafter,  $V_{CC}$  must be lowered below 0.2 V to reset the device.

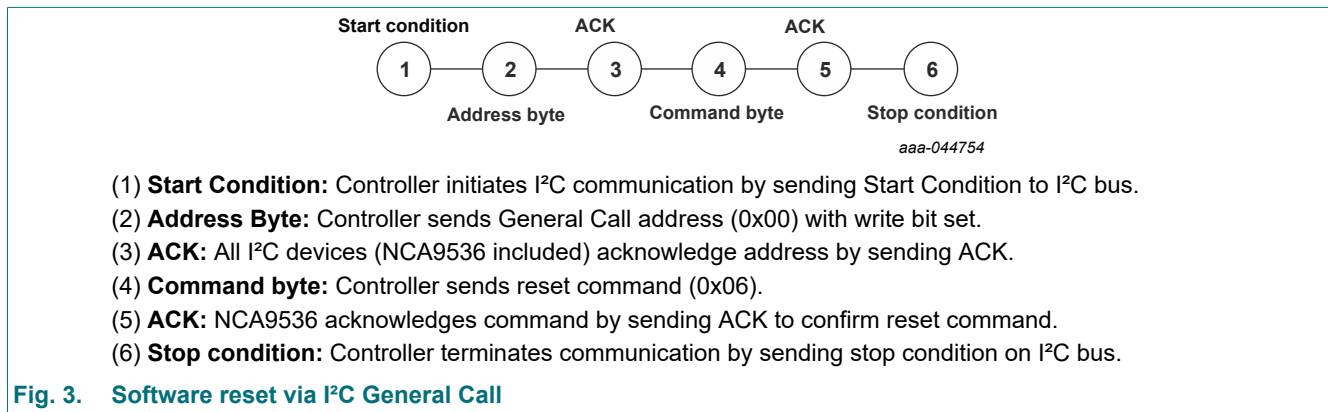
For a power reset cycle,  $V_{CC}$  must be lowered below 0.2 V and then restored to the operating voltage.

## 7.3. Software reset via I<sup>2</sup>C General Call

The NCA9536 supports a software reset mechanism using the I<sup>2</sup>C General Call address (0x00). When the device receives a specific reset command (0x06) through this address, it performs a soft reset. This action performs the below mentioned:

- Clears all internal registers to their default states
- Reinitializes the device without requiring a power cycle
- Helps recover from communication errors or unexpected behavior

This feature is particularly useful in systems where hardware reset is not feasible or where multiple devices need to be reset simultaneously via a single I<sup>2</sup>C command.



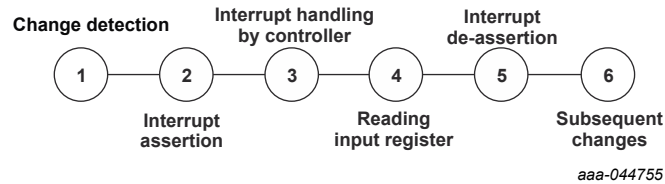
## 7.4. P3 reconfigurable as interrupt output ( $\overline{\text{INT}}$ )

Pin P3 on the NCA9536 can be optionally configured to function as an interrupt output ( $\overline{\text{INT}}$ ).

When enabled:

- The pin signals the changes in the input state of any I/O configured as input
- It allows the host controller to respond to input changes without polling
- The interrupt is active-low and open-drain, suitable for wired-OR configurations

This feature enhances responsiveness and power efficiency in systems where real-time input monitoring is critical, such as in button interfaces or sensor-triggered events.



- (1) **Change detection:** The NCA9536 continuously monitors the input pins (P0, P1, and P2) for changes in their logic levels.
- (2) **Interrupt assertion:** When a change is detected on any of the input pins, the P3 pin is asserted. The specific logic level that represents "asserted" depends on the external pull-up resistor configuration. Typically, an external pull-up resistor is used, and the NCA9536 drives the P3 pin low to assert the interrupt.
- (3) **Interrupt handling by controller:** The controller detects the interrupt signal on the P3 pin.
- (4) **Reading the input register:** The controller reads the Input Register (address 0x00) of the NCA9536. This action acknowledges the interrupt and clears the interrupt condition within the NCA9536.
- (5) **Interrupt de-assertion:** After the Input Register is read, the P3 pin is de-asserted (typically pulled high by the external pull-up resistor).
- (6) **Subsequent changes:** The NCA9536 continues to monitor the input pins, and the process repeats if another change is detected.

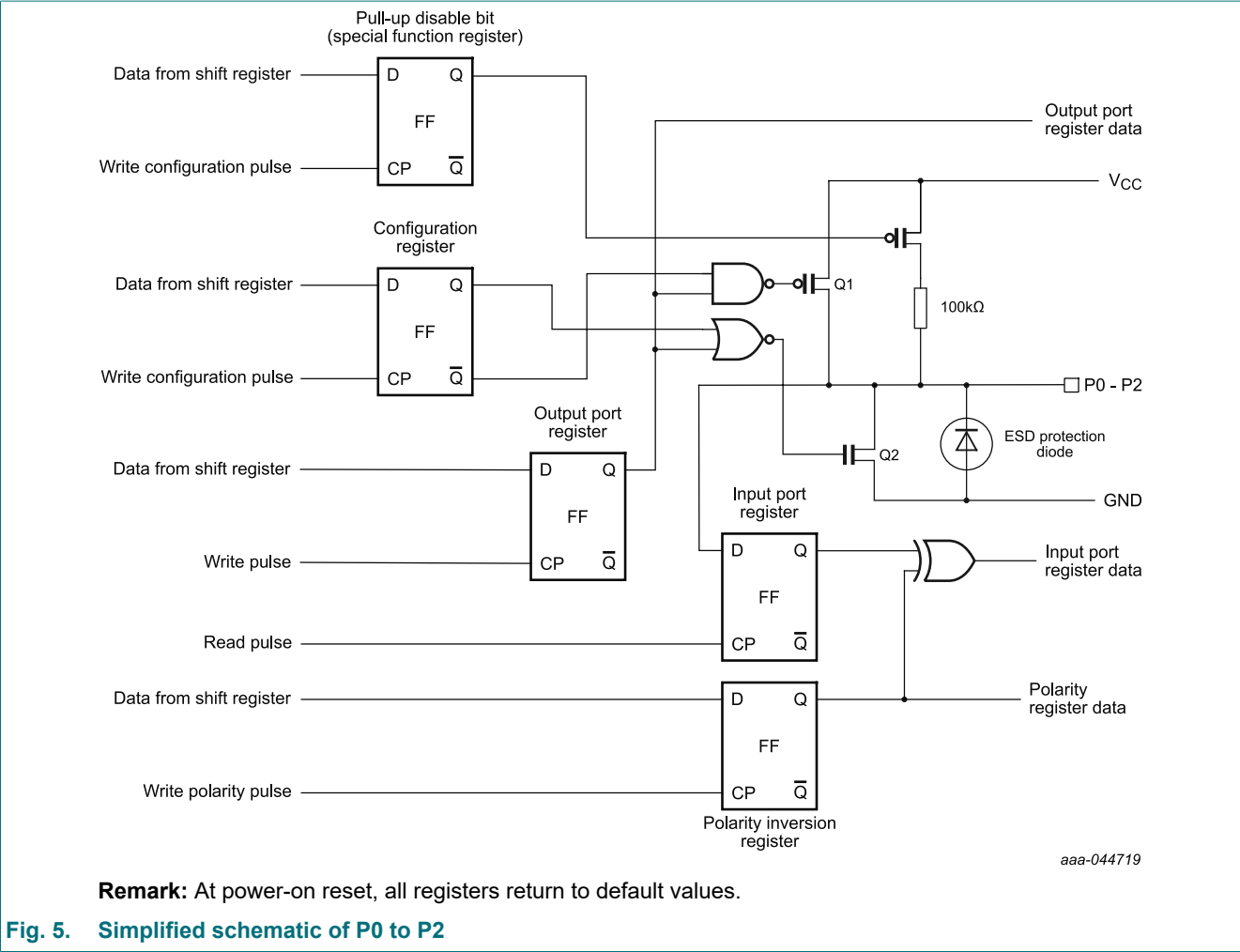
**Fig. 4. NCA9536 Interrupt Sequence ( $\overline{\text{INT}}$ )**

## 7.5. I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up (100 k $\Omega$  typical) to  $V_{CC}$ . The input voltage may be raised above  $V_{CC}$  to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance paths that exist between the pin and either  $V_{CC}$  or GND.

4-bit I<sup>2</sup>C and SMBus low-power I/O expander with configurable registers and interrupt



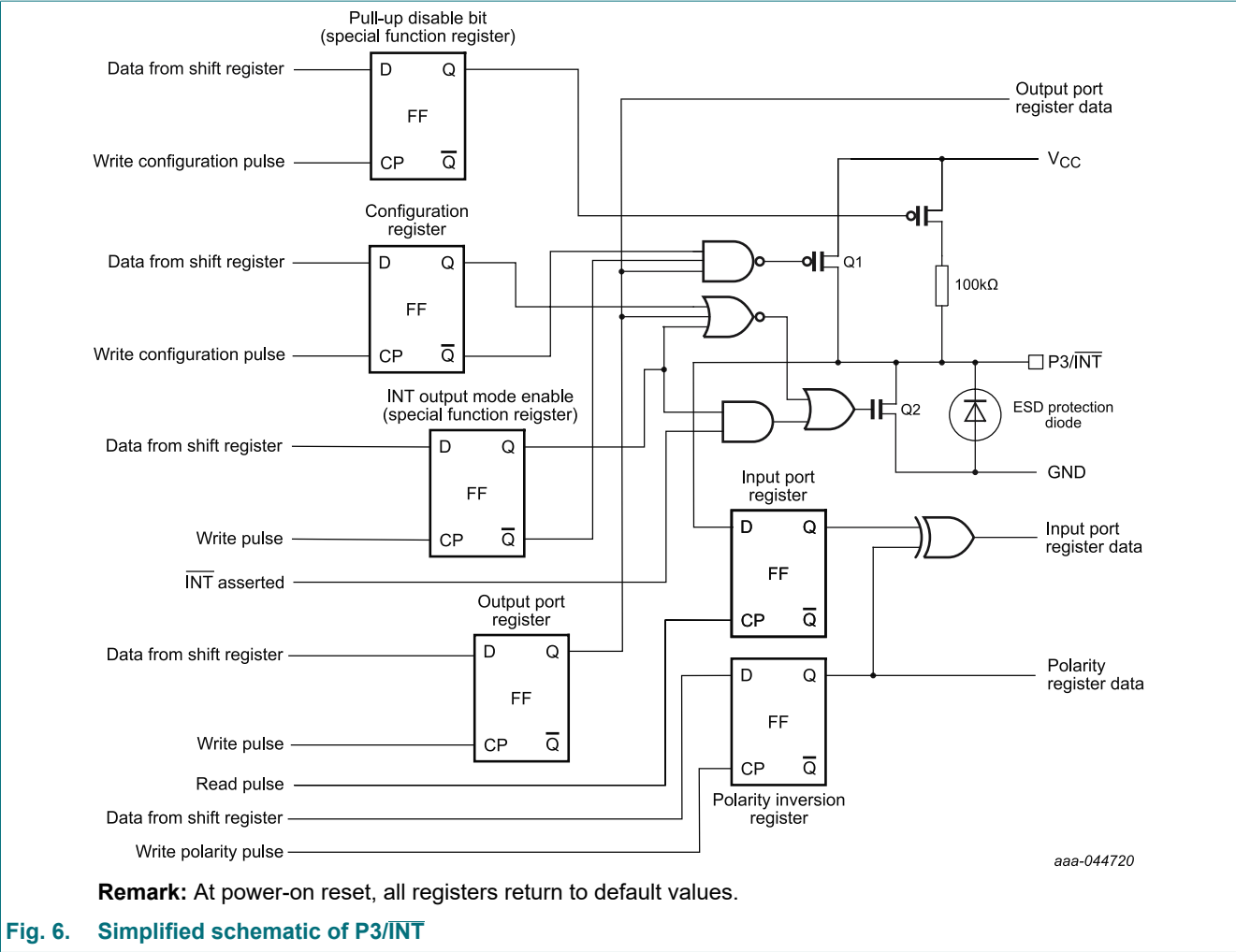


Fig. 6. Simplified schematic of P3/INT

7.6. Device address

Table 10. NCA9536 device addresses

| Type number | A6 | A5 | A4 | A3 | A2 | A1 | A0 | 7-bit address (hex) | 7-bit address (dec) |
|-------------|----|----|----|----|----|----|----|---------------------|---------------------|
| NCA9536DQ   | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 0x41                | 65                  |
| NCA9536GX   | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 0x41                | 65                  |
| NCA9536AGX  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0x40                | 64                  |
| NCA9536BGX  | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 0x43                | 67                  |
| NCA9536CGX  | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 0x42                | 66                  |

7.7. Bus transactions

Data is transmitted to the NCA9536 registers using the Write mode as shown in Fig. 7 and Fig. 8. Data is read from the NCA9536 registers using the Read mode as shown in Fig. 9 and Fig. 10. These devices do not implement an auto-increment function, so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

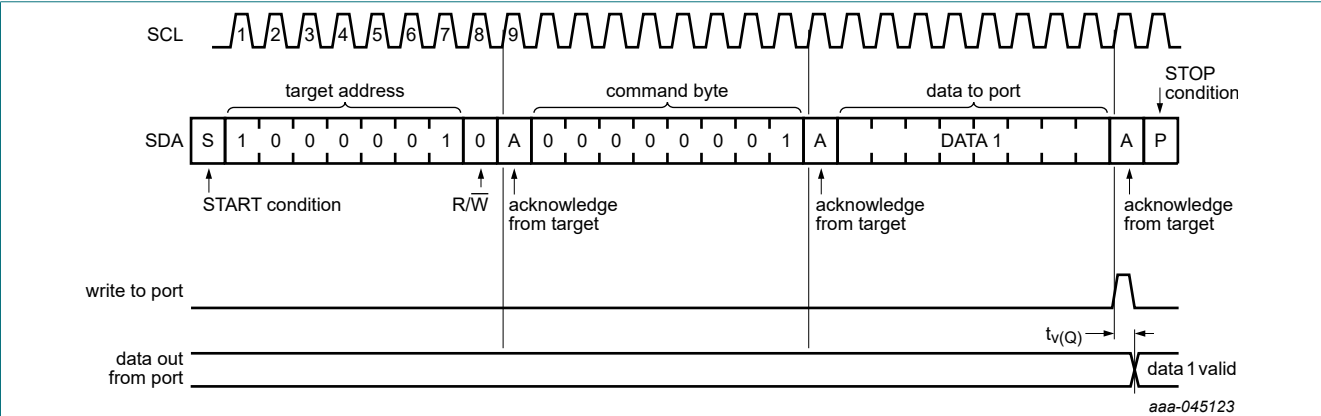


Fig. 7. Write to Output Port register

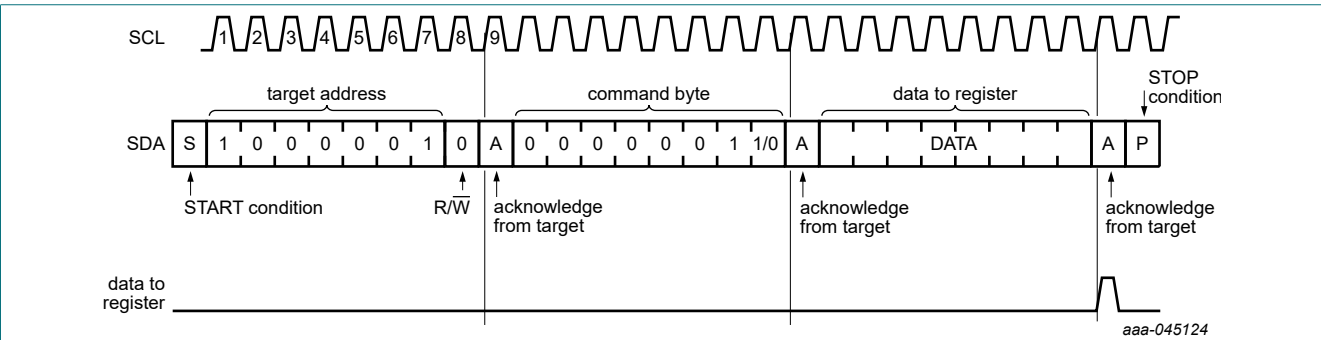


Fig. 8. Write to Configuration register or Polarity Inversion register

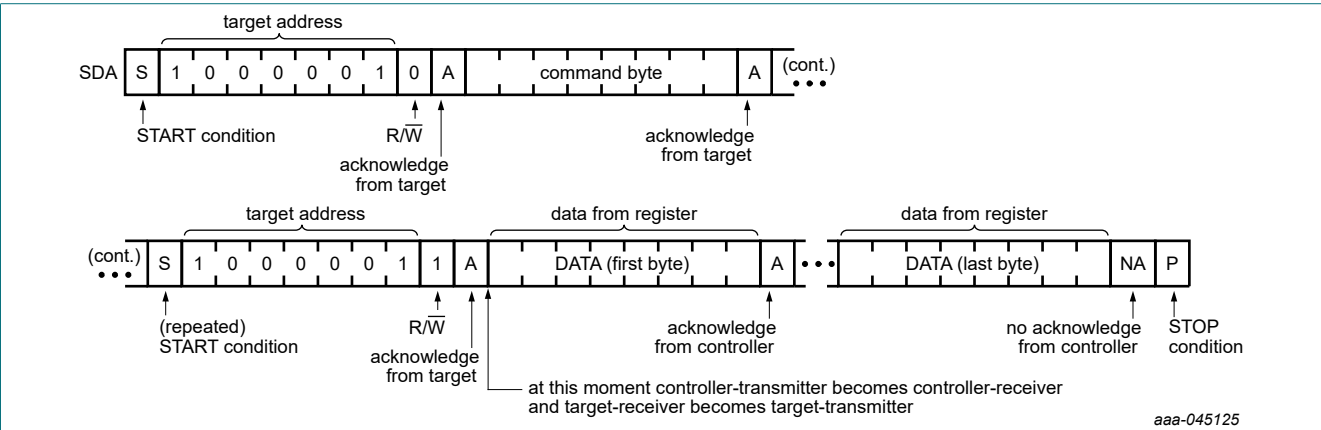
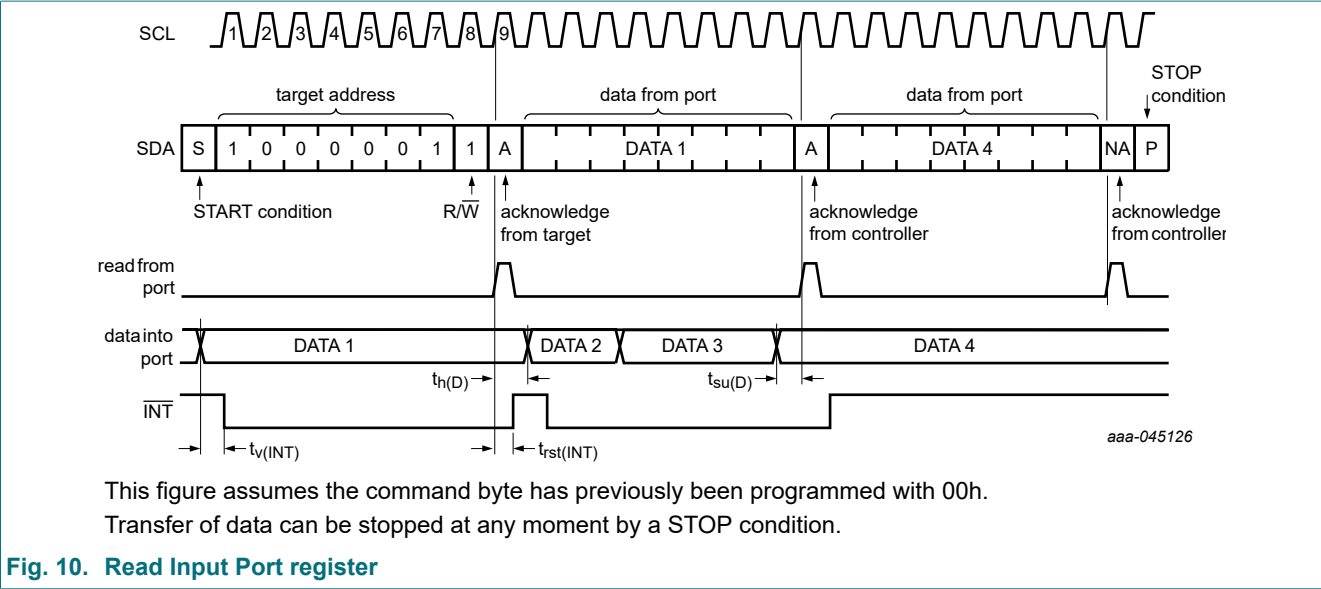


Fig. 9. Read from register



8. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

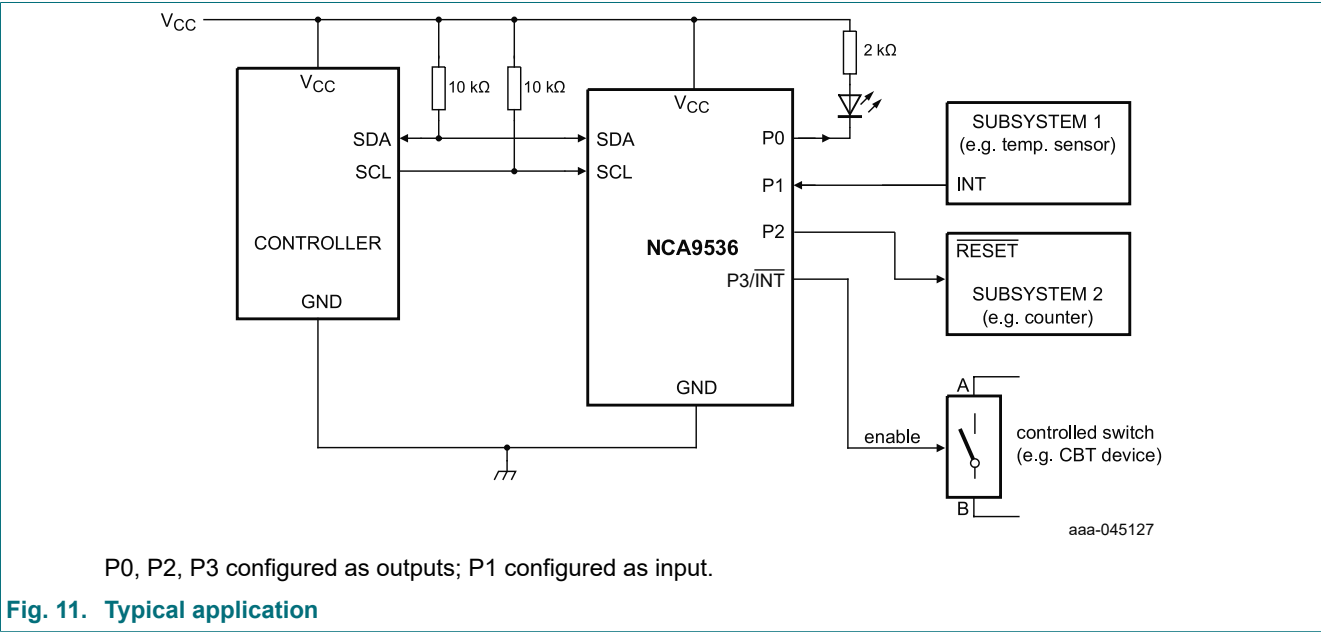
| Symbol              | Parameter                      | Conditions | Min       | Max  | Unit |
|---------------------|--------------------------------|------------|-----------|------|------|
| V <sub>CC</sub>     | supply voltage                 |            | -0.5      | +6.0 | V    |
| I <sub>I</sub>      | input current                  |            | -         | ±20  | mA   |
| V <sub>I/O</sub>    | voltage on an input/output pin |            | GND - 0.5 | 6.0  | V    |
| I <sub>O(Pn)</sub>  | output current on pin Pn       |            | -         | ±50  | mA   |
| I <sub>CC</sub>     | supply current                 |            | -         | 85   | mA   |
| I <sub>GND</sub>    | ground supply current          |            | -         | 100  | mA   |
| P <sub>tot</sub>    | total power dissipation        |            | -         | 200  | mW   |
| T <sub>stg</sub>    | storage temperature            |            | -65       | +150 | °C   |
| T <sub>j(max)</sub> | maximum junction temperature   |            | -         | +125 | °C   |

9. Recommended operating conditions

Table 12. Operating conditions

| Symbol           | Parameter                 | Conditions            | Min                   | Max                   | Unit |
|------------------|---------------------------|-----------------------|-----------------------|-----------------------|------|
| V <sub>CC</sub>  | supply voltage            |                       | 1.65                  | 5.5                   | V    |
| V <sub>IH</sub>  | HIGH-level input voltage  | SCL, SDA              | 0.7 × V <sub>CC</sub> | 5.5                   | V    |
|                  |                           | P3 to P0              | 0.7 × V <sub>CC</sub> | 5.5                   | V    |
| V <sub>IL</sub>  | LOW-level input voltage   | SCL, SDA              | -0.5                  | 0.3 × V <sub>CC</sub> | V    |
|                  |                           | P3 to P0              | -0.5                  | 0.3 × V <sub>CC</sub> | V    |
| I <sub>OH</sub>  | HIGH-level output current | P3 to P0              | -                     | 10                    | mA   |
| I <sub>OL</sub>  | LOW-level output current  | P3 to P0              | -                     | 25                    | mA   |
| T <sub>amb</sub> | ambient temperature       | operating in free air | -40                   | +125                  | °C   |

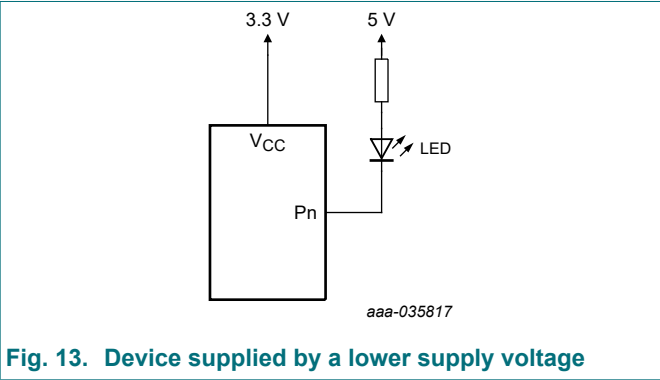
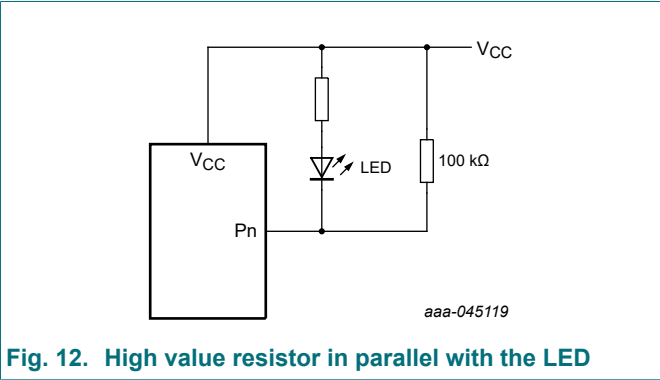
10. Application design-in information



10.1. Minimizing I<sub>CC</sub> when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V<sub>CC</sub> through a resistor as shown in Fig. 11. Since the LED acts as a diode, when the LED is off the I/O V<sub>I</sub> is about 1.2 V less than V<sub>CC</sub>. The supply current, I<sub>CC</sub>, increases as V<sub>I</sub> becomes lower than V<sub>CC</sub>.

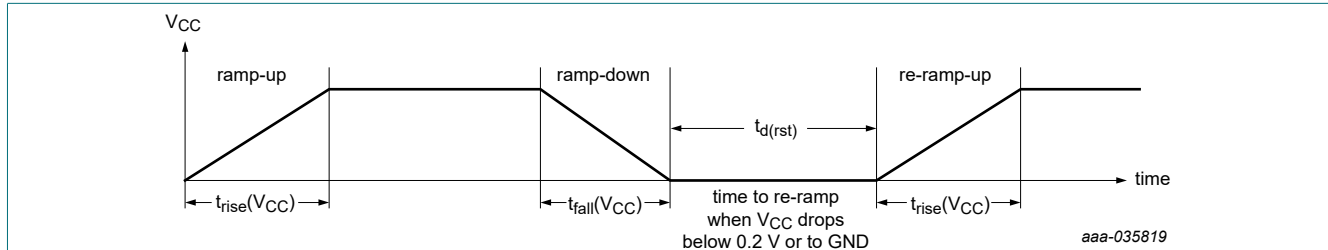
Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V<sub>CC</sub> when the LED is off. Fig. 12 shows a high value resistor in parallel with the LED. Fig. 13 shows V<sub>CC</sub> less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V<sub>I</sub> at or above V<sub>CC</sub> and prevents additional supply current consumption when the LED is off.



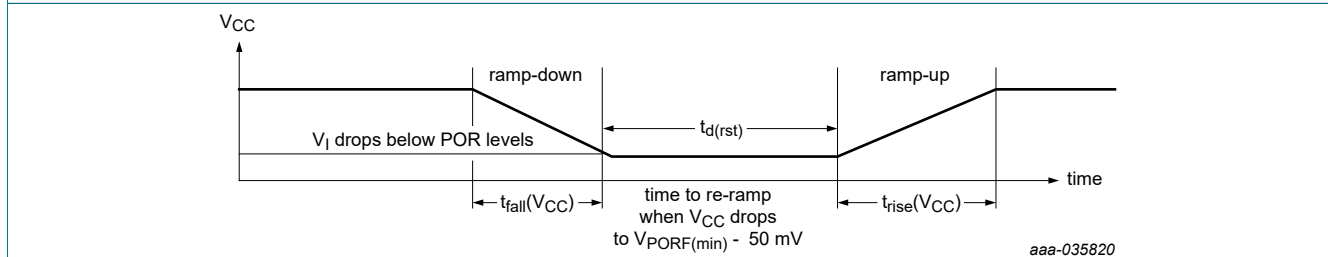
## 10.2. Power-on reset requirements

In the event of a glitch or data corruption, NCA9536 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Fig. 14](#) and [Fig. 15](#).



**Fig. 14.**  $V_{CC}$  is lowered below 0.2 V or to 0 V and then ramped up to  $V_{CC}$



**Fig. 15.**  $V_{CC}$  is lowered below the POR threshold, then ramped back up to  $V_{CC}$

[Table 13](#) specifies the performance of the power-on reset feature for NCA9536 for both types of power-on reset.

**Table 13. Recommended supply sequencing and ramp rates**

$T_{amb} = 25\text{ °C}$  (unless otherwise noted). Not tested; specified by design.

| Symbol              | Parameter                         | Condition                                                                                                    | $T_{amb} = 25\text{ °C}$ |     |      | Unit          |
|---------------------|-----------------------------------|--------------------------------------------------------------------------------------------------------------|--------------------------|-----|------|---------------|
|                     |                                   |                                                                                                              | Min                      | Typ | Max  |               |
| $t_{rise}(V_{CC})$  | supply ramp up time               | <a href="#">Fig. 14</a>                                                                                      | 0.1                      | -   | 2000 | ms            |
| $t_{fall}(V_{CC})$  | supply ramp down time             | <a href="#">Fig. 14</a>                                                                                      | 0.1                      | -   | 2000 | ms            |
| $t_{d(rst)}$        | reset delay time                  | <a href="#">Fig. 14</a> ; re-ramp time when $V_{CC}$ drops below 0.2 V or to GND                             | 1                        | -   | -    | $\mu\text{s}$ |
|                     |                                   | <a href="#">Fig. 15</a> ; re-ramp time when $V_{CC}$ drops to $V_{PORF(min)} - 50\text{ mV}$                 | 1                        | -   | -    | $\mu\text{s}$ |
| $\Delta V_{CC(gl)}$ | glitch supply voltage difference  | <a href="#">Fig. 16</a>                                                                                      | -                        | -   | 1    | V             |
| $V_{CC\_MIN(gl)}$   | minimum glitch supply voltage     | minimum voltage that $V_{CC}$ can glitch down to, but not cause functional disruption when $t_{w(gl)}V_{CC}$ | 1.5                      | -   | -    | V             |
| $t_{w(gl)}V_{CC}$   | supply voltage glitch pulse width | <a href="#">Fig. 16</a>                                                                                      | -                        | -   | 10   | $\mu\text{s}$ |

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $t_{w(gl)}V_{CC}$ ) and glitch height ( $\Delta V_{CC(gl)}$ ) are dependent on each other. The glitch on power supply should never go below  $V_{CC\_MIN(gl)}$  in order to properly guarantee functionality. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Fig. 16](#) and [Table 13](#) provide more information on how to measure these specifications.

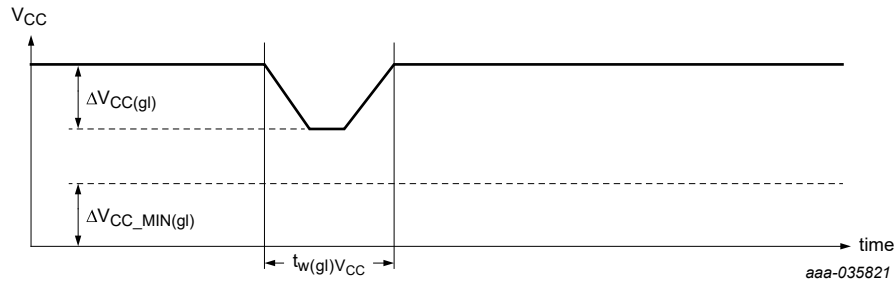
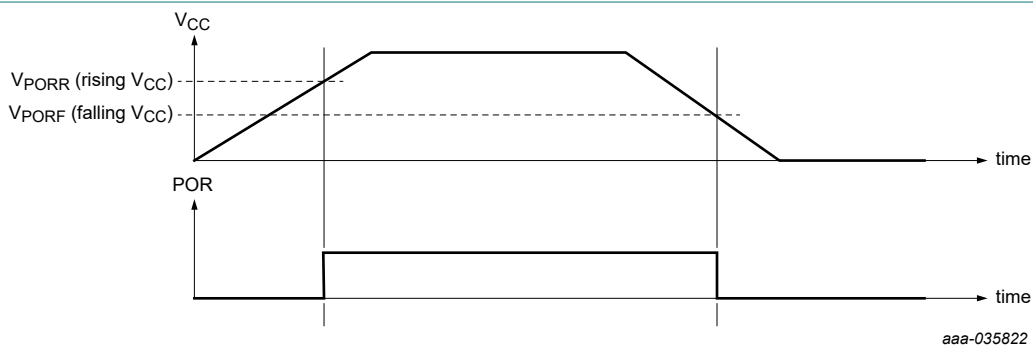


Fig. 16. Glitch width and glitch height

$V_{PORR}$  and  $V_{PORF}$  are critical to the power-on reset.  $V_{PORR}$  is the voltage level of  $V_{CC}$  at which the reset condition is released and all the registers and the I<sup>2</sup>C-bus/SMBus state machine are initialized to their default states.  $V_{PORF}$  is the voltage level of  $V_{CC}$  below which NCA9536 enters reset state. Fig. 17 and Table 14 provide more details on this specification.

Fig. 17. Power-on reset voltage ( $V_{POR}$ )

## 11. Static characteristics

Table 14. Static characteristics

$V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$ ; unless otherwise specified.

| Symbol     | Parameter                                   | Conditions                                                             | -40 °C to +85 °C |     |             | -40 °C to +125 °C |             | Unit |
|------------|---------------------------------------------|------------------------------------------------------------------------|------------------|-----|-------------|-------------------|-------------|------|
|            |                                             |                                                                        | Min              | Typ | Max         | Min               | Max         |      |
| $V_{IK}$   | input clamping voltage                      | $I_I = -18 \text{ mA}$                                                 | -1.2             | -   | -           | -1.2              | -           | V    |
| $V_{PORF}$ | power-on reset voltage;<br>$V_{CC}$ falling | $V_I = V_{CC}$ or GND; $I_O = 0 \text{ mA}$ [1]                        | 0.8              | 1.1 | -           | 0.8               | -           | V    |
| $V_{PORR}$ | power-on reset voltage;<br>$V_{CC}$ rising  | $V_I = V_{CC}$ or GND; $I_O = 0 \text{ mA}$ [1]                        | -                | 1.2 | 1.5         | -                 | 1.6         | V    |
| $V_{IH}$   | HIGH-level input voltage                    | SDA, SCL                                                               | $0.7V_{CC}$      | -   | -           | $0.7V_{CC}$       | -           | V    |
|            |                                             | P-port                                                                 | $0.7V_{CC}$      | -   | -           | $0.7V_{CC}$       | -           | V    |
| $V_{IL}$   | LOW-level input voltage                     | SDA, SCL                                                               | -                | -   | $0.3V_{CC}$ | -                 | $0.3V_{CC}$ | V    |
|            |                                             | P-port                                                                 | -                | -   | $0.3V_{CC}$ | -                 | $0.3V_{CC}$ | V    |
| $I_{OL}$   | LOW-level output current                    | $V_{OL} = 0.4 \text{ V}$ ; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$ |                  |     |             |                   |             |      |
|            |                                             | SDA                                                                    | 20               | -   | -           | 20                | -           | mA   |
|            |                                             | P3 configured as INT [2]                                               | 4                | -   | -           | 4                 | -           | mA   |
|            |                                             | P port [3]                                                             |                  |     |             |                   |             |      |
|            |                                             | $V_{OL} = 0.5 \text{ V}$ ; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$ | 8                | -   | -           | 8                 | -           | mA   |
|            |                                             | $V_{OL} = 0.7 \text{ V}$ ; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$ | 10               | -   | -           | 10                | -           | mA   |

4-bit I<sup>2</sup>C and SMBus low-power I/O expander with configurable registers and interrupt

| Symbol          | Parameter                 | Conditions                                                                  | -40 °C to +85 °C |     |      | -40 °C to +125 °C |      | Unit |
|-----------------|---------------------------|-----------------------------------------------------------------------------|------------------|-----|------|-------------------|------|------|
|                 |                           |                                                                             | Min              | Typ | Max  | Min               | Max  |      |
| V <sub>OH</sub> | HIGH-level output voltage | P port [4]                                                                  |                  |     |      |                   |      |      |
|                 |                           | I <sub>OH</sub> = -8 mA; V <sub>CC</sub> = 1.65 V                           | 1.2              | -   | -    | 1.2               | -    | V    |
|                 |                           | I <sub>OH</sub> = -10 mA; V <sub>CC</sub> = 1.65 V                          | 1.1              | -   | -    | 1                 | -    | V    |
|                 |                           | I <sub>OH</sub> = -8 mA; V <sub>CC</sub> = 2.3 V                            | 1.8              | -   | -    | 1.8               | -    | V    |
|                 |                           | I <sub>OH</sub> = -10 mA; V <sub>CC</sub> = 2.3 V                           | 1.7              | -   | -    | 1.7               | -    | V    |
|                 |                           | I <sub>OH</sub> = -8 mA; V <sub>CC</sub> = 3.0 V                            | 2.6              | -   | -    | 2.6               | -    | V    |
|                 |                           | I <sub>OH</sub> = -10 mA; V <sub>CC</sub> = 3.0 V                           | 2.5              | -   | -    | 2.5               | -    | V    |
|                 |                           | I <sub>OH</sub> = -8 mA; V <sub>CC</sub> = 4.5 V                            | 4.1              | -   | -    | 4.1               | -    | V    |
|                 |                           | I <sub>OH</sub> = -10 mA; V <sub>CC</sub> = 4.5 V                           | 4.0              | -   | -    | 4.0               | -    | V    |
|                 |                           | I <sub>OH</sub> = -8 mA; V <sub>CC</sub> = 4.75 V                           | 4.1              | -   | -    | 4.1               | -    | V    |
|                 |                           | I <sub>OH</sub> = -10 mA; V <sub>CC</sub> = 4.75 V                          | 4.0              | -   | -    | 4.0               | -    | V    |
| V <sub>OL</sub> | LOW-level output voltage  | P port; I <sub>OL</sub> = 8 mA                                              |                  |     |      |                   |      |      |
|                 |                           | V <sub>CC</sub> = 1.65 V                                                    | -                | -   | 0.45 | -                 | 0.45 | V    |
|                 |                           | V <sub>CC</sub> = 2.3 V                                                     | -                | -   | 0.30 | -                 | 0.30 | V    |
|                 |                           | V <sub>CC</sub> = 3.0 V                                                     | -                | -   | 0.25 | -                 | 0.25 | V    |
|                 |                           | V <sub>CC</sub> = 4.5 V                                                     | -                | -   | 0.2  | -                 | 0.2  | V    |
| I <sub>I</sub>  | input current             | V <sub>CC</sub> = 1.65 V to 5.5 V                                           |                  |     |      |                   |      |      |
|                 |                           | SCL, SDA; V <sub>I</sub> = V <sub>CC</sub> or GND                           | -                | 0   | ±1   | -                 | ±1   | µA   |
|                 |                           | P-port                                                                      |                  |     |      |                   |      |      |
|                 |                           | V <sub>I</sub> = V <sub>CC</sub> ; V <sub>CC</sub> = 1.65 V to 5.5 V        | -                | 0   | ±1   | -                 | ±1   | µA   |
|                 |                           | V <sub>I</sub> = 5.5 V; V <sub>CC</sub> = 0 V                               | -                | 0   | ±1   | -                 | ±2   | µA   |
|                 |                           | Pull-up disabled<br>V <sub>I</sub> = GND; V <sub>CC</sub> = 1.65 V to 5.5 V | -                | 0   | ±1   | -                 | ±1   | µA   |
|                 |                           | Pull-up enabled<br>V <sub>I</sub> = GND; V <sub>CC</sub> = 1.65 V to 5.5 V  | -100             | -40 | -    | -100              | -    | µA   |

4-bit I<sup>2</sup>C and SMBus low-power I/O expander with configurable registers and interrupt

| Symbol           | Parameter                           | Conditions                                                                                                                                        | -40 °C to +85 °C |     |     | -40 °C to +125 °C |     | Unit |
|------------------|-------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|------------------|-----|-----|-------------------|-----|------|
|                  |                                     |                                                                                                                                                   | Min              | Typ | Max | Min               | Max |      |
| I <sub>CC</sub>  | supply current                      | <b>Operating mode (Pull-up disabled)</b><br>V <sub>I</sub> = V <sub>CC</sub> ; I/O = inputs; f <sub>SCL</sub> = 400 kHz (t <sub>r</sub> = 300 ns) |                  |     |     |                   |     |      |
|                  |                                     | V <sub>CC</sub> = 5.5 V                                                                                                                           | -                | 25  | 40  | -                 | 40  | μA   |
|                  |                                     | V <sub>CC</sub> = 3.6 V                                                                                                                           | -                | 10  | 15  | -                 | 15  | μA   |
|                  |                                     | V <sub>CC</sub> = 2.7 V                                                                                                                           | -                | 5   | 10  | -                 | 10  | μA   |
|                  |                                     | V <sub>CC</sub> = 1.95 V                                                                                                                          | -                | 3   | 5   | -                 | 5   | μA   |
|                  |                                     | <b>Operating mode (Pull-up enabled)</b><br>V <sub>I</sub> = GND; I/O = inputs; f <sub>SCL</sub> = 400 kHz (t <sub>r</sub> = 300 ns)               |                  |     |     |                   |     |      |
|                  |                                     | V <sub>CC</sub> = 5.5 V                                                                                                                           | -                | 225 | 390 | -                 | 390 | μA   |
|                  |                                     | V <sub>CC</sub> = 3.6 V                                                                                                                           | -                | 175 | 280 | -                 | 280 | μA   |
|                  |                                     | V <sub>CC</sub> = 2.7 V                                                                                                                           | -                | 125 | 200 | -                 | 200 | μA   |
|                  |                                     | V <sub>CC</sub> = 1.95 V                                                                                                                          | -                | 100 | 150 | -                 | 150 | μA   |
|                  |                                     | <b>Operating mode (Pull-up disabled)</b><br>V <sub>I</sub> = V <sub>CC</sub> ; f <sub>SCL</sub> = 1 MHz (t <sub>r</sub> = 120 ns)                 |                  |     |     |                   |     |      |
|                  |                                     | V <sub>CC</sub> = 5.5 V                                                                                                                           | -                | 45  | 60  | -                 | 60  | μA   |
|                  |                                     | V <sub>CC</sub> = 3.6 V                                                                                                                           | -                | 17  | 23  | -                 | 23  | μA   |
|                  |                                     | V <sub>CC</sub> = 2.7 V                                                                                                                           | -                | 9   | 13  | -                 | 13  | μA   |
|                  |                                     | V <sub>CC</sub> = 1.95 V                                                                                                                          | -                | 5   | 8   | -                 | 8   | μA   |
|                  |                                     | <b>Operating mode (Pull-up enabled)</b><br>V <sub>I</sub> = GND; I/O = inputs; f <sub>SCL</sub> = 1 MHz (t <sub>r</sub> = 120 ns)                 |                  |     |     |                   |     |      |
|                  |                                     | V <sub>CC</sub> = 5.5 V                                                                                                                           | -                | 225 | 425 | -                 | 425 | μA   |
|                  |                                     | V <sub>CC</sub> = 3.6 V                                                                                                                           | -                | 175 | 250 | -                 | 250 | μA   |
|                  |                                     | V <sub>CC</sub> = 2.7 V                                                                                                                           | -                | 125 | 200 | -                 | 200 | μA   |
|                  |                                     | V <sub>CC</sub> = 1.95 V                                                                                                                          | -                | 100 | 150 | -                 | 150 | μA   |
|                  |                                     | <b>Standby mode</b><br>V <sub>I</sub> = V <sub>CC</sub> ; I/O = inputs; f <sub>SCL</sub> = 0 Hz                                                   |                  |     |     |                   |     |      |
|                  |                                     | V <sub>CC</sub> = 5.5 V                                                                                                                           | -                | 1.5 | 3   | -                 | 3.3 | μA   |
|                  |                                     | V <sub>CC</sub> = 3.6 V                                                                                                                           | -                | 0.9 | 1.8 | -                 | 2   | μA   |
|                  |                                     | V <sub>CC</sub> = 2.7 V                                                                                                                           | -                | 0.6 | 1.4 | -                 | 1.6 | μA   |
|                  |                                     | V <sub>CC</sub> = 1.95 V                                                                                                                          | -                | 0.6 | 1   | -                 | 1.1 | μA   |
|                  |                                     | <b>Standby mode (Pull-up enabled)</b><br>V <sub>I</sub> = GND; I/O = inputs; f <sub>SCL</sub> = 0 Hz                                              |                  |     |     |                   |     |      |
|                  |                                     | V <sub>CC</sub> = 5.5 V                                                                                                                           | -                | 225 | 350 | -                 | 370 | μA   |
|                  |                                     | V <sub>CC</sub> = 3.6 V                                                                                                                           | -                | 175 | 250 | -                 | 250 | μA   |
|                  |                                     | V <sub>CC</sub> = 2.7 V                                                                                                                           | -                | 125 | 200 | -                 | 200 | μA   |
|                  |                                     | V <sub>CC</sub> = 1.95 V                                                                                                                          | -                | 100 | 150 | -                 | 150 | μA   |
| ΔI <sub>CC</sub> | additional quiescent supply current | SCL, SDA; one input at V <sub>CC</sub> - 0.6 V, other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 1.65 V to 5.5 V                         | -                | -   | 5   | -                 | 10  | μA   |
|                  |                                     | P-port ; one input at V <sub>CC</sub> - 0.6 V, other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 1.65 V to 5.5 V                          | -                | -   | 12  | -                 | 18  | μA   |
| C <sub>i</sub>   | input capacitance                   | SCL; V <sub>CC</sub> = 1.65 V to 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND                                                                   | -                | 1.5 | 2.5 | -                 | 3.5 | pF   |

4-bit I<sup>2</sup>C and SMBus low-power I/O expander with configurable registers and interrupt

| Symbol          | Parameter                | Conditions                                                                              | -40 °C to +85 °C |     |     | -40 °C to +125 °C |     | Unit |
|-----------------|--------------------------|-----------------------------------------------------------------------------------------|------------------|-----|-----|-------------------|-----|------|
|                 |                          |                                                                                         | Min              | Typ | Max | Min               | Max |      |
| C <sub>io</sub> | input/output capacitance | SDA; V <sub>CC</sub> = 1.65 V to 5.5 V;<br>V <sub>I/O</sub> = V <sub>CC</sub> or GND    | -                | 5   | 6   | -                 | 7   | pF   |
|                 |                          | P port; V <sub>CC</sub> = 1.65 V to 5.5 V;<br>V <sub>I/O</sub> = V <sub>CC</sub> or GND | -                | 3   | 4.5 | -                 | 5   | pF   |

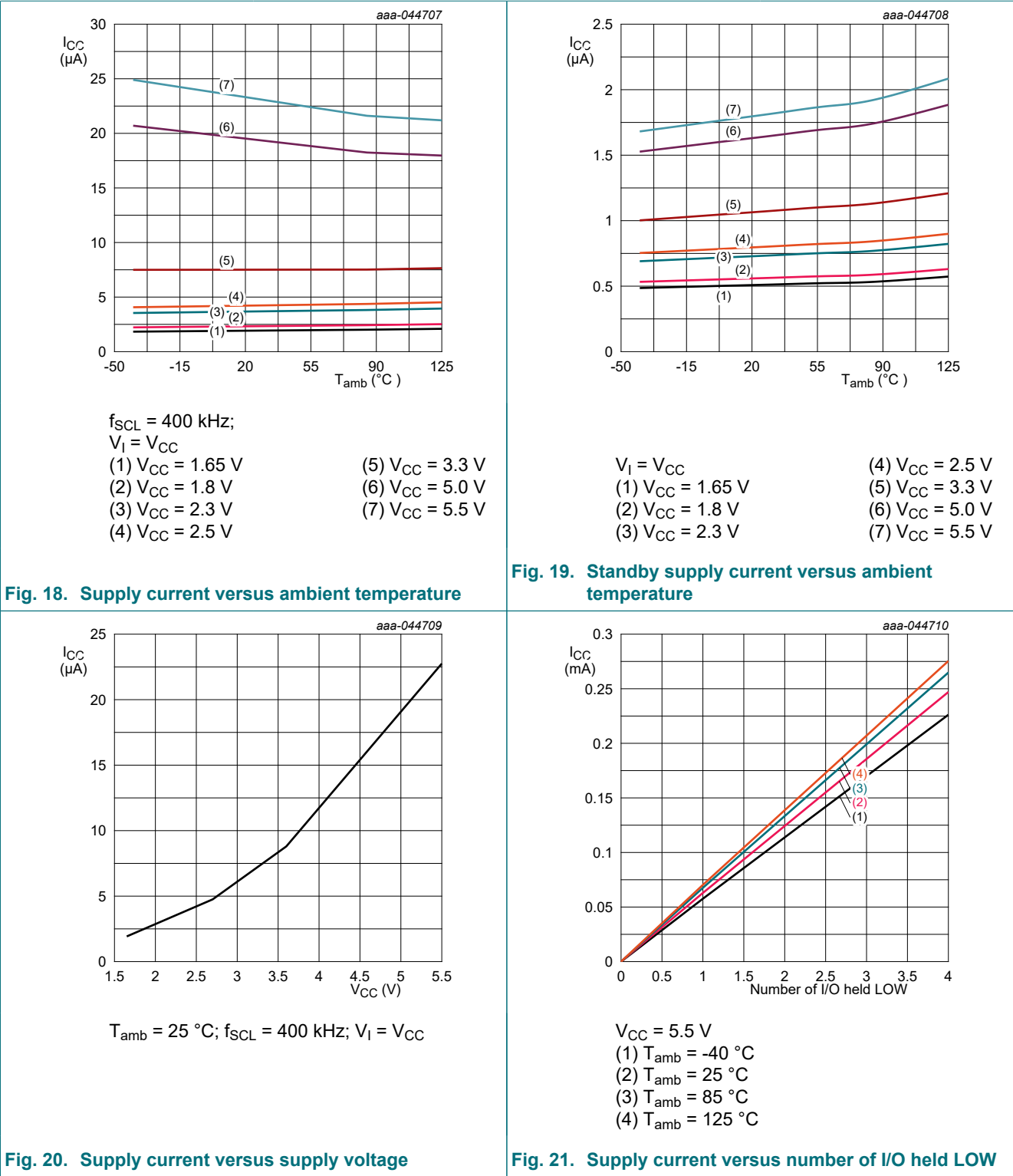
[1] V<sub>CC</sub> must be lowered to 0.2 V in order to reset part.

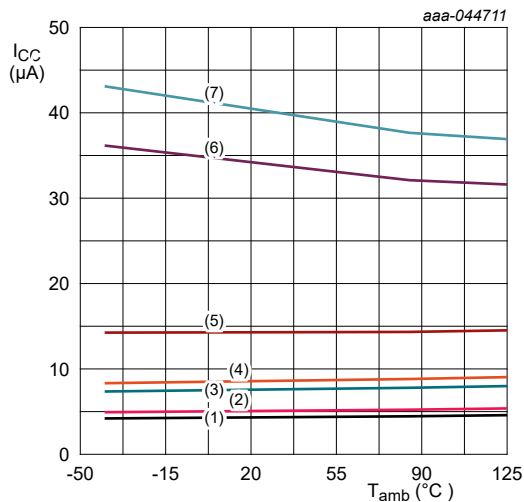
[2] P3 can be repurposed as  $\overline{\text{INT}}$  (open-drain interrupt output) in the special function register.

[3] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

[4] The total current sourced by all I/Os must be limited to 85 mA.

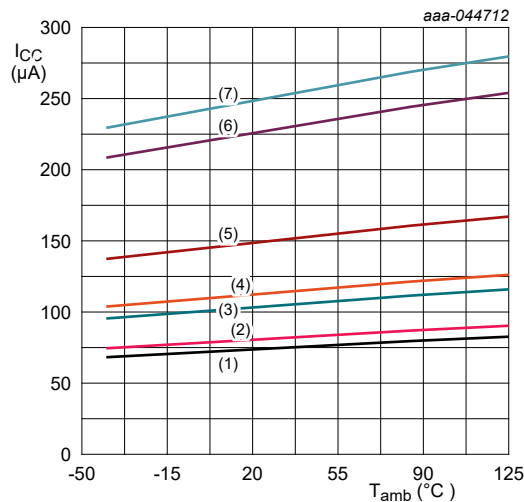
11.1. Typical characteristics





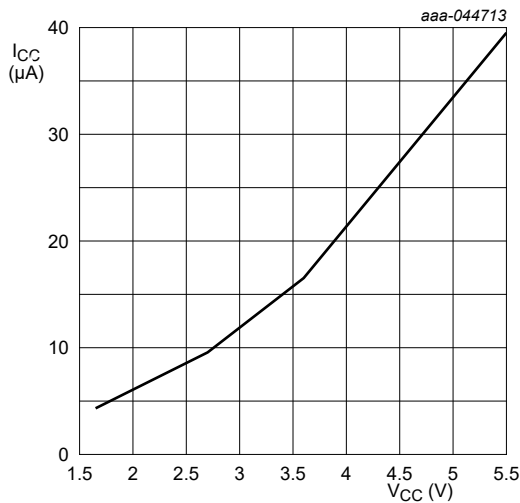
$f_{SCL} = 1$  MHz;  
 $V_I = V_{CC}$   
(1)  $V_{CC} = 1.65$  V  
(2)  $V_{CC} = 1.8$  V  
(3)  $V_{CC} = 2.3$  V  
(4)  $V_{CC} = 2.5$  V  
(5)  $V_{CC} = 3.3$  V  
(6)  $V_{CC} = 5.0$  V  
(7)  $V_{CC} = 5.5$  V

Fig. 22. Supply current versus ambient temperature



$V_I = GND$   
(1)  $V_{CC} = 1.65$  V  
(2)  $V_{CC} = 1.8$  V  
(3)  $V_{CC} = 2.3$  V  
(4)  $V_{CC} = 2.5$  V  
(5)  $V_{CC} = 3.3$  V  
(6)  $V_{CC} = 5.0$  V  
(7)  $V_{CC} = 5.5$  V

Fig. 23. Standby supply current versus ambient temperature



$T_{amb} = 25$  °C;  $f_{SCL} = 1$  MHz;  $V_I = V_{CC}$

Fig. 24. Supply current versus supply voltage

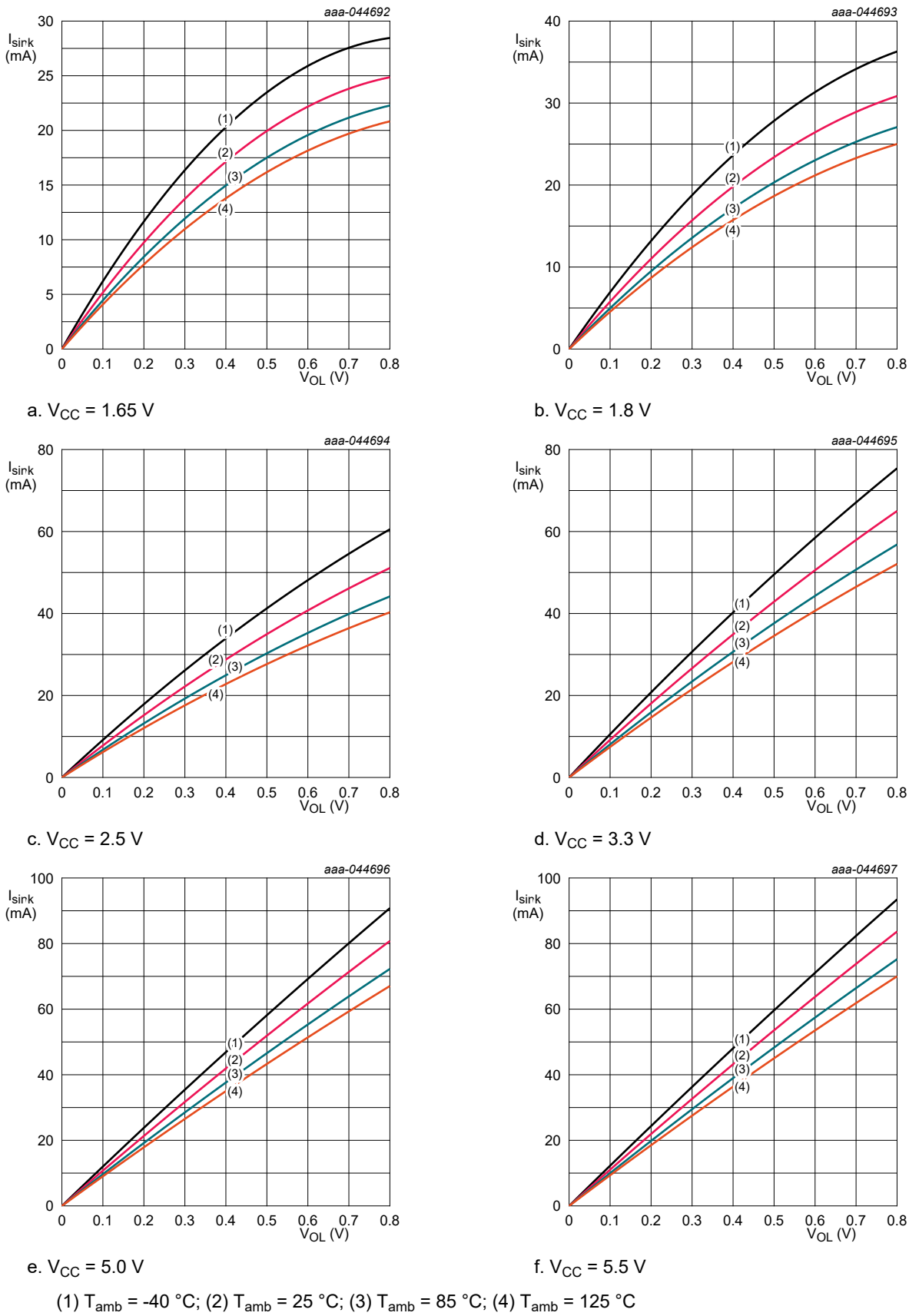
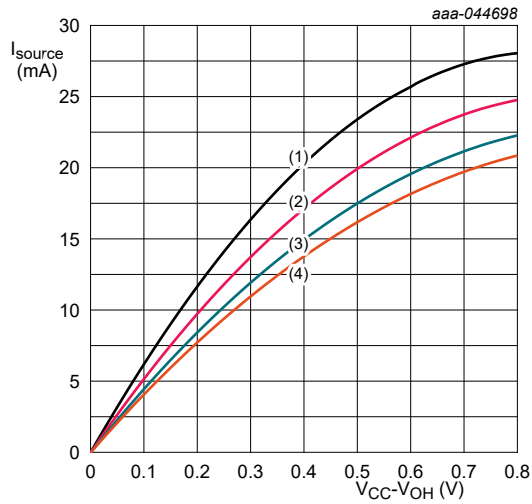
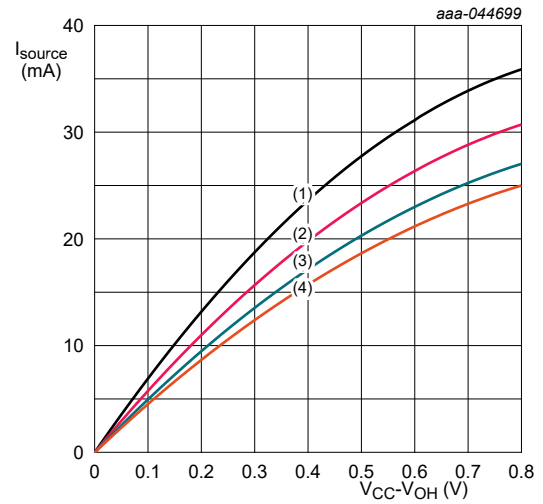
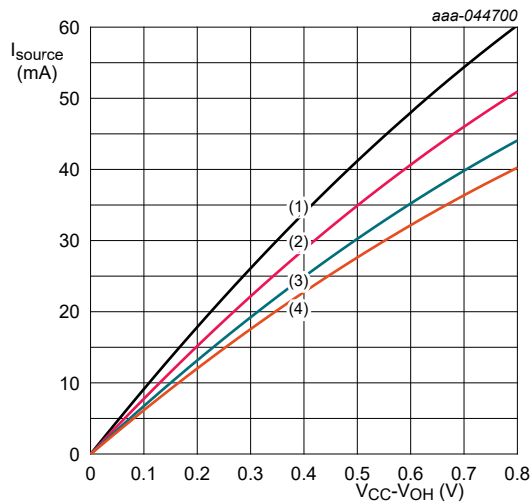
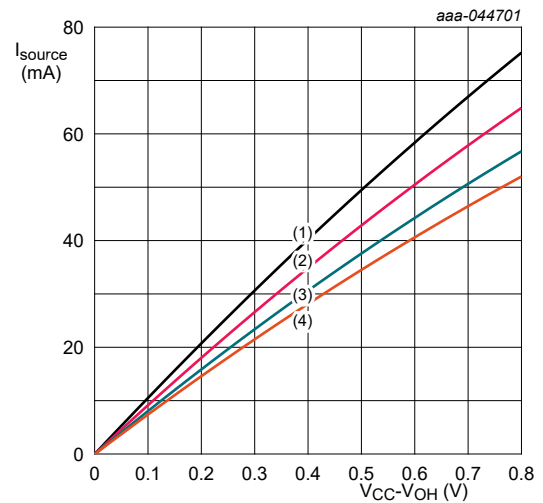
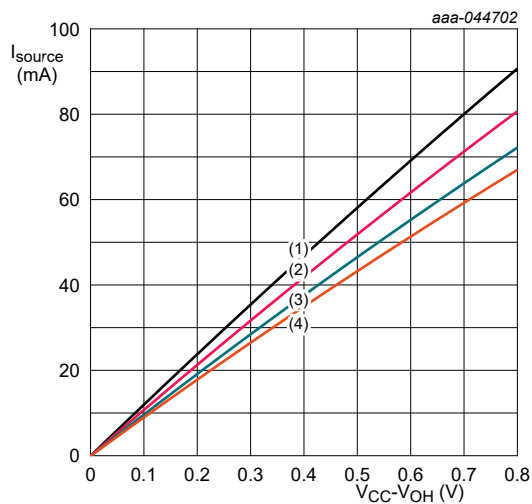
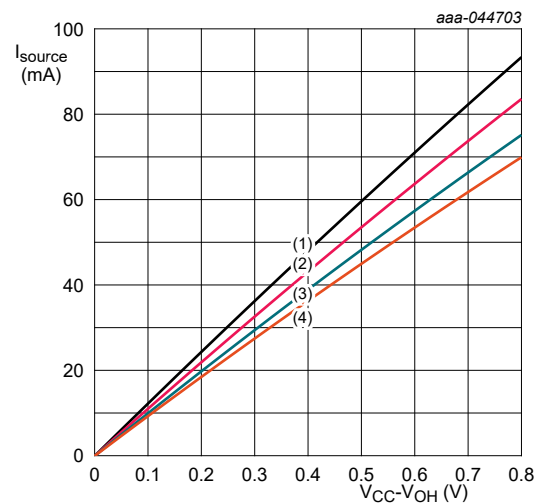
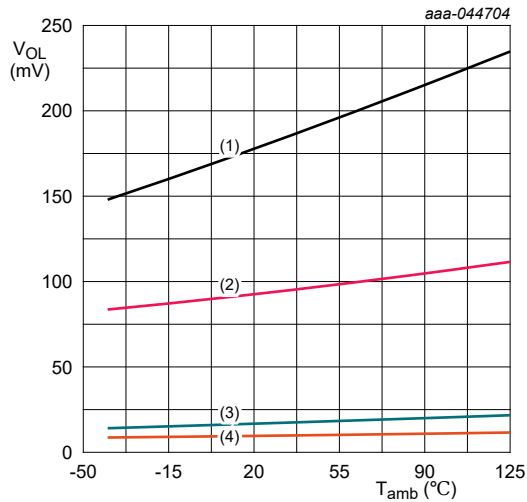


Fig. 25. I/O sink current versus LOW-level output voltage

a.  $V_{\text{CC}} = 1.65 \text{ V}$ b.  $V_{\text{CC}} = 1.8 \text{ V}$ c.  $V_{\text{CC}} = 2.5 \text{ V}$ d.  $V_{\text{CC}} = 3.3 \text{ V}$ e.  $V_{\text{CC}} = 5.0 \text{ V}$ f.  $V_{\text{CC}} = 5.5 \text{ V}$ 

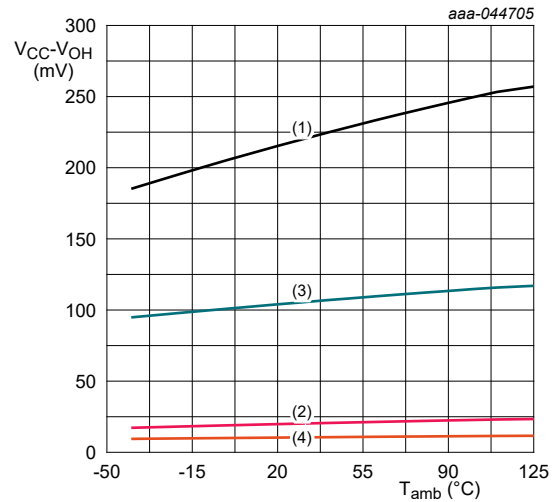
(1)  $T_{\text{amb}} = -40 \text{ }^{\circ}\text{C}$ ; (2)  $T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$ ; (3)  $T_{\text{amb}} = 85 \text{ }^{\circ}\text{C}$ ; (4)  $T_{\text{amb}} = 125 \text{ }^{\circ}\text{C}$

Fig. 26. I/O source current versus HIGH-level output voltage

4-bit I<sup>2</sup>C and SMBus low-power I/O expander with configurable registers and interrupt

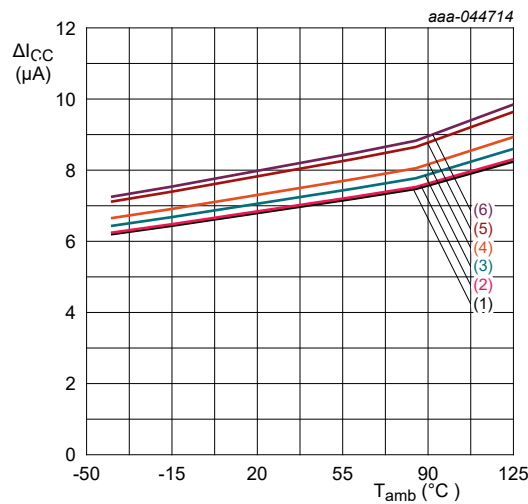
- (1)  $V_{CC} = 1.8\text{ V}$ ;  $I_{\text{sink}} = 10\text{ mA}$   
 (2)  $V_{CC} = 5\text{ V}$ ;  $I_{\text{sink}} = 10\text{ mA}$   
 (3)  $V_{CC} = 1.8\text{ V}$ ;  $I_{\text{sink}} = 1\text{ mA}$   
 (4)  $V_{CC} = 5\text{ V}$ ;  $I_{\text{sink}} = 1\text{ mA}$

Fig. 27. LOW-level output voltage versus temperature



- (1)  $V_{CC} = 1.8\text{ V}$ ;  $I_{\text{source}} = -10\text{ mA}$   
 (2)  $V_{CC} = 5\text{ V}$ ;  $I_{\text{source}} = -10\text{ mA}$   
 (3)  $V_{CC} = 1.8\text{ V}$ ;  $I_{\text{source}} = -1\text{ mA}$   
 (4)  $V_{CC} = 5\text{ V}$ ;  $I_{\text{source}} = -1\text{ mA}$

Fig. 28. I/O high voltage versus temperature



$$V_I = V_{CC} - 0.6\text{ V}$$

- (1)  $V_{CC} = 1.65\text{ V}$ ; (2)  $V_{CC} = 1.8\text{ V}$ ; (3)  $V_{CC} = 2.5\text{ V}$ ;  
 (4)  $V_{CC} = 3.3\text{ V}$ ; (5)  $V_{CC} = 5.0\text{ V}$ ; (6)  $V_{CC} = 5.5\text{ V}$

Fig. 29. Additional quiescent supply current versus temperature

## 12. Dynamic characteristics

Table 15. Dynamic characteristics

| Symbol              | Parameter                                                         | Conditions                             | Standard-mode I <sup>2</sup> C-bus |      | Fast-mode I <sup>2</sup> C-bus |     | Fast-mode plus I <sup>2</sup> C-bus |      | Unit |
|---------------------|-------------------------------------------------------------------|----------------------------------------|------------------------------------|------|--------------------------------|-----|-------------------------------------|------|------|
|                     |                                                                   |                                        | Min                                | Max  | Min                            | Max | Min                                 | Max  |      |
| f <sub>SCL</sub>    | SCL clock frequency                                               |                                        | 0                                  | 100  | 0                              | 400 | 0                                   | 1000 | kHz  |
| t <sub>BUF</sub>    | bus free time between a STOP and START condition                  |                                        | 4.7                                | -    | 1.3                            | -   | 0.5                                 | -    | µs   |
| t <sub>HD;STA</sub> | hold time (repeated) START condition                              |                                        | 4.0                                | -    | 0.6                            | -   | 0.26                                | -    | µs   |
| t <sub>SU;STA</sub> | set-up time for a repeated START condition                        |                                        | 4.7                                | -    | 0.6                            | -   | 0.26                                | -    | µs   |
| t <sub>SU;STO</sub> | set-up time for STOP condition                                    |                                        | 4.0                                | -    | 0.6                            | -   | 0.26                                | -    | µs   |
| t <sub>HD;DAT</sub> | data hold time                                                    |                                        | 0                                  | -    | 0                              | -   | 0                                   | -    | µs   |
| t <sub>VD;ACK</sub> | data valid acknowledge time                                       | [1]                                    | 0.3                                | 3.45 | 0.1                            | 0.9 | -                                   | 0.45 | µs   |
| t <sub>VD;DAT</sub> | data valid time                                                   | [2]                                    | -                                  | 3.45 | -                              | 0.9 | -                                   | 0.45 | µs   |
| t <sub>SU;DAT</sub> | data set-up time                                                  |                                        | 250                                | -    | 100                            | -   | 50                                  | -    | ns   |
| t <sub>LOW</sub>    | LOW period of the SCL clock                                       |                                        | 4.7                                | -    | 1.3                            | -   | 0.5                                 | -    | µs   |
| t <sub>HIGH</sub>   | HIGH period of the SCL clock                                      |                                        | 4.0                                | -    | 0.6                            | -   | 0.26                                | -    | µs   |
| t <sub>r</sub>      | rise time of both SDA and SCL signals                             |                                        | -                                  | 1000 | 20xV <sub>CC</sub> /5.5 V      | 300 | 20xV <sub>CC</sub> /5.5 V           | 120  | ns   |
| t <sub>f</sub>      | fall time of both SDA and SCL signals                             |                                        | -                                  | 300  | 20xV <sub>CC</sub> /5.5 V      | 300 | 20xV <sub>CC</sub> /5.5 V           | 120  | ns   |
| t <sub>SP</sub>     | pulse width of spikes that must be suppressed by the input filter |                                        | -                                  | 50   | -                              | 50  | -                                   | 50   | ns   |
| <b>Device</b>       |                                                                   |                                        |                                    |      |                                |     |                                     |      |      |
| t <sub>READY</sub>  | Power on to start condition time                                  |                                        | 10                                 | -    | 10                             | -   | 10                                  | -    | µs   |
| <b>Port timing</b>  |                                                                   |                                        |                                    |      |                                |     |                                     |      |      |
| t <sub>v(Q)</sub>   | data output valid time                                            | SCL to P-port; V <sub>CC</sub> ≥ 2.3 V | -                                  | 200  | -                              | 200 | -                                   | 200  | ns   |
|                     |                                                                   | SCL to P-port; V <sub>CC</sub> < 2.3 V | -                                  | 350  | -                              | 350 | -                                   | 350  | ns   |
| t <sub>su(D)</sub>  | data input set-up time                                            | P-port to SCL                          | -50                                | -    | -50                            | -   | -50                                 | -    | ns   |
| t <sub>h(D)</sub>   | data input hold time                                              | P-port to SCL                          | 300                                | -    | 300                            | -   | 300                                 | -    | ns   |

4-bit I<sup>2</sup>C and SMBus low-power I/O expander with configurable registers and interrupt

| Symbol                | Parameter                                 | Conditions | Standard-mode I <sup>2</sup> C-bus |     | Fast-mode I <sup>2</sup> C-bus |     | Fast-mode plus I <sup>2</sup> C-bus |     | Unit |
|-----------------------|-------------------------------------------|------------|------------------------------------|-----|--------------------------------|-----|-------------------------------------|-----|------|
|                       |                                           |            | Min                                | Max | Min                            | Max | Min                                 | Max |      |
| Interrupt timing      |                                           |            |                                    |     |                                |     |                                     |     |      |
| t <sub>v(INT)</sub>   | valid time on pin $\overline{\text{INT}}$ |            | -                                  | 1   | -                              | 1   | -                                   | 1   | μs   |
| t <sub>rst(INT)</sub> | reset time on pin $\overline{\text{INT}}$ |            | -                                  | 1   | -                              | 1   | -                                   | 1   | μs   |

- [1]  $t_{VD,ACK}$  = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.  
[2]  $t_{VD,DAT}$  = minimum time for SDA data output to be valid following SCL LOW.

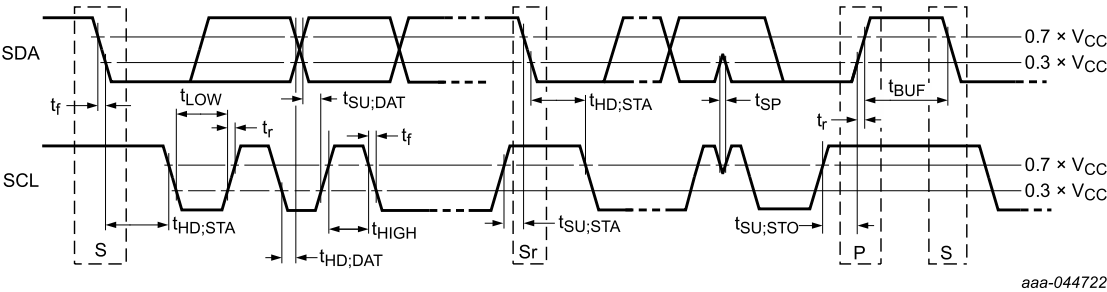
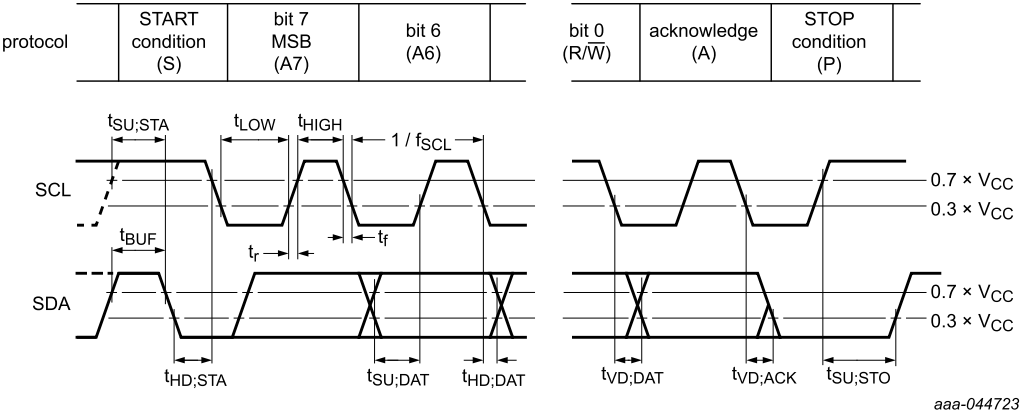


Fig. 30. Definition of timing

4-bit I<sup>2</sup>C and SMBus low-power I/O expander with configurable registers and interrupt



Rise and fall times refer to  $V_{IL}$  and  $V_{IH}$

Fig. 31. I<sup>2</sup>C-bus timing diagram

13. Test information

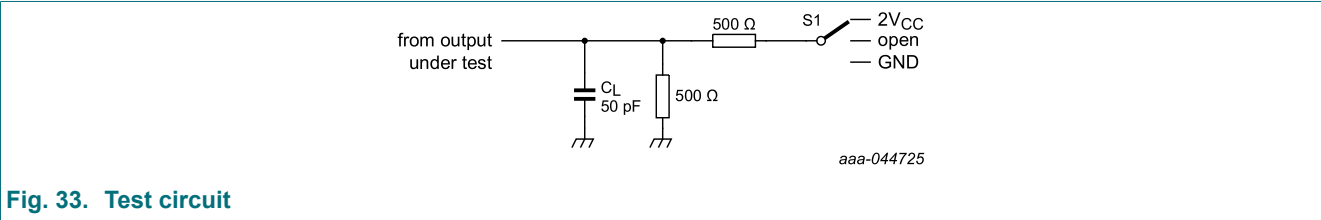
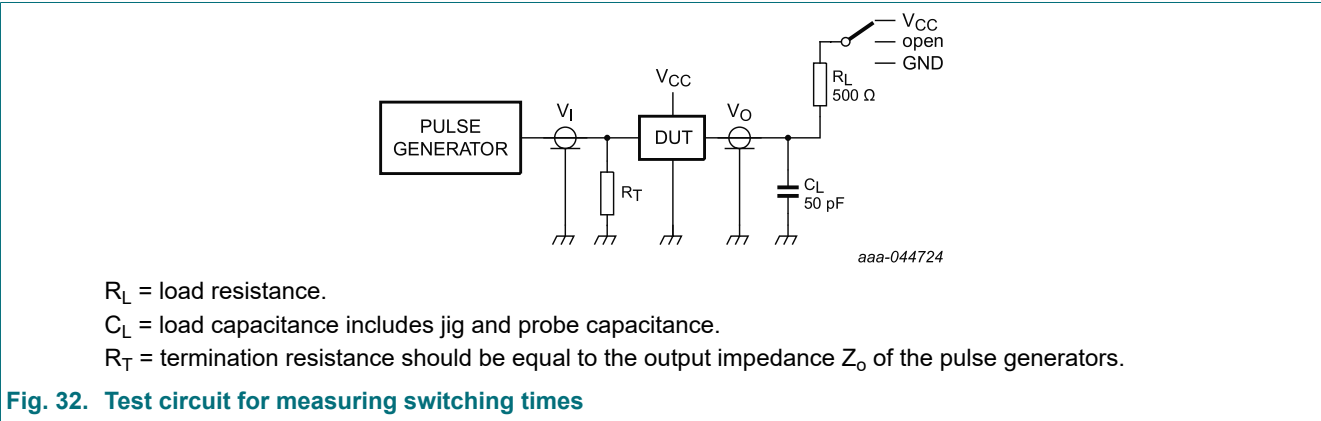


Table 16. Test data

| Test       | Load  |       | Switch    |
|------------|-------|-------|-----------|
|            | $C_L$ | $R_L$ |           |
| $t_{V(Q)}$ | 50 pF | 500 Ω | $2V_{CC}$ |

14. Package outline

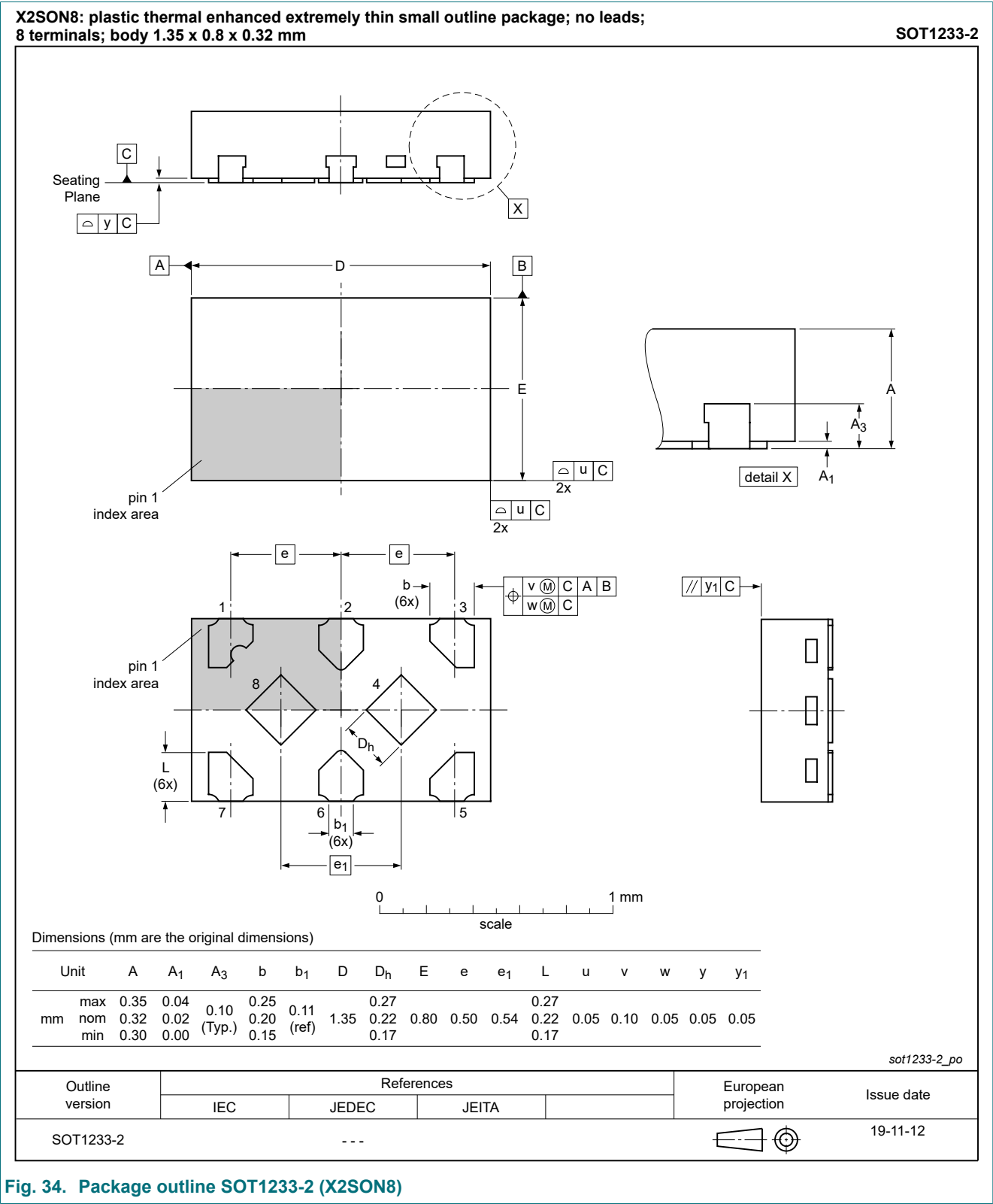


Fig. 34. Package outline SOT1233-2 (X2SON8)

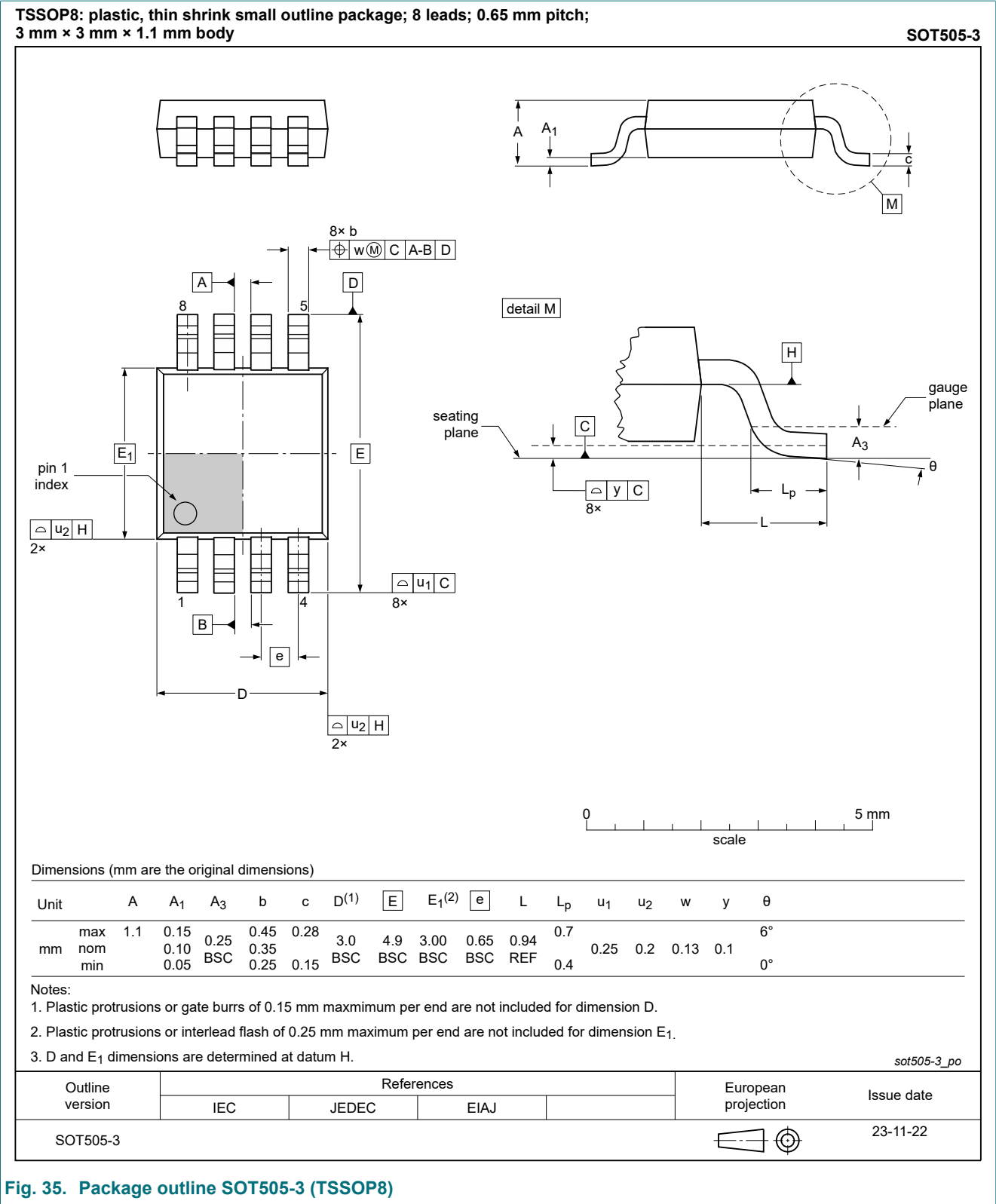


Fig. 35. Package outline SOT505-3 (TSSOP8)

## 15. Abbreviations

Table 17. Abbreviations

| Acronym          | Description              |
|------------------|--------------------------|
| CDM              | Charged Device Model     |
| DUT              | Device Under Test        |
| ESD              | ElectroStatic Discharge  |
| FET              | Field Effect Transistor  |
| HBM              | Human Body Model         |
| I <sup>2</sup> C | Inter-Integrated Circuit |
| PCB              | Printed Circuit Board    |
| PMBus            | Power Management Bus     |
| PRR              | Pulse Rate Repetition    |
| SMBus            | System Management Bus    |

## 16. Revision history

Table 18. Revision history

| Document ID | Release date | Data sheet status  | Change notice | Supersedes |
|-------------|--------------|--------------------|---------------|------------|
| NCA9536 v.1 | 20260304     | Product data sheet | -             | -          |

## 17. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 4 March 2026