



PSMN2R0-60PSR

N-channel 60 V, 2.2 m Ω standard level MOSFET in TO-220 using Trench Technology

25 June 2014

Product data sheet

1. General description

Standard level gate drive N-channel enhancement mode MOSFET in TO-220 package using advanced TrenchMOS technology. This product has been designed and qualified to 175 °C for use in a wide range of industrial, communications and Power Supply Equipment.

2. Features and benefits

- Low Q_G , Q_{GD} and Q_{OSS} for high system efficiency
- High reliability TO-220 package
- Qualified to 175 °C
- Reflow solderable

3. Applications

- Server and Telecom voltage regulator
- DC-to-DC, POL and System Power
- Motor Control
- Power OR-ing
- Sync Rectifier
- Load switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$		-	-	60	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 2	[1]	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	338	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	[2]	-	1.8	2.2	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 100\text{ °C}$; Fig. 12 ; Fig. 13		-	3	3.5	m Ω



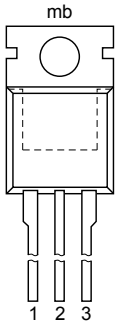
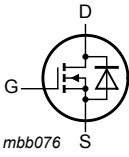
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 75\text{ A}; V_{DS} = 30\text{ V};$	-	32	45	nC
$Q_{G(tot)}$	total gate charge	Fig. 14 ; Fig. 15	-	137	192	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; I_D = 120\text{ A}; V_{sup} \leq 60\text{ V}; R_{GS} = 50\text{ }\Omega;$ Unclamped	-	-	913	mJ

- [1] Continuous current limited by package
- [2] Measured 3 mm from package.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>TO-220AB (SOT78)</p>	 <p>mbb076</p>
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R0-60PSR	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

7. Limiting values

Table 4. Limiting values

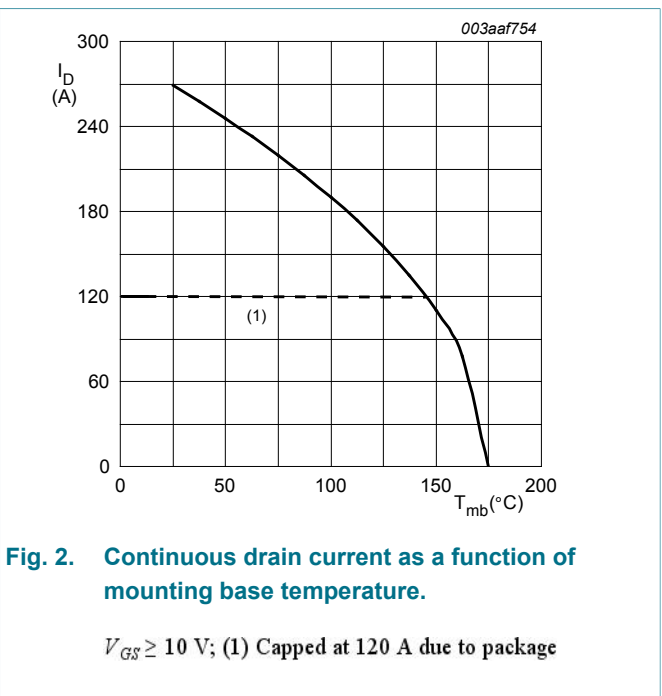
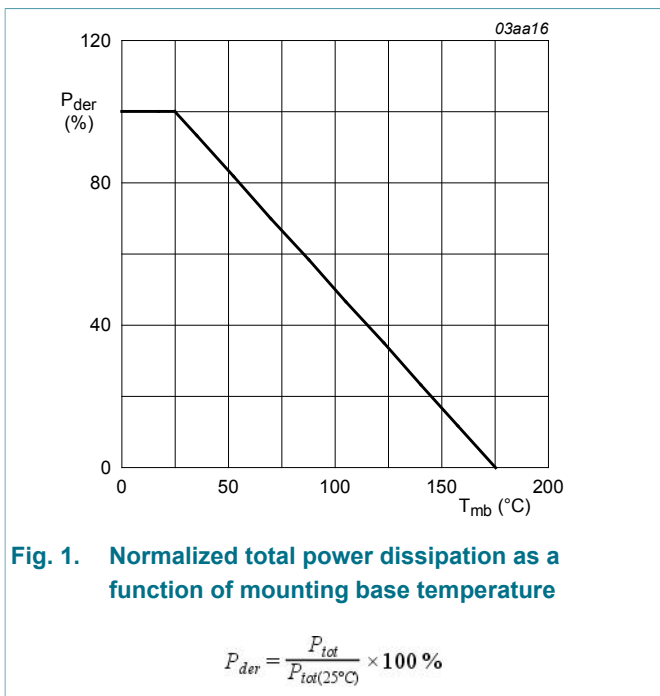
In accordance with the Absolute Maximum Rating System (IEC 60134).

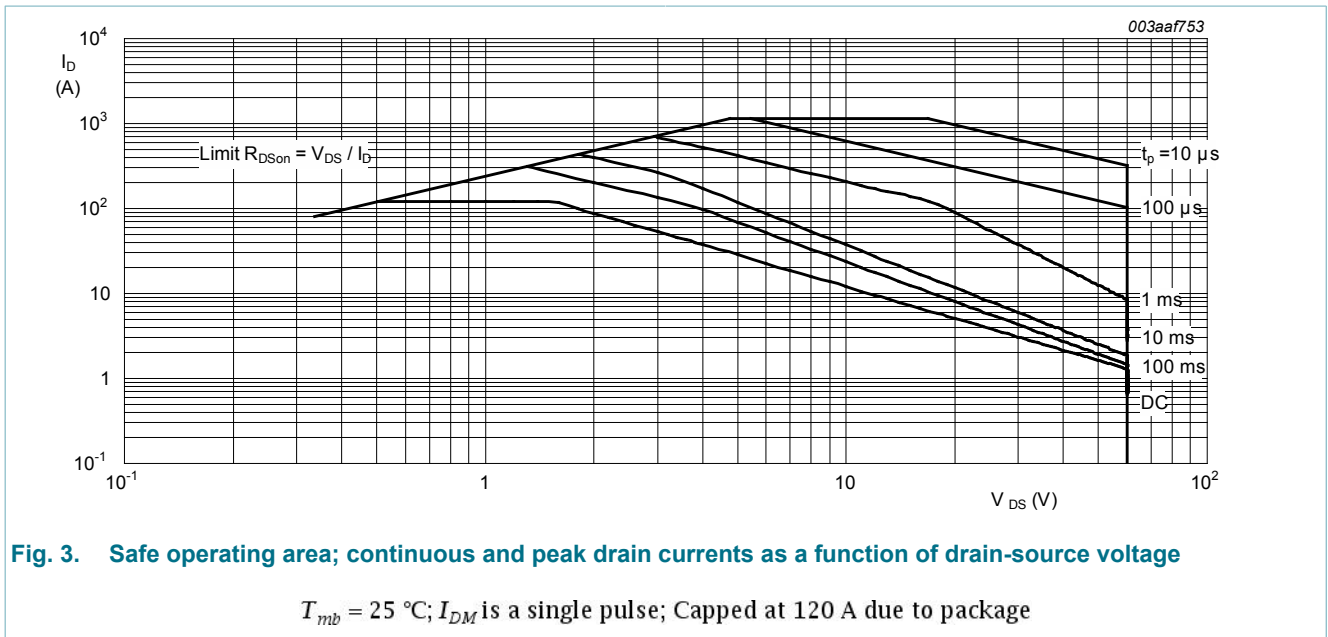
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	60	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	60	V

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Symbol	Parameter	Conditions		Min	Max	Unit
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	338	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	[1]	-	120	A
		V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	120	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	1135	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	120	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1135	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 120 A; V _{sup} ≤ 60 V; R _{GS} = 50 Ω; Unclamped		-	913	mJ

[1] Continuous current limited by package

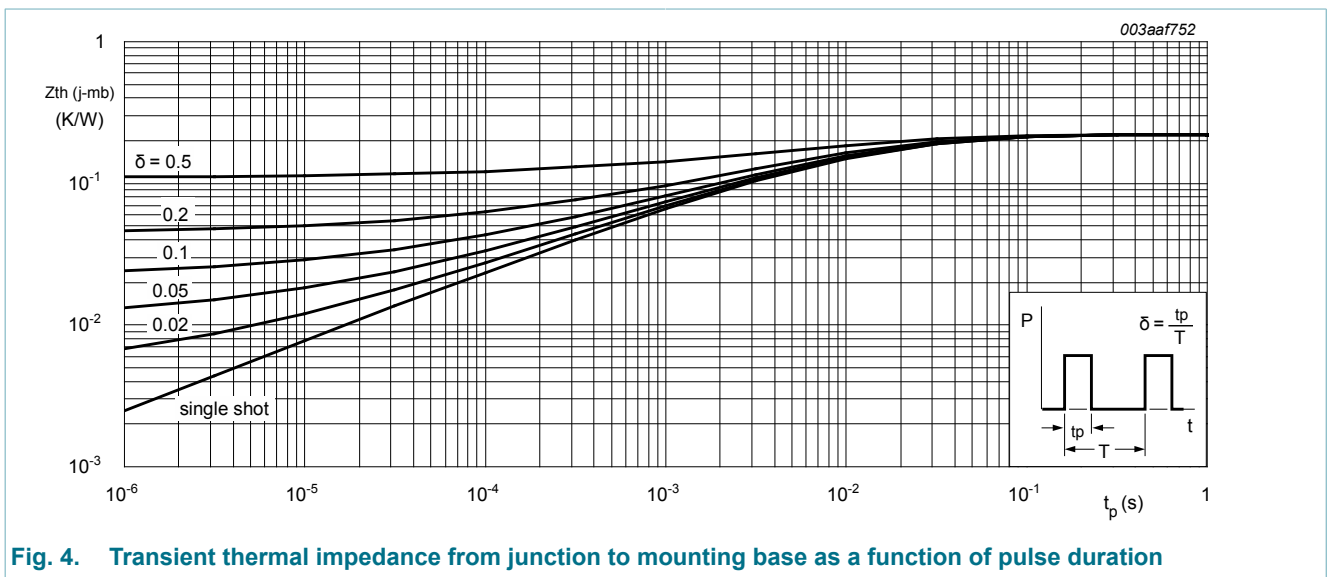




8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.22	0.44	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Vertical in free air	-	60	-	K/W



9. Characteristics

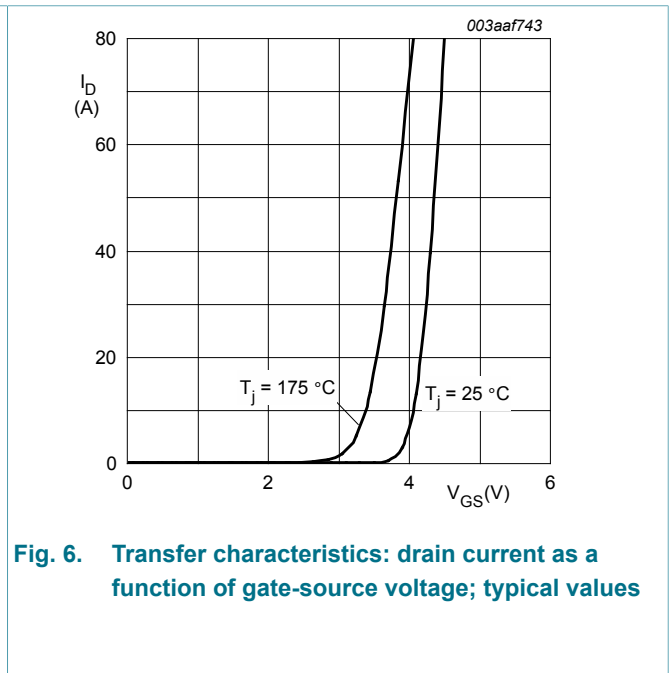
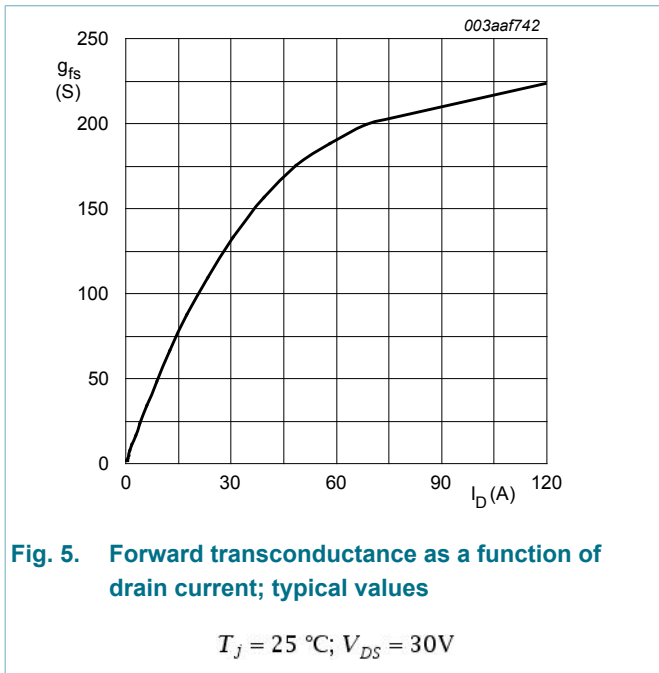
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C	54	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C	60	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 175 °C; Fig. 10	1	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 25 °C; Fig. 11 ; Fig. 10	2	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = -55 °C; Fig. 10	-	-	4.6	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _J = 25 °C	-	0.03	10	μA
		V _{DS} = 60 V; V _{GS} = 0 V; T _J = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C	-	-	100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C	-	-	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 12	[1]	1.8	2.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 12 ; Fig. 13	-	4.3	5.1	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 100 °C; Fig. 12 ; Fig. 13	-	3	3.5	mΩ
R _G	gate resistance	f = 1 MHz	0.45	0.9	1.8	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 75 A; V _{DS} = 30 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15	-	137	192	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15	-	129	181	nC
Q _{GS}	gate-source charge	I _D = 75 A; V _{DS} = 30 V; V _{GS} = 10 V	-	48	68	nC
Q _{GS(th)}	pre-threshold gate-source charge	I _D = 75 A; V _{DS} = 30 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15	-	29	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	19	-	nC
Q _{GD}	gate-drain charge		-	32	45	nC
V _{GS(pl)}	gate-source plateau voltage	V _{DS} = 30 V; Fig. 14 ; Fig. 15	-	5.7	-	V
C _{iss}	input capacitance	V _{DS} = 30 V; V _{GS} = 0 V; f = 1 MHz;	-	9997	13500	pF
C _{oss}	output capacitance	T _J = 25 °C; Fig. 16	-	1210	1640	pF

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rSS}	reverse transfer capacitance		-	594	835	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 0.4\ \Omega; V_{GS} = 10\text{ V}; R_{G(ext)} = 4.7\ \Omega; I_D = 75\text{ A}$	-	42	63	ns
t_r	rise time		-	56	84	ns
$t_{d(off)}$	turn-off delay time		-	115	173	ns
t_f	fall time		-	49	74	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 17}$	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 30\text{ V}$	-	57	75	ns
Q_r	recovered charge	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 30\text{ V}$	-	80	104	nC

[1] Measured 3 mm from package.



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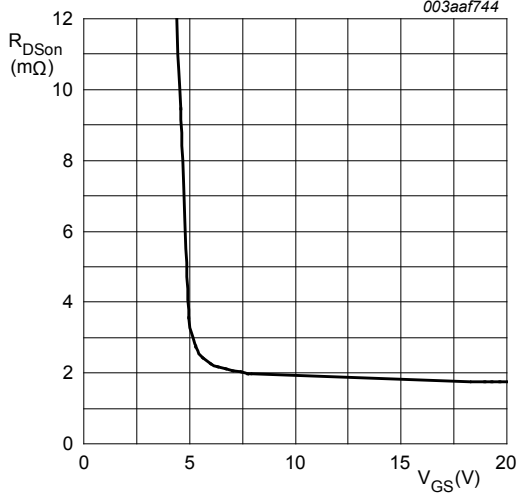


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

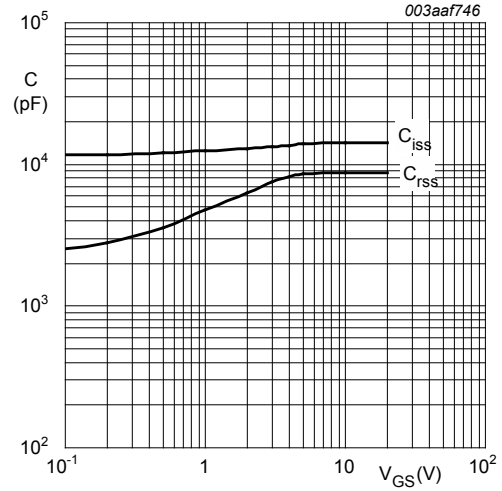


Fig. 8. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

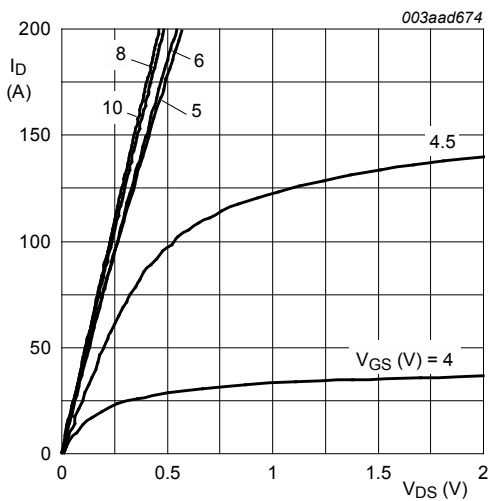


Fig. 9. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}$

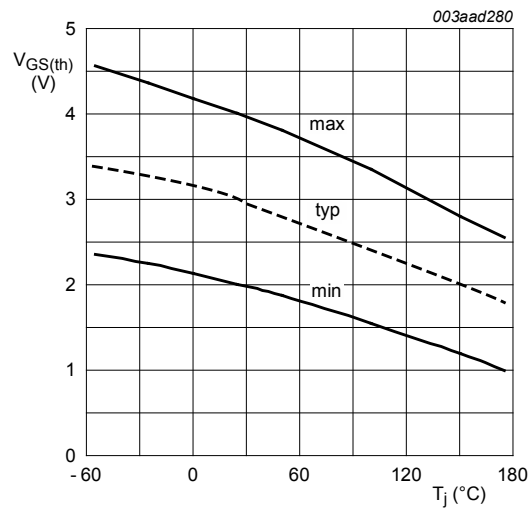


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

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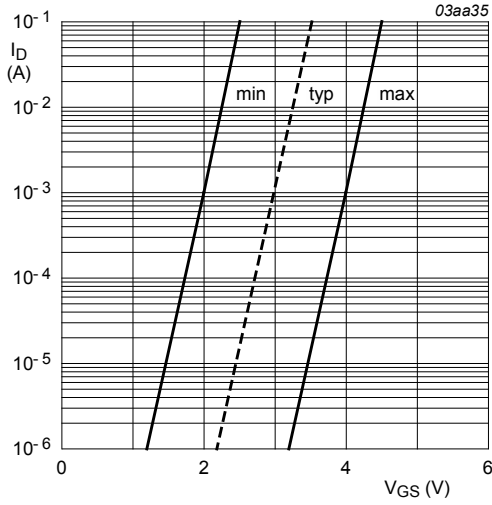


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$

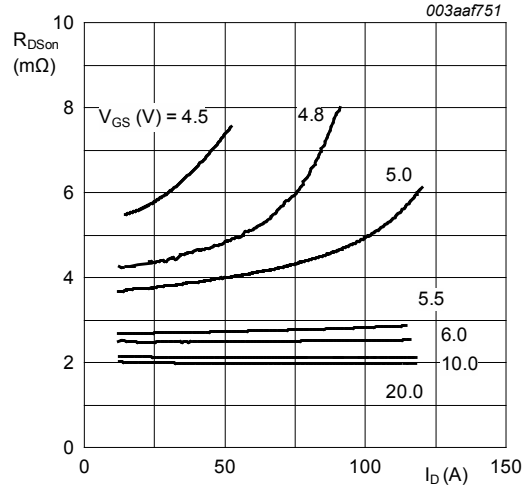


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25\text{ }^\circ\text{C}$

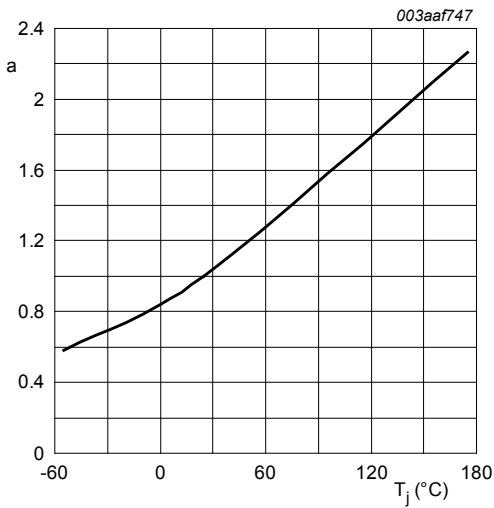


Fig. 13. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

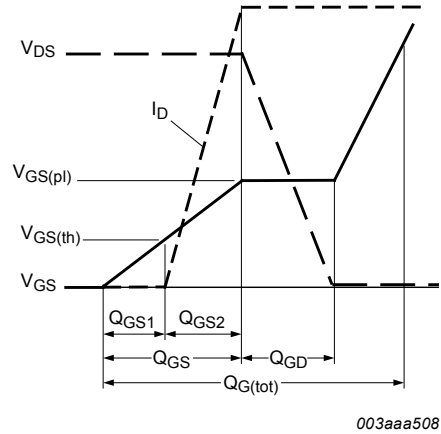


Fig. 14. Gate charge waveform definitions

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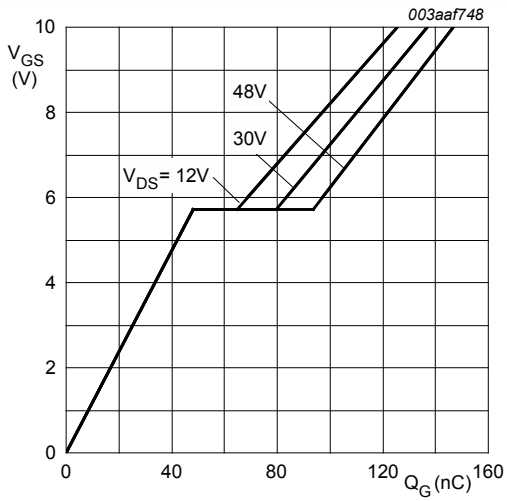


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 75\text{ A}$

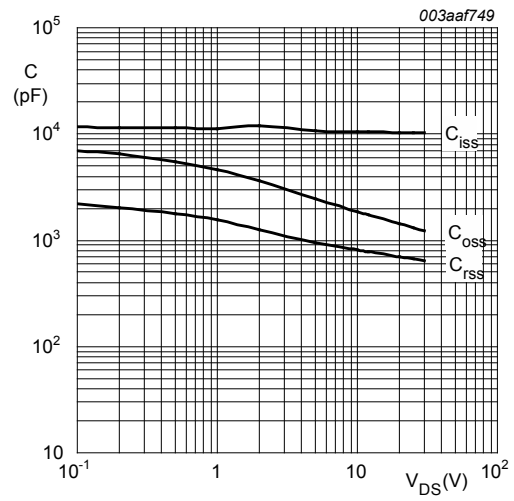


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

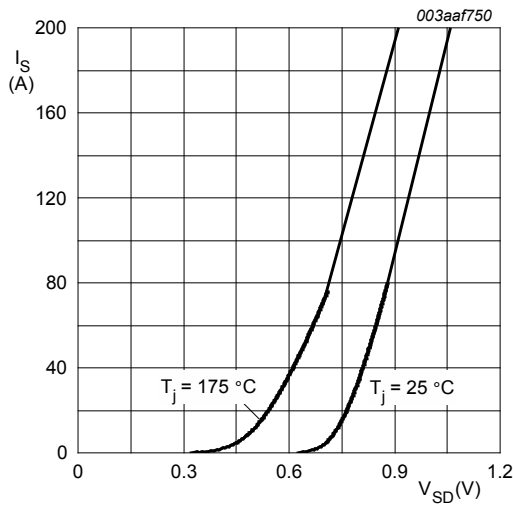


Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0\text{ V}$

10. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁ (2)	b ₂ (2)	c	D	D ₁	E	e	L	L ₁ (1)	L ₂ (1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes

- Lead shoulder designs may vary.
- Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT78		3-lead TO-220AB	SC-46		08-04-23 08-06-13

Fig. 18. Package outline TO-220AB (SOT78)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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