**Product data sheet** 

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a 6 bumps Wafer Level Chip-Size Package (WLCSP) using Trench MOSFET technology.

### 2. Features and benefits

- Low threshold voltage
- Ultra small package: 0.98 × 1.48 × 0.35 mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

# 3. Applications

- · Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

#### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
$V_{DS}$	drain-source voltage	T <sub>j</sub> = 25 °C		-	-	12	V	
V <sub>GS</sub>	gate-source voltage			-8	-	8	V	
I <sub>D</sub>	drain current	V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	-	9.6	Α	
Static characte	Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 3 \text{ A}; T_j = 25 ^{\circ}\text{C}$		-	15	18	mΩ	

<sup>[1]</sup> Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.



# 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol	
A1	G	gate	1 2	D I	
A2	S	source	A O O		
B1	S	source	В	$G \left( \begin{array}{c} \downarrow \\ \downarrow \\ \downarrow \end{array} \right)$	
B2	S	source			
C1	D	drain			
C2	D	drain	Transparent top view WLCSP6 (OL- PMCM6501VNE)	S 017aaa255	

# 6. Ordering information

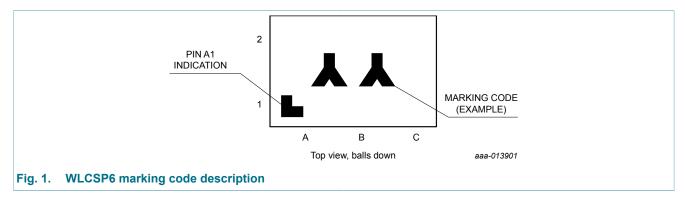
Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PMCM6501VNE	WLCSP6	WLCSP6: wafer level chip-size package; 6 bumps (3 x 2)	OL-PMCM6501VNE			

# 7. Marking

Table 4. Marking codes

Type number	Marking code
PMCM6501VNE	AC



# **Limiting values**

Table 5. **Limiting values** 

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> = 25 °C		-	12	V
$V_{GS}$	gate-source voltage			-8	8	V
I <sub>D</sub>	drain current	$V_{GS} = 4.5 \text{ V}; T_{amb} = 25 \text{ °C}; t \le 5 \text{ s}$	[1]	-	9.6	Α
		V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	7.3	Α
		V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	4.6	Α
I <sub>DM</sub>	peak drain current	$T_{amb}$ = 25 °C; single pulse; $t_p \le 10 \mu s$		-	29	Α
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	556	mW
			[1]	-	1300	mW
		T <sub>sp</sub> = 25 °C		-	12500	mW
Tj	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
Source-drai	n diode	,				J
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	1.2	Α

<sup>[1]</sup> Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

Device mounted on an FR4 Printed Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

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12 V, N-channel Trench MOSFET

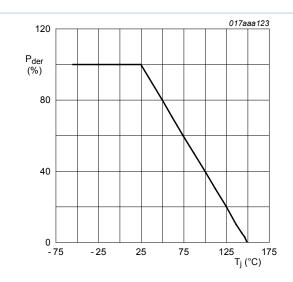


Fig. 2. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

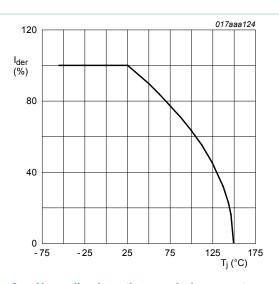


Fig. 3. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

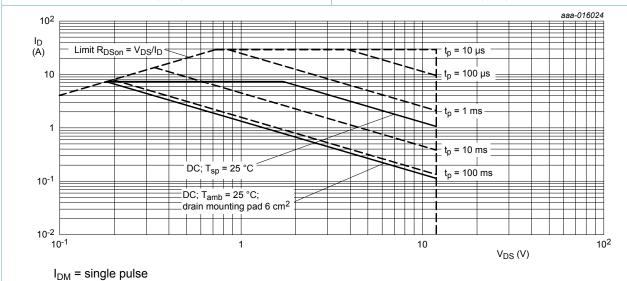


Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R <sub>th(j-a)</sub> thermal resista from junction to ambient	thermal resistance		[1]	-	180	225	K/W
	1		[2]	-	65	85	K/W
	ambient		[3]	-	75	95	K/W
		in free air; t ≤ 5 s	[3]	-	45	55	K/W
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Product data sheet 26 August 2015 4 / 15

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point		-	5	10	K/W

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain, 4-layer, 1 cm<sup>2</sup>.
- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

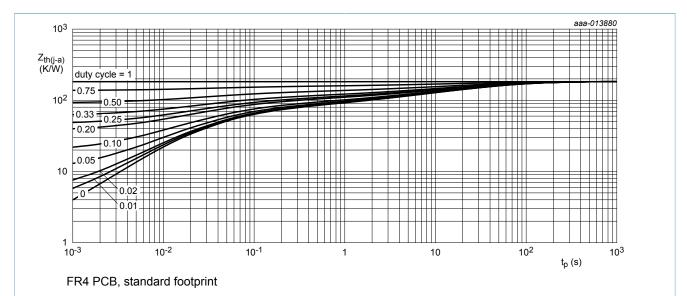


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

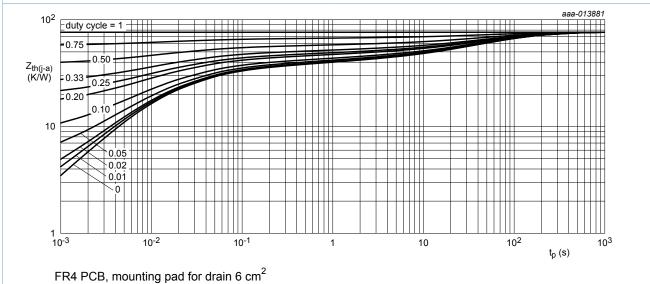


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

# 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics			'		_
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	12	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	0.4	0.6	0.9	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 12 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	10	μA
		V <sub>GS</sub> = -8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	-10	μA
		V <sub>GS</sub> = 4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	1	μA
		V <sub>GS</sub> = -4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	-1	μA
		V <sub>GS</sub> = 2.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	200	nA
		V <sub>GS</sub> = -2.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	-200	nA
R <sub>DSon</sub>	drain-source on-state	$V_{GS}$ = 4.5 V; $I_D$ = 3 A; $T_j$ = 25 °C	-	15	18	mΩ
	resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 3 A; T <sub>j</sub> = 150 °C	-	20	25	mΩ
		$V_{GS}$ = 2.5 V; $I_D$ = 3 A; $T_j$ = 25 °C	-	18	22	mΩ
		V <sub>GS</sub> = 1.8 V; I <sub>D</sub> = 2 A; T <sub>j</sub> = 25 °C	-	22	30	mΩ
		V <sub>GS</sub> = 1.5 V; I <sub>D</sub> = 1 A; T <sub>j</sub> = 25 °C	-	30	45	mΩ
9 <sub>fs</sub>	forward transconductance	$V_{DS} = 6 \text{ V}; I_D = 3 \text{ A}; T_j = 25 \text{ °C}$	-	30	-	S
$R_G$	gate resistance	f = 1 MHz; T <sub>j</sub> = 25 °C	-	12.7	-	Ω
Dynamic o	characteristics				'	
Q <sub>G(tot)</sub>	total gate charge	$V_{DS} = 6 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 4.5 \text{ V};$	-	16.1	24	nC
$Q_{GS}$	gate-source charge	T <sub>j</sub> = 25 °C	-	1.1	-	nC
$Q_{GD}$	gate-drain charge		-	4.7	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 6 V; f = 1 MHz; V <sub>GS</sub> = 0 V;	-	920	-	pF
C <sub>oss</sub>	output capacitance	$T_j = 25 ^{\circ}\text{C}$	-	350	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	330	-	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 6 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 4.5 \text{ V};$	-	10.8	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	33.5	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	97.5	-	ns
t <sub>f</sub>	fall time		-	73.2	-	ns

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Source-drain o	Source-drain diode						
V <sub>SD</sub>	source-drain voltage	$I_S = 1.2 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$		-	0.6	1.2	V

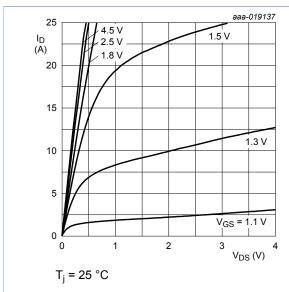
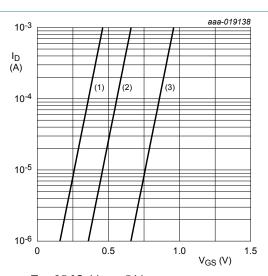


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values



$$T_j$$
 = 25 °C;  $V_{DS}$  = 5  $V$ 

- (1) minimum values
- (2) typical values
- (3) maximum values

Fig. 8. Sub-threshold drain current as a function of gate-source voltage

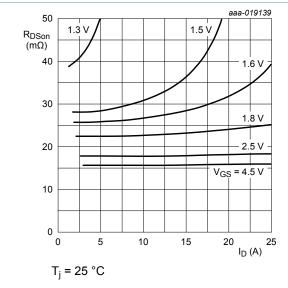


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

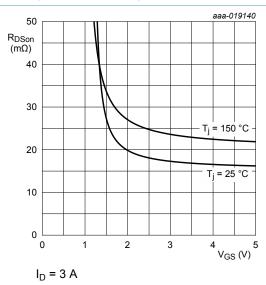


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

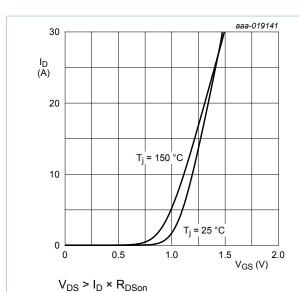


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

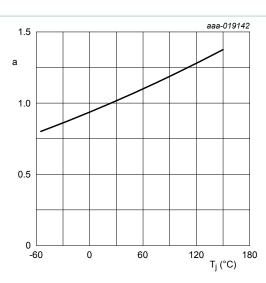
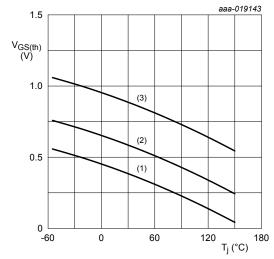


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

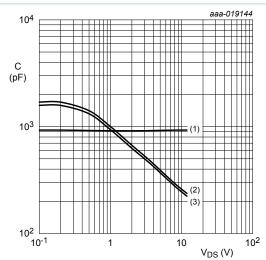
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$



 $I_D$  = 0.25 mA;  $V_{DS}$  =  $V_{GS}$ 

- (1) minimum values
- (2) typical values
- (3) maximum values

Fig. 13. Gate-source threshold voltage as a function of junction temperature



 $f = 1 MHz; V_{GS} = 0 V$ 

- (1) C<sub>iss</sub>
- (2) C<sub>oss</sub>
- (3) C<sub>rss</sub>

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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12 V, N-channel Trench MOSFET

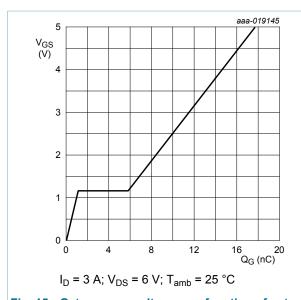


Fig. 15. Gate-source voltage as a function of gate charge; typical values

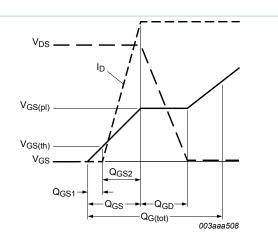


Fig. 16. MOSFET transistor: Gate charge waveform definitions

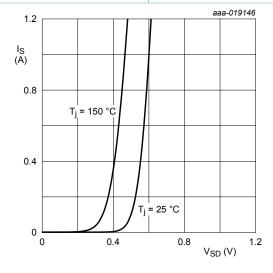
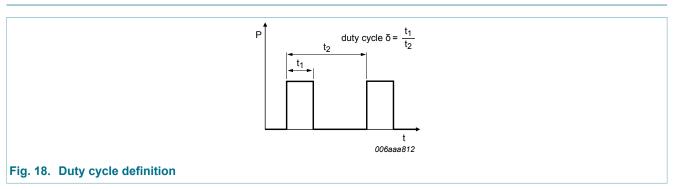


Fig. 17. Source current as a function of source-drain voltage; typical values

### 11. Test information

 $V_{GS} = 0 V$ 

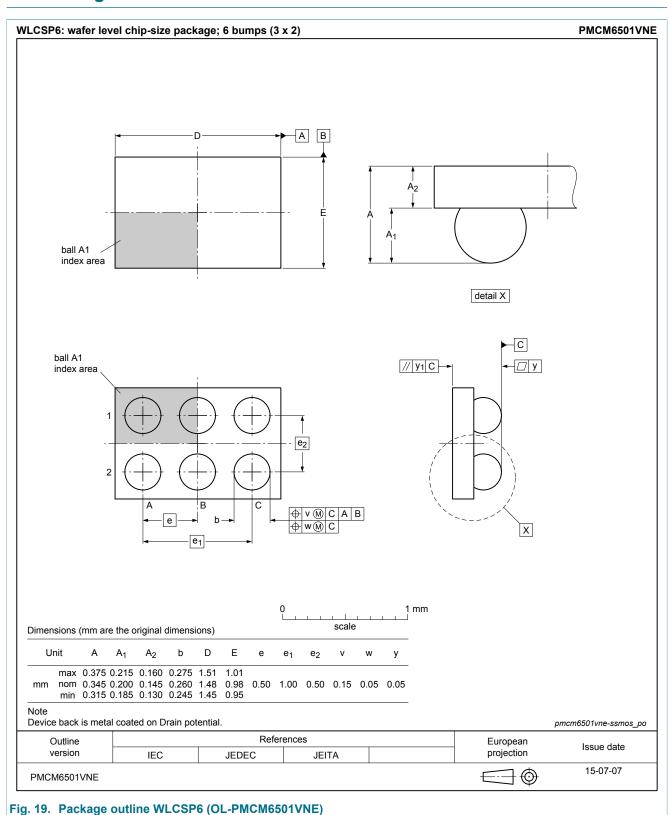


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# 12. Package outline

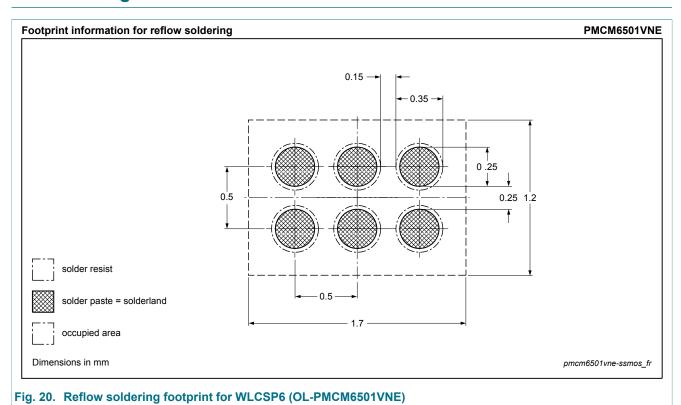


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# 13. Soldering



# 14. Revision history

#### Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMCM6501VNE v.1	20150825	Product data sheet	-	-

### 15. Legal information

#### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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### 16. Contents

2 Features and benefits 3 Applications 4 Quick reference data 5 Pinning information 6 Ordering information 7 Marking 8 Limiting values 9 Thermal characteristics 10 Characteristics 11 Test information 12 Package outline 13 Soldering 14 Revision history 15 Legal information 15.1 Data sheet status 15.2 Definitions 15.3 Disclaimers 15.4 Trademarks	1	General description	1
4 Quick reference data	2	Features and benefits	1
5 Pinning information	3	Applications	1
6 Ordering information	4	Quick reference data	1
7 Marking	5	Pinning information	2
8 Limiting values	6	Ordering information	2
9 Thermal characteristics	7	Marking	2
10 Characteristics	8	Limiting values	3
11 Test information	9	Thermal characteristics	4
12 Package outline	10	Characteristics	6
13 Soldering	11	Test information	9
14 Revision history	12	Package outline	10
15 Legal information	13	Soldering	11
15.1 Data sheet status	14	Revision history	12
<ul><li>15.2 Definitions</li><li>15.3 Disclaimers</li></ul>	15	Legal information	13
15.3 Disclaimers	15.1	Data sheet status	13
	15.2	Definitions	13
15.4 Trademarks	15.3	Disclaimers	13
	15.4	Trademarks	14

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