



BUK768R1-40E

N-channel TrenchMOS standard level FET

Rev. 1.1 — 10 July 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with VGS(th) rating of greater than 1V at 175 °C

1.3 Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

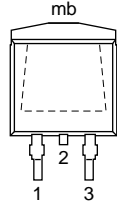
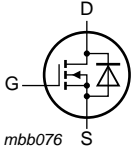
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	40	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1	[1]	-	75	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	96	W
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 20 A; T _j = 25 °C; see Figure 11	-	5.6	7.2	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 20 A; V _{DS} = 32 V; see Figure 13 ; see Figure 14	-	7.4	-	nC

[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p style="text-align: center;">D2PAK (SOT404)</p>	 <p style="text-align: center;"><i>mbb076</i></p>
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK768R1-40E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
BUK768R1-40E	BUK768R1-40E

5. Limiting values

Table 5. Limiting values

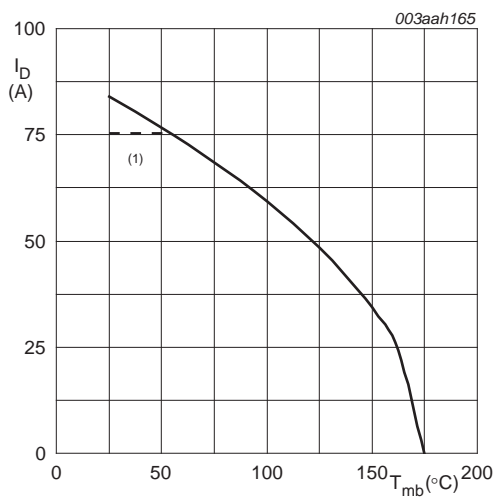
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	40	V	
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V	
V_{GS}	gate-source voltage	$T_j = 25\text{ °C}$	-20	20	V	
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1	[1]	-	75	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1	[1]	-	59	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ see Figure 4	-	335	A	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	96	W	
T_{stg}	storage temperature		-55	175	°C	
T_j	junction temperature		-55	175	°C	
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	75	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$	-	335	A	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}; V_{sup} \leq 40\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped; see Figure 3	[2][3]	-	43.8	mJ

[1] Continuous current is limited by package.

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

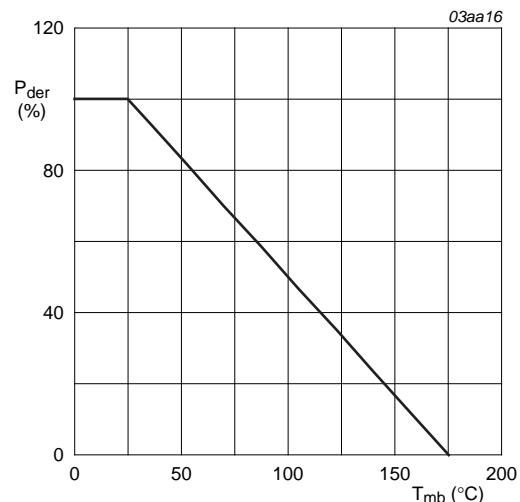
[3] Refer to application note AN10273 for further information.



$$V_{GS} \geq 10V$$

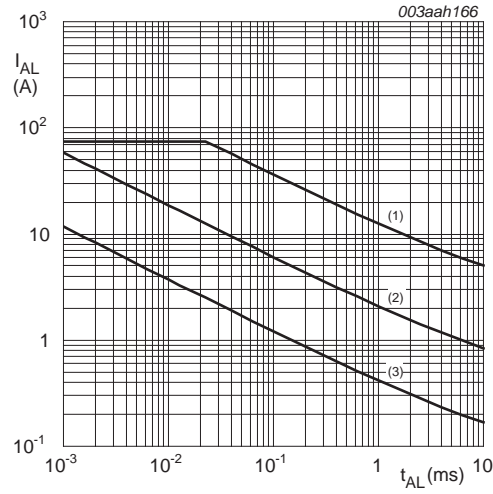
(1) Capped at 75A due to package

Fig 1. Continuous drain current as a function of mounting base temperature



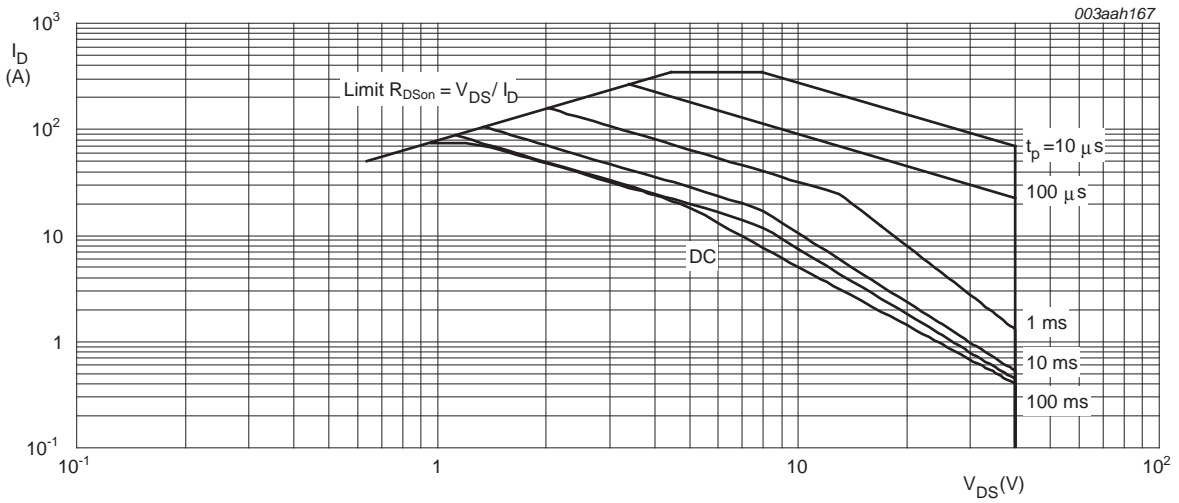
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



(1) $T_{j (init)} = 25^{\circ}C$; (2) $T_{j (init)} = 150^{\circ}C$; (3) Repetitive Avalanche

Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



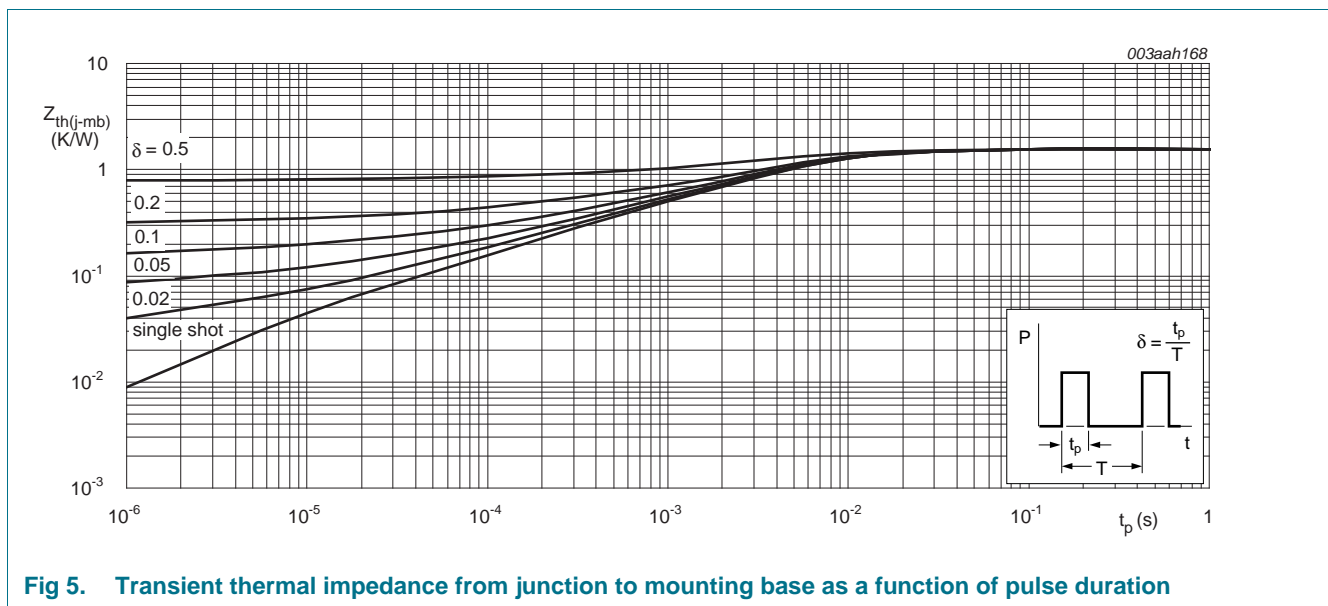
$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

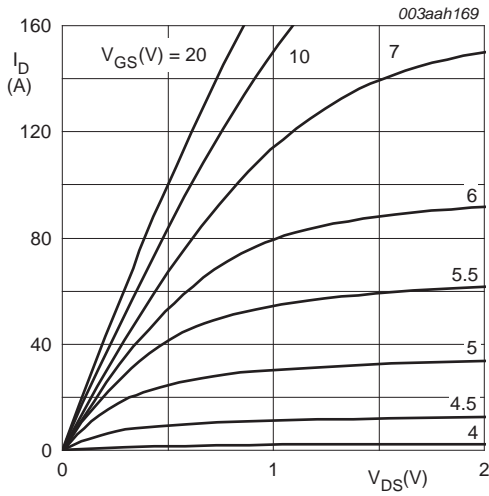
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W



7. Characteristics

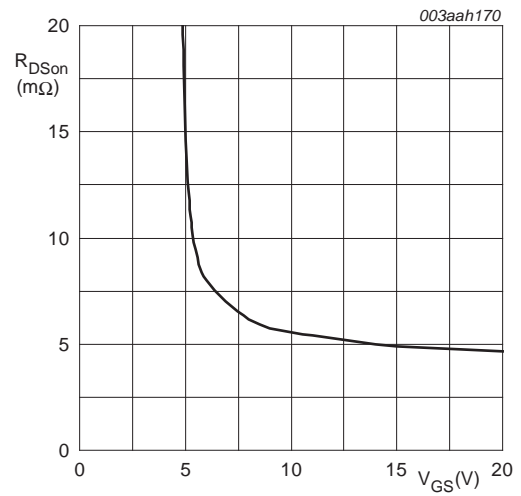
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 9 ; see Figure 10	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 10	-	-	4.5	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$; see Figure 10	1	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.05	1	μA
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 20 A; T_j = 25 \text{ }^\circ C$; see Figure 11	-	5.6	7.2	m Ω
		$V_{GS} = 10 V; I_D = 20 A; T_j = 175 \text{ }^\circ C$; see Figure 12 ; see Figure 11	-	-	13.7	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 20 A; V_{DS} = 32 V; V_{GS} = 10 V$; see Figure 13 ; see Figure 14	-	24	-	nC
Q_{GS}	gate-source charge		-	5.6	-	nC
Q_{GD}	gate-drain charge		-	7.4	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 V; V_{DS} = 25 V; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; see Figure 15	-	1300	1730	pF
C_{oss}	output capacitance		-	260	312	pF
C_{riss}	reverse transfer capacitance		-	144	197	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 V; R_L = 1.5 \text{ } \Omega; V_{GS} = 10 V; R_{G(ext)} = 5 \text{ } \Omega$	-	11	-	ns
t_r	rise time		-	9	-	ns
$t_{d(off)}$	turn-off delay time		-	21	-	ns
t_f	fall time		-	9	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 20 A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$; see Figure 16	-	0.86	1.2	V
t_{rr}	reverse recovery time	$I_S = 20 A; di_S/dt = -100 A/\mu s; V_{GS} = 0 V; V_{DS} = 25 V$	-	18.6	-	ns
Q_r	recovered charge		-	10.7	-	nC



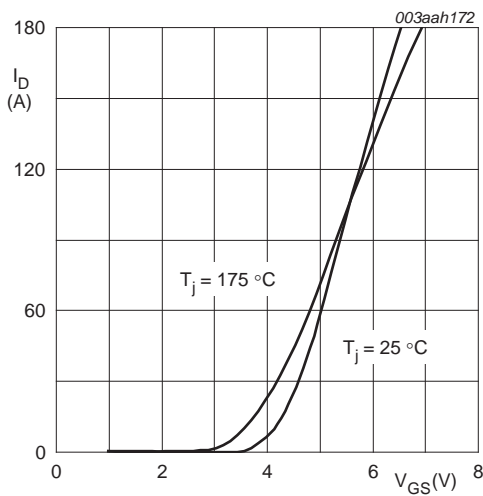
$T_j = 25^\circ\text{C}$; $t_p = 300 \mu\text{s}$

Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values



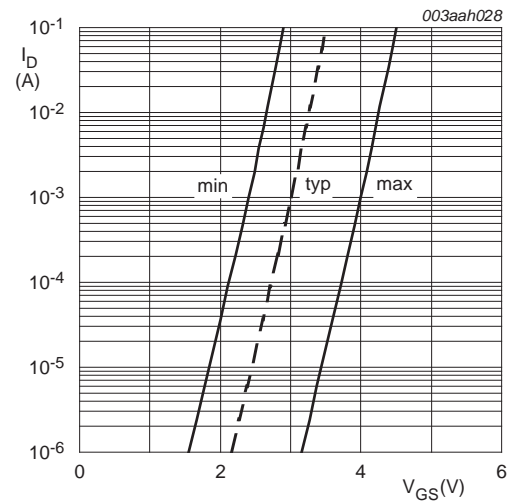
$T_j = 25^\circ\text{C}$; $I_D = 20\text{A}$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



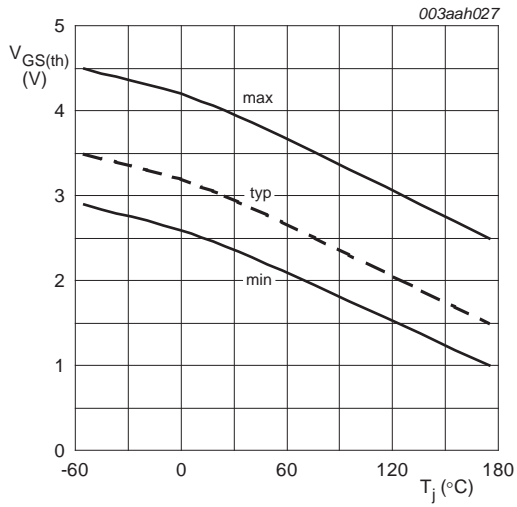
$V_{DS} = 10\text{V}$

Fig 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



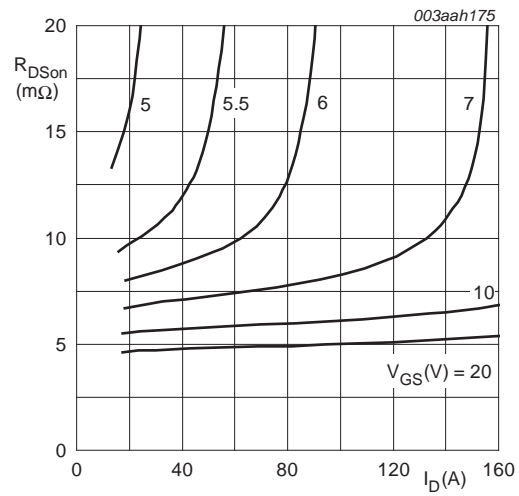
$T_j = 25^\circ\text{C}$; $V_{DS} = 5\text{V}$

Fig 9. Sub-threshold drain current as a function of gate-source voltage



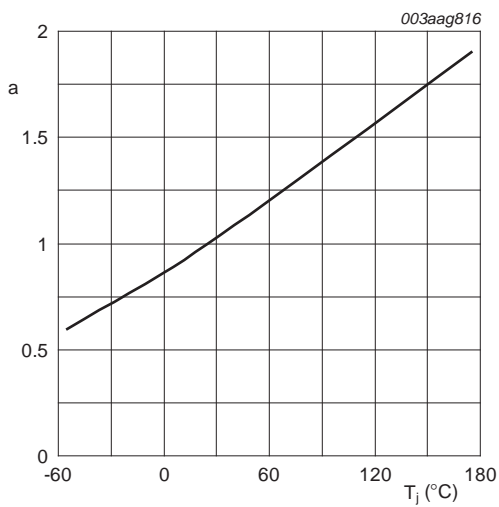
$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

Fig 10. Gate-source threshold voltage as a function of junction temperature



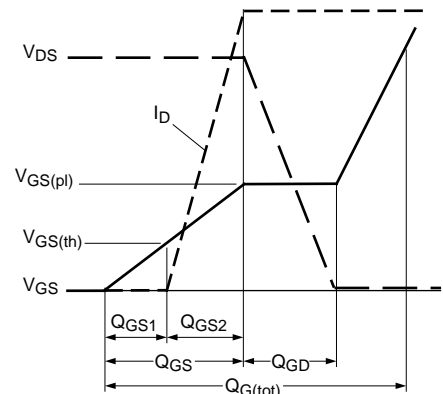
$$T_j = 25 \text{ °C}; t_p = 300 \text{ }\mu\text{s}$$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values



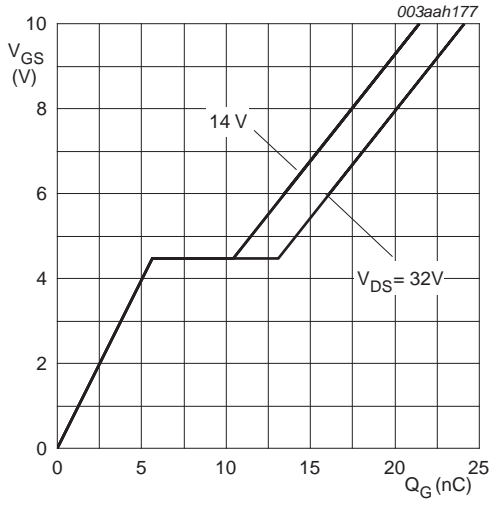
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25 \text{ °C})}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



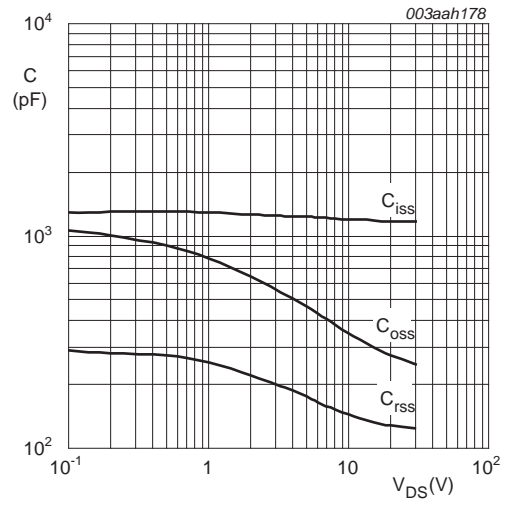
003aaa508

Fig 13. Gate charge waveform definitions



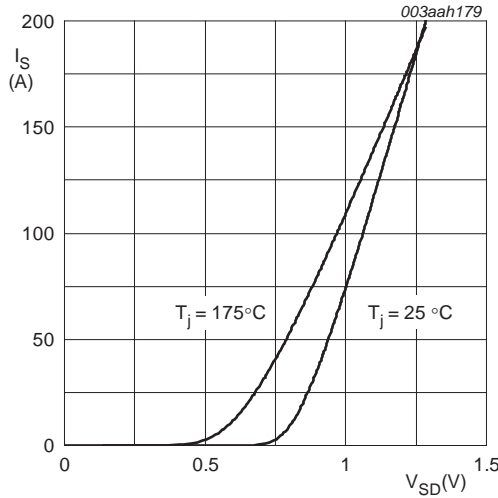
$T_j = 25^\circ\text{C}; I_D = 15\text{A}$

Fig 14. Transient thermal impedance from junction to mounting base as a function of pulse duration



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{V}$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

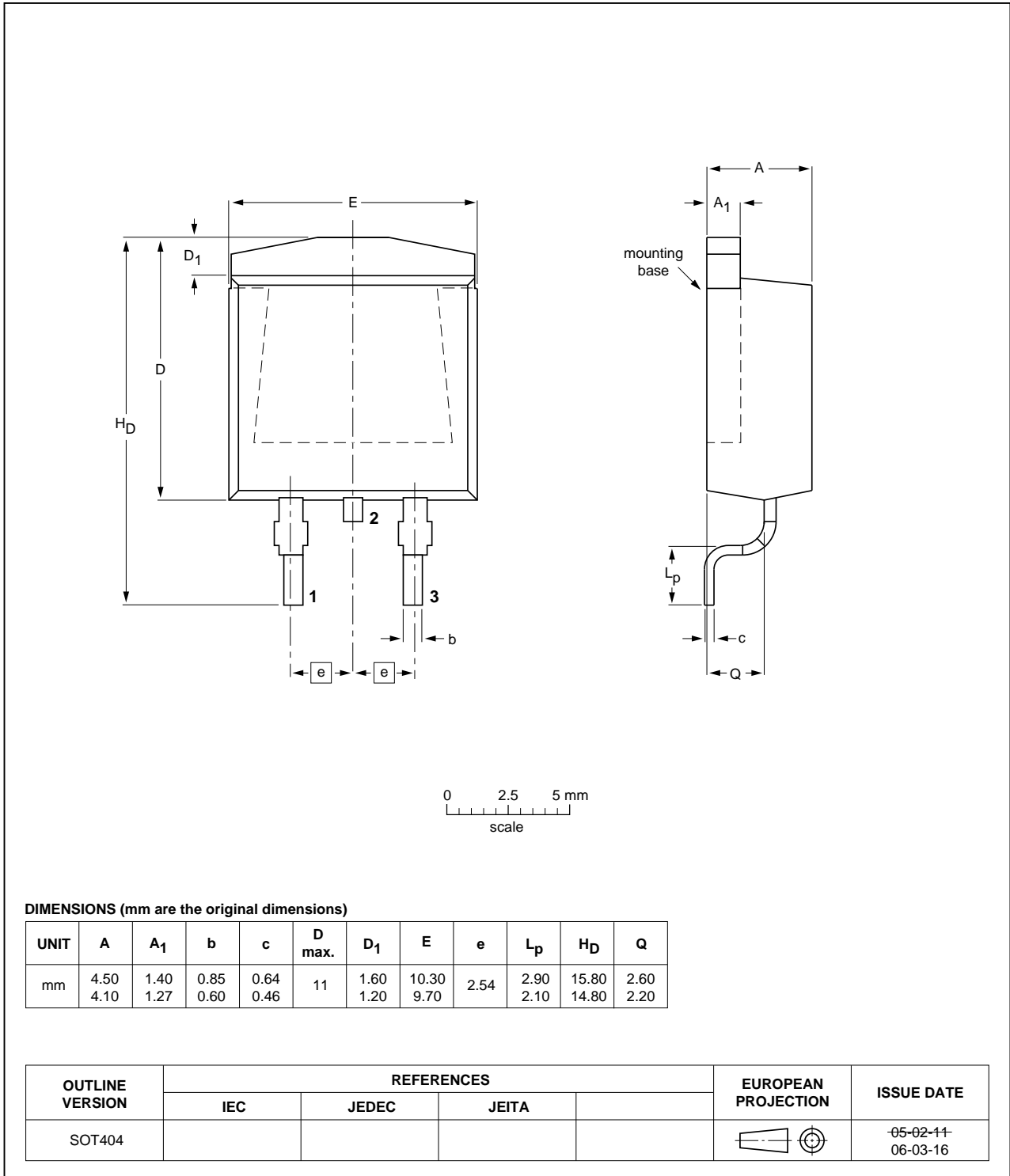


Fig 17. D2PAK (SOT404)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK768R1-40E v.1.1	20120710	Product data sheet	-	BUK768R1-40E v.1
BUK768R1-40E v.1	20120706	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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For sales office addresses, please send an email to: salesaddresses@nxp.com

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