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Kind regards,

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74LV244-Q100

Octal buffer/line driver (3-state)

Rev. 1 — 19 May 2014

Product data sheet

1. General description

The 74LV244-Q100 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC244-Q100 and 74HCT244-Q100.

The 74LV244-Q100 is an octal non-inverting buffer/line driver with 3-state outputs. The output enable inputs $1\overline{OE}$ and $2\overline{OE}$ control the 3-state outputs. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7\text{ V}$ and $V_{CC} = 3.6\text{ V}$
- Typical V_{OLP} (output ground bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$
- Typical V_{OHV} (output V_{OH} undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV244D-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LV244PW-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1



4. Block diagram

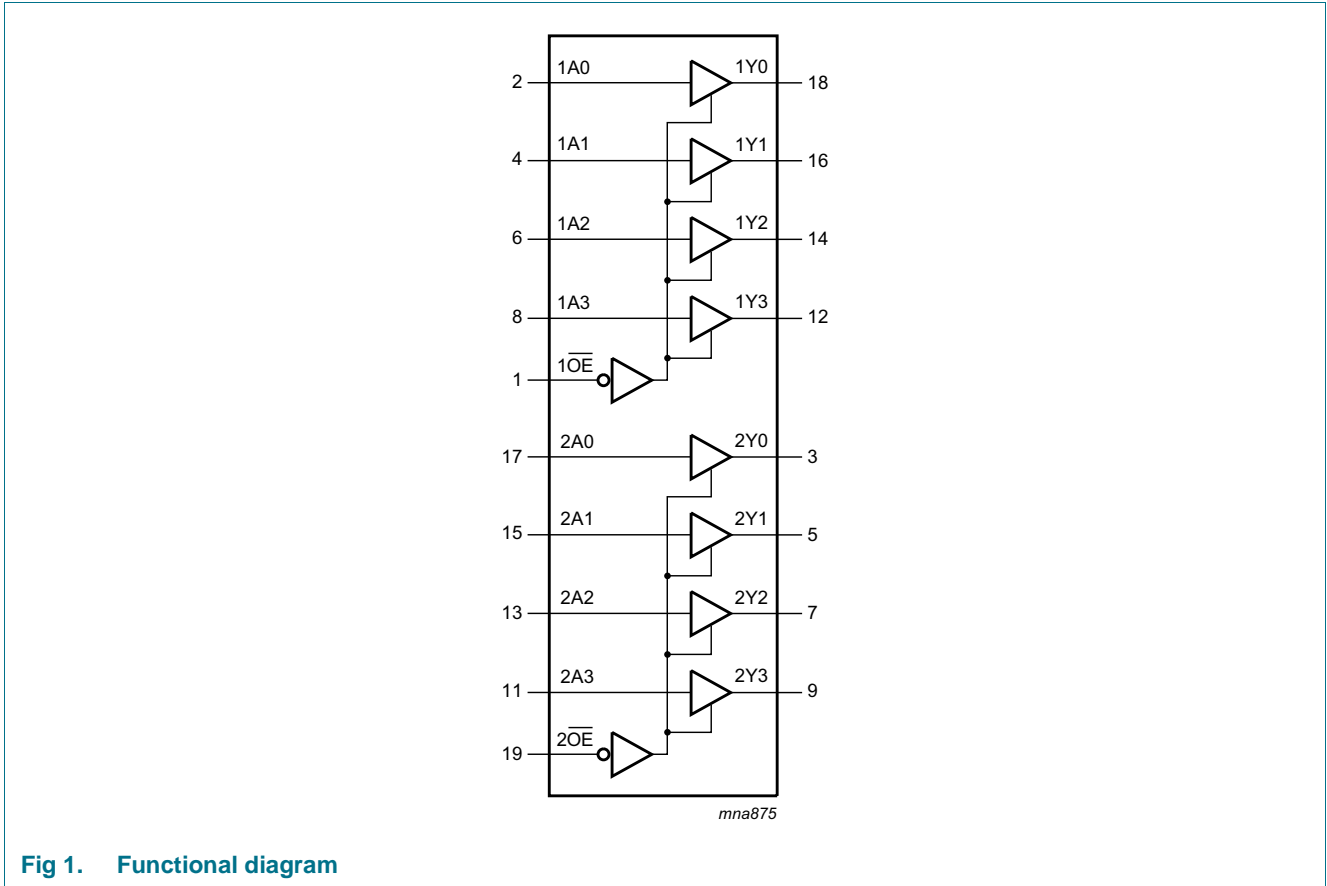


Fig 1. Functional diagram

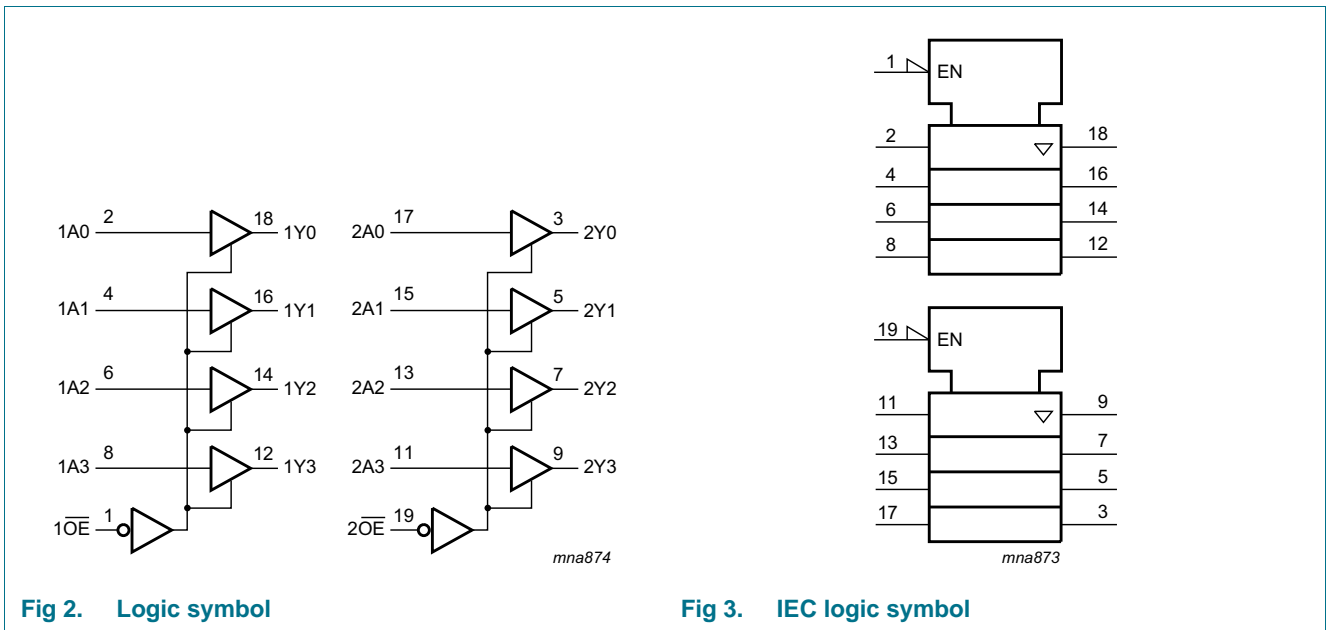


Fig 2. Logic symbol

Fig 3. IEC logic symbol

5. Pinning information

5.1 Pinning

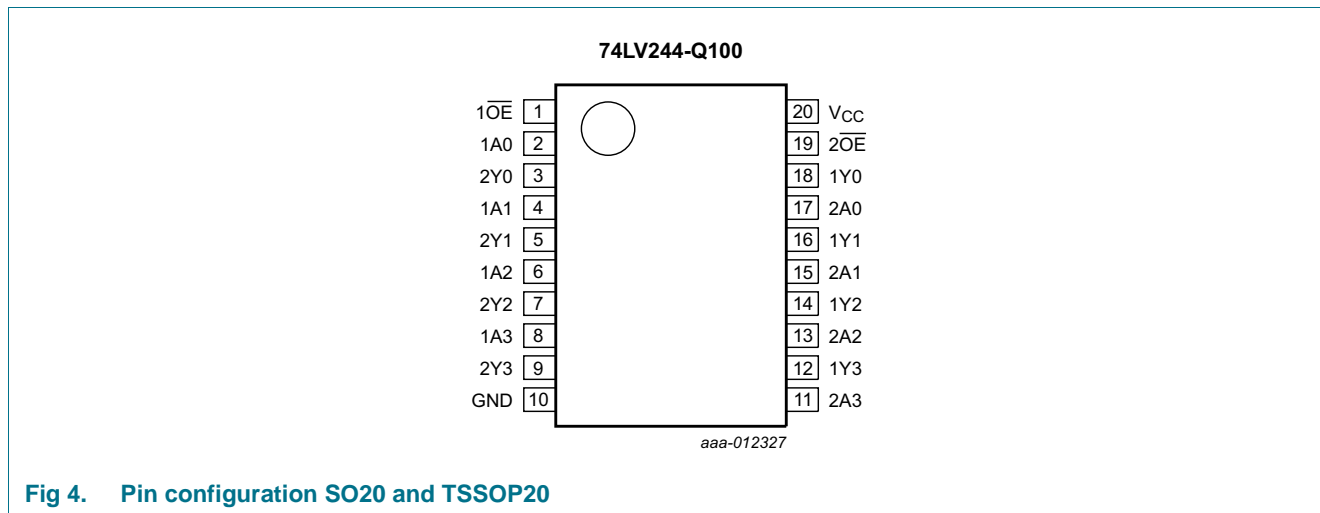


Fig 4. Pin configuration SO20 and TSSOP20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}, 2\overline{OE}$	1, 19	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	bus output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	bus output
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table^[1]

Input		Output
$n\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{CC}	supply voltage		-0.5	+7.0	V	
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA	
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 50	mA	
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	± 35	mA	
I_{CC}	supply current		-	70	mA	
I_{GND}	ground current		-70	-	mA	
T_{stg}	storage temperature		-65	+150	°C	
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$				
		SO20	[1]	-	500	mW
		TSSOP20	[2]	-	400	mW

[1] For SO20 packages: P_{tot} derates linearly with 8 mW/K above 70 °C.

[2] For TSSOP20 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+85	°C
			-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V}$ to 2.0 V	0	-	500	ns/V
		$V_{CC} = 2.0\text{ V}$ to 2.7 V	0	-	200	ns/V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	0	-	100	ns/V
		$V_{CC} = 3.6\text{ V}$ to 5.5 V	0	-	50	ns/V

[1] The LV is guaranteed to function down to $V_{CC} = 1.0\text{ V}$ (input levels GND or V_{CC}). DC characteristics are guaranteed from $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 5.5\text{ V}$.

9. Static characteristics

Table 6. Static characteristics

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	0.9	-	-	0.9		V
		V _{CC} = 2.0 V	1.4	-	-	1.4		V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0		V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}		V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.3		0.3	V
		V _{CC} = 2.0 V	-	-	0.6		0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8		0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}		0.3V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = -100 μA						
		V _{CC} = 1.2 V	-	1.2	-	-	-	V
		V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		V _{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		V _{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		V _{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		V _I = V _{IH} or V _{IL}						
		V _{CC} = 3.0 V; I _O = -8 mA	2.40	2.82	-	2.20	-	V
V _{CC} = 4.5 V; I _O = -16 mA	3.60	4.20	-	3.50	-	V		
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = 100 μA						
		V _{CC} = 1.2 V	-	0	-	-	-	V
		V _{CC} = 2.0 V	-	0	0.2	-	0.2	V
		V _{CC} = 2.7 V	-	0	0.2	-	0.2	V
		V _{CC} = 3.0 V	-	0	0.2	-	0.2	V
		V _{CC} = 4.5 V	-	0	0.2	-	0.2	V
		V _{CC} = 3.0 V; I _O = 8 mA	-	0.25	0.40	-	0.50	V
		V _{CC} = 4.5 V; I _O = 16 mA	-	0.35	0.55	-	0.65	V
I _I	input leakage current	V _{CC} = 5.5 V; V _I = V _{CC} or GND	-	-	1.0	-	1.0	μA
I _{OZ}	OFF-state output current	V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	-	-	5	-	10	μA
I _{CC}	supply current	V _{CC} = 5.5 V; V _I = V _{CC} or GND; I _O = 0 A	-	-	20	-	160	μA
ΔI _{CC}	additional supply current	per input; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V	-	-	500	-	850	μA
C _I	input capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics
GND (ground = 0 V); for test circuit, see Figure 7

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	1An to 1Yn; 2An to 2Yn; see Figure 5 ^[2]						
		V _{CC} = 1.2 V	-	50		-	-	ns
		V _{CC} = 2.0 V	-	17	24	-	31	ns
		V _{CC} = 2.7 V	-	13	17	-	23	ns
		V _{CC} = 3.0 V to 3.6 V	-	9	14	-	18	ns
		V _{CC} = 3.3 V; C _L = 15 pF	-	8.0	-	-	-	ns
		V _{CC} = 4.5 V to 5.5 V	-	-	12	-	15	ns
t _{en}	enable time	1 $\overline{O}E$ to 1Yn; 2 $\overline{O}E$ to 2Yn; see Figure 6 ^[2]						
		V _{CC} = 1.2 V	-	65	-	-	-	ns
		V _{CC} = 2.0 V	-	22	39	-	49	ns
		V _{CC} = 2.7 V	-	16	29	-	36	ns
		V _{CC} = 3.0 V to 3.6 V	-	12	23	-	29	ns
		V _{CC} = 4.5 V to 5.5 V	-	-	19	-	24	ns
t _{dis}	disable time	1 $\overline{O}E$ to 1Yn; 2 $\overline{O}E$ to 2Yn; see Figure 6 ^[2]						
		V _{CC} = 1.2 V	-	60		-	-	ns
		V _{CC} = 2.0 V	-	22	34	-	43	ns
		V _{CC} = 2.7 V	-	17	24	-	32	ns
		V _{CC} = 3.0 V to 3.6 V	-	13	21	-	26	ns
		V _{CC} = 4.5 V to 5.5 V	-	-	16	-	19	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 3.3 V ^[3]	-	35	-	-	-	ns

[1] Unless otherwise stated, all typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation P_D = C_{PD} × V_{CC}² × f_i + Σ (C_L × V_{CC}² × f_o) (P_D in μW), where:

f_i = input frequency in MHz;

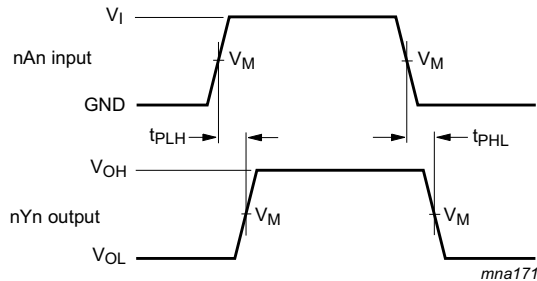
f_o = output frequency in MHz;

Σ (C_L × V_{CC}² × f_o) = sum of outputs;

C_L = output load capacitance in pF;

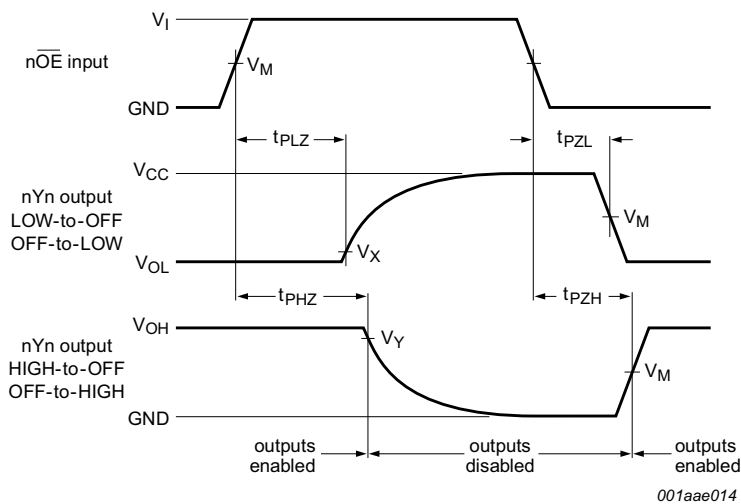
V_{CC} = supply voltage in V.

11. Waveforms



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Input (nAn) to output (nYn) propagation delays

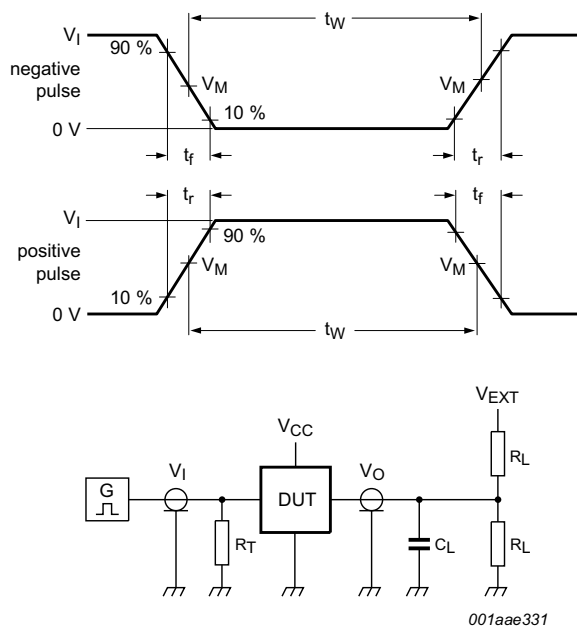


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
$\geq 4.5 V$	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 k Ω	open	GND	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	15 pF, 50 pF	1 k Ω	open	GND	$2V_{CC}$
≥ 4.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 k Ω	open	GND	$2V_{CC}$

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

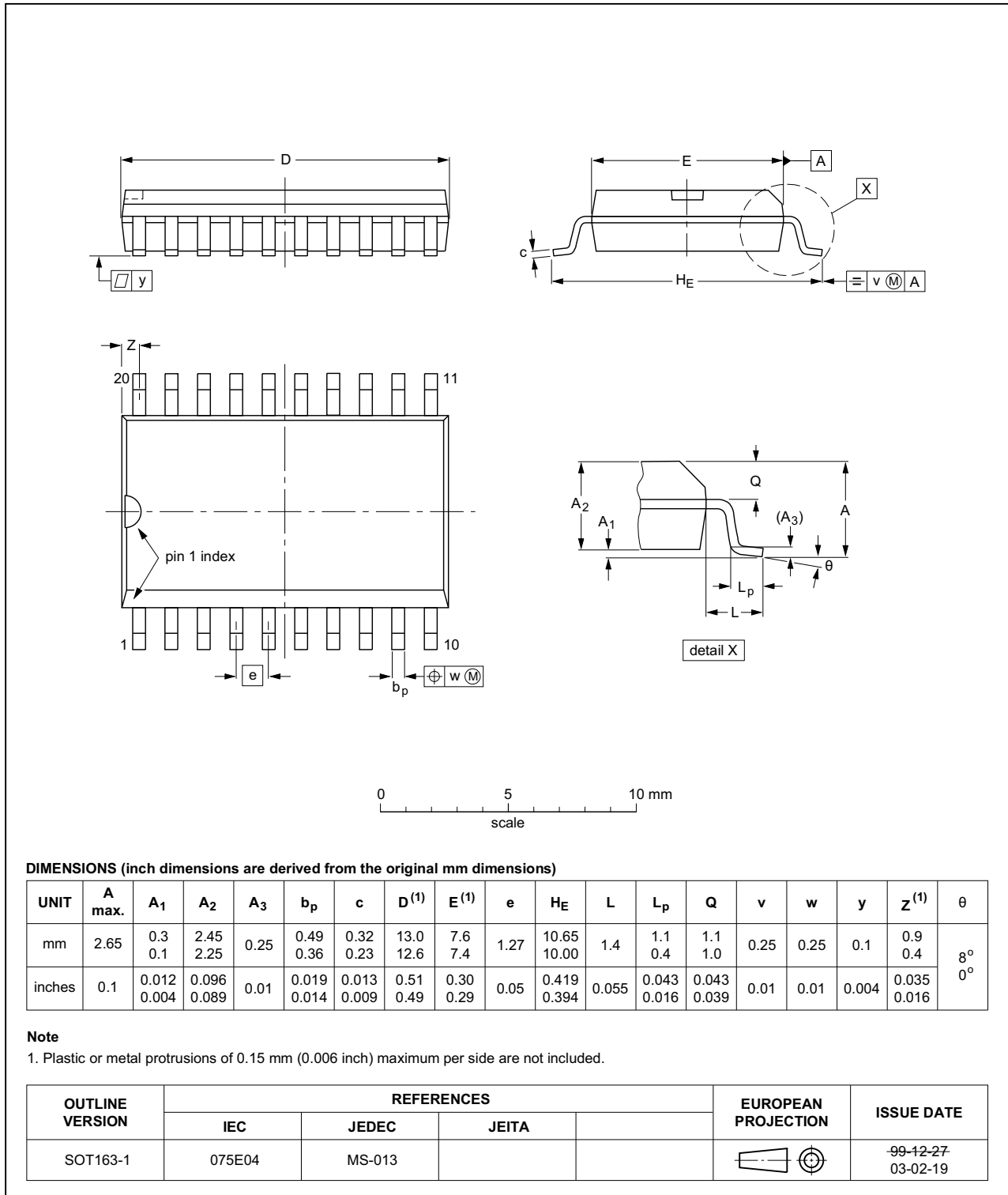


Fig 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

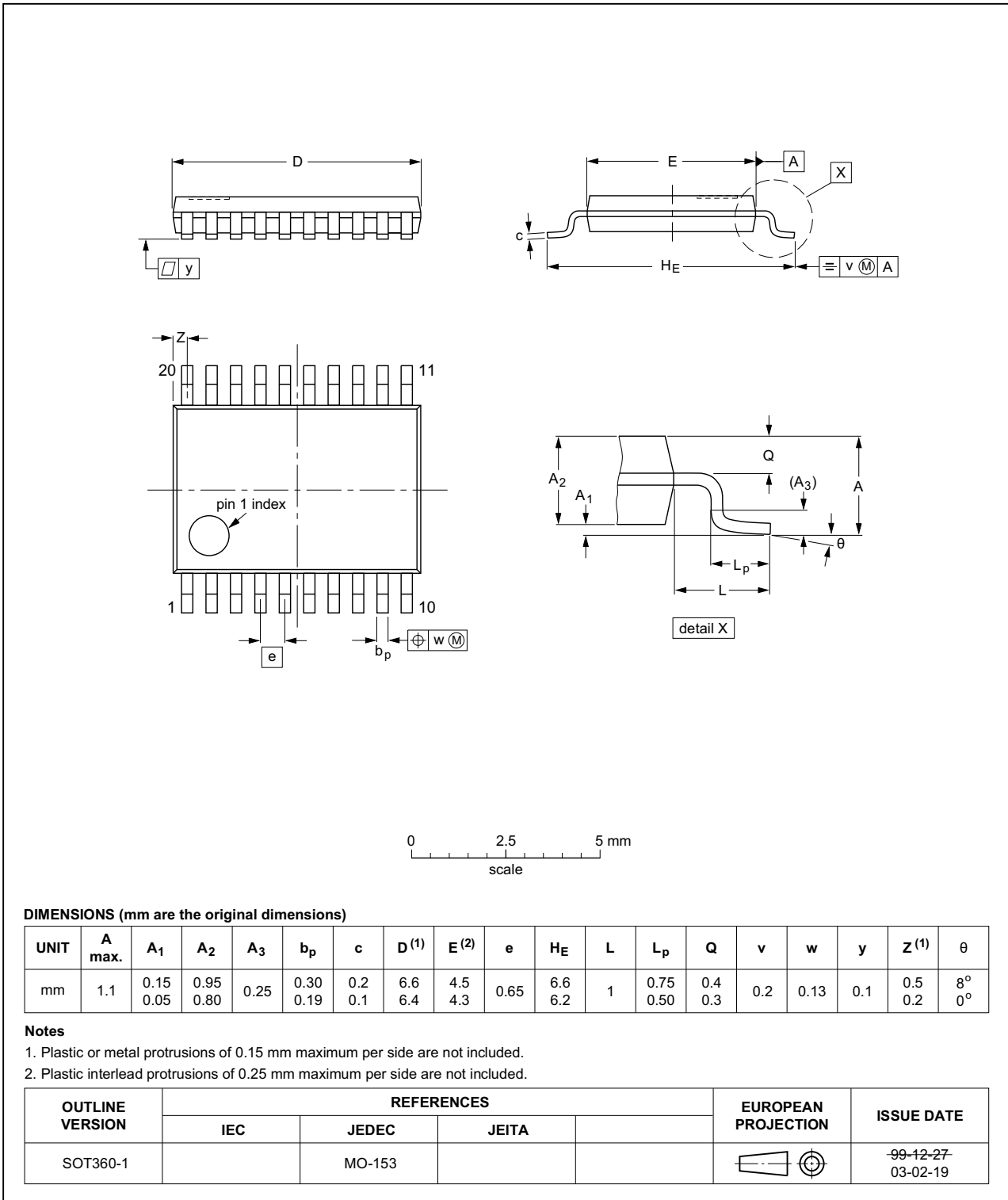


Fig 9. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV244_Q100 v.1	20140519	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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