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Kind regards,

Team Nexperia

74LVT162374

3.3 V 16-bit edge-triggered D-type flip-flop with 30 Ω termination resistors; 3-state

Rev. 03 — 17 January 2005 Product data sheet

1. General description

The 74LVT162374 is a high performance BiCMOS product designed for V_{CC} operation at 3.3 V.

The 74LVT162374 is designed with 30 Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

This device is a 16-bit edge-triggered D-type flip-flop featuring non-inverting 3-state outputs. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CP), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

2. Features

- 16-bit edge-triggered flip-flop
- 3-state buffers
- Output capability: +12 mA and –12 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Outputs include series resistance of 30 Ω making external resistors unnecessary
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - Machine model: exceeds 200 V

PHILIPS

3. Quick reference data

Table 1: Quick reference data

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}, t_{PHL}	propagation delay nCP to nQn	C_L = 50 pF; V_{CC} = 3.3 V	-	3.0	-	ns
C_I	input capacitance	V_I = 0 V or 3.0 V	-	3	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or 3.0 V	-	9	-	pF
I_{CC}	supply current	outputs disabled; V_{CC} = 3.6 V	-	70	-	µA

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT162374DGG	–40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVT162374DL	–40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1

5. Functional diagram

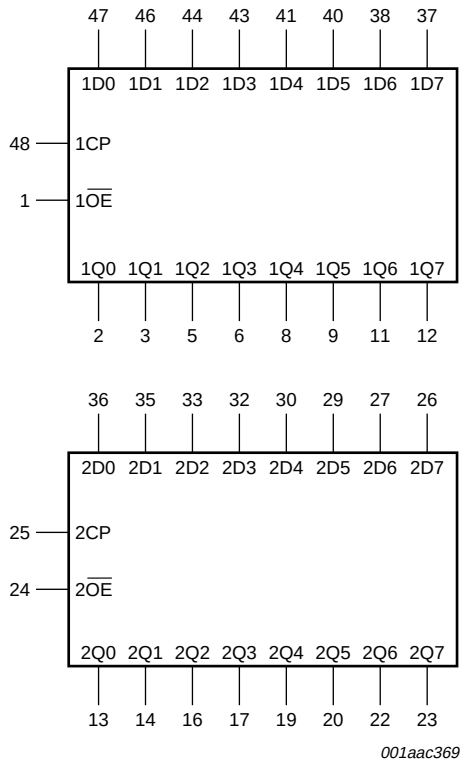


Fig 1. Logic symbol

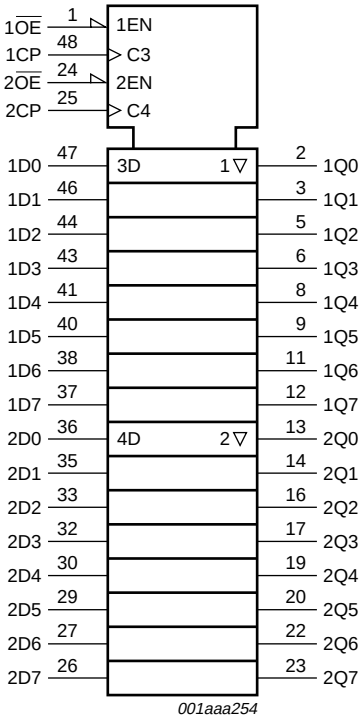


Fig 2. IEC logic symbol

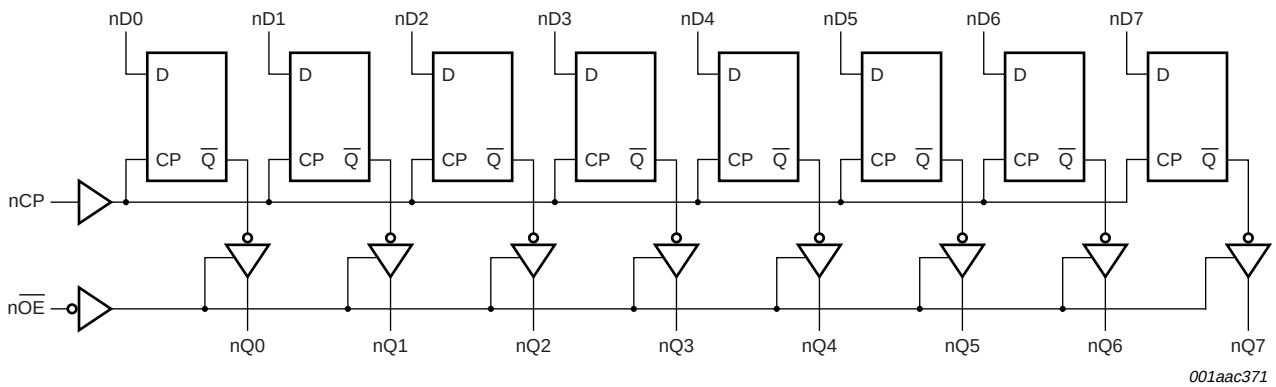


Fig 3. Logic diagram

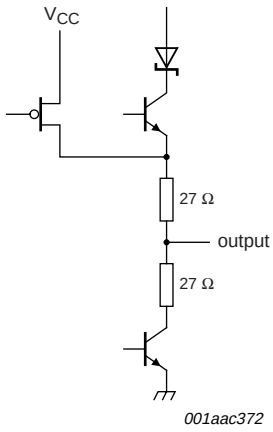


Fig 4. Output schematic (one output)

6. Pinning information

6.1 Pinning

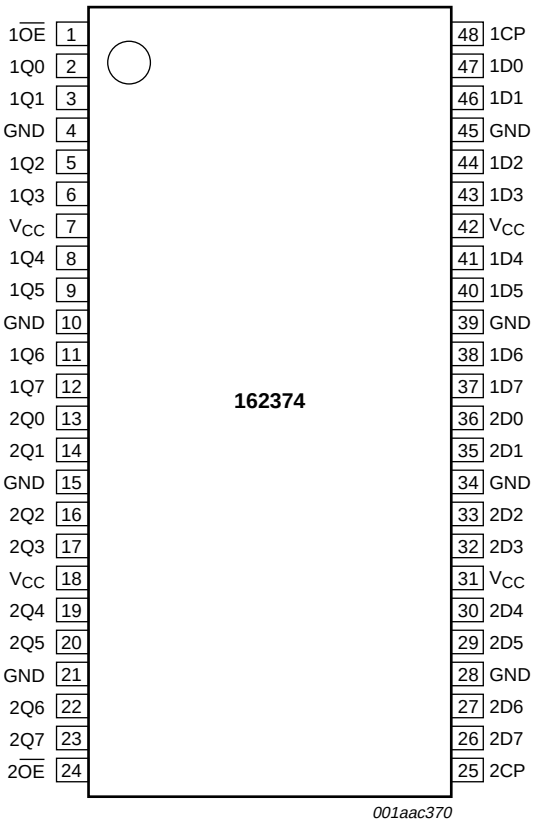


Fig 5. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	output enable input (active LOW)
1Q0	2	data output
1Q1	3	data output
GND	4	ground (0 V)
1Q2	5	data output
1Q3	6	data output
V_{CC}	7	supply voltage
1Q4	8	data output
1Q5	9	data output
GND	10	ground (0 V)
1Q6	11	data output
1Q7	12	data output
2Q0	13	data output
2Q1	14	data output
GND	15	ground (0 V)
2Q2	16	data output
2Q3	17	data output
V_{CC}	18	supply voltage
2Q4	19	data output
2Q5	20	data output
GND	21	ground (0 V)
2Q6	22	data output
2Q7	23	data output
$2\overline{OE}$	24	output enable input (active LOW)
2CP	25	clock pulse input (active rising edge)
2D7	26	data input
2D6	27	data input
GND	28	ground (0 V)
2D5	29	data input
2D4	30	data input
V_{CC}	31	supply voltage
2D3	32	data input
2D2	33	data input
GND	34	ground (0 V)
2D1	35	data input
2D0	36	data input
1D7	37	data input
1D6	38	data input
GND	39	ground (0 V)

Table 3: Pin description

Symbol	Pin	Description
1D5	40	data input
1D4	41	data input
V_{CC}	42	supply voltage
1D3	43	data input
1D2	44	data input
GND	45	ground (0 V)
1D1	46	data input
1D0	47	data input
1CP	48	clock pulse input (active rising edge)

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Input			Internal register	Output
	$n\overline{OE}$	nCP	nDn		nQ0 to nQ7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Hold	L	NC	X	NC	NC
Disable outputs	H	NC	X	NC	Z
	H	↑	nDn	nDn	Z

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;
NC = no change;
X = don't care;
Z = high-impedance OFF-state;
↑ = LOW-to-HIGH clock transition.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
I_{IK}	input diode current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+7.0	V
I_{OK}	output diode current	$V_O < 0$ V		–50	-	mA
V_O	output voltage	output in OFF-state or HIGH-state	[1]	–0.5	+7.0	V

Table 5: Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
I_O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	–64	mA
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[2]		150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input diode voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	–12	mA
I_{OL}	LOW-level output current		-	-	12	mA
$\Delta t/\Delta V$	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
T_{amb}	ambient temperature		–40	-	+85	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
V_{IK}	input clamp voltage	V_{CC} = 2.7 V; I_{IK} = –18 mA	-	–0.85	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 3.0 V; I_{OH} = –12 mA	2.0	-	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 3.0 V; I_{OL} = 12 mA	-	-	0.8	V
V_{RST}	power-up output low voltage	V_{CC} = 3.6 V; I_O = 1 mA; V_I = GND or V_{CC} [2]	-	0.1	0.55	V
I_{LI}	input leakage current					
	control pins	V_{CC} = 3.6 V; V_I = V_{CC} or GND	-	0.1	±1	µA
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	0.4	10	µA
	I/O data pins	V_{CC} = 3.6 V; V_I = V_{CC}	-	0.1	1	µA
		V_{CC} = 3.6 V; V_I = 0 V	-	–0.4	–5	µA
I_{OFF}	output off current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V	-	0.1	±100	µA

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{HOLD}	bus hold current D inputs	V_{CC} = 3 V; V_I = 0.8 V	[4]	75	135	-	µA
		V_{CC} = 3 V; V_I = 2.0 V		–75	–135	-	µA
		V_{CC} = 0 V to 3.6 V; V_I = 3.6 V		±500	-	-	µA
I_{EX}	external current into output	output in HIGH-state when $V_O > V_{CC}$; measured at V_O = 5.5 V and V_{CC} = 3.0 V		-	50	125	µA
I_{PU}, I_{PD}	power-up or power-down 3-state output current	$V_{CC} \leq$ 1.2 V; V_O = 5.0 V to V_{CC}; V_I = GND or V_{CC}; $n\overline{OE}$ and nOE = don't care	[5]	-	1	±100	µA
I_{OZH}	3-state output HIGH current	V_{CC} = 3.6 V; V_O = 3.0 V; $V_I = V_{IH}$ or V_{IL}		-	0.5	5	µA
I_{OZL}	3-state output LOW current	V_{CC} = 3.6 V; V_O = 0.5 V; $V_I = V_{IH}$ or V_{IL}		-	+0.5	–5	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A					
		outputs HIGH		-	0.07	0.12	mA
		outputs LOW		-	4	6	mA
		outputs disabled	[6]	-	0.07	0.12	mA
ΔI_{CC}	additional supply current per input pin	V_{CC} = 3 V to 3.6 V; one input at V_{CC} – 0.6 V; other inputs at V_{CC} or GND	[7]	-	0.1	0.2	mA
C_I	input capacitance	V_I = 0 V or 3.0 V		-	3	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or 3.0 V		-	9	-	pF

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

[3] Unused pins at V_{CC} or GND.

[4] This is the bus-hold overdrive current required to force the input to the opposite logic state.

[5] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.

[6] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
f_{max}	maximum clock frequency	V_{CC} = 3.3 V ± 0.3 V; see Figure 6	150	-	-	MHz
t_{PLH}	propagation delay nCP to nQn	see Figure 6				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.0	5.3	ns
		V_{CC} = 2.7 V	-	-	6.2	ns

Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}	propagation delay nCP to nQn	see Figure 6				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.0	4.9	ns
		V_{CC} = 2.7 V	-	-	5.1	ns
t_{PZH}	output enable time to HIGH-level	see Figure 7				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.5	5.6	ns
		V_{CC} = 2.7 V	-	-	6.9	ns
t_{PZL}	output enable time to LOW-level	see Figure 8				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.2	4.9	ns
		V_{CC} = 2.7 V	-	-	6.0	ns
t_{PHZ}	output disable time from HIGH-level	see Figure 7				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.5	5.4	ns
		V_{CC} = 2.7 V	-	-	5.7	ns
t_{PLZ}	output disable time from LOW-level	see Figure 8				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.2	5.0	ns
		V_{CC} = 2.7 V	-	-	5.1	ns

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

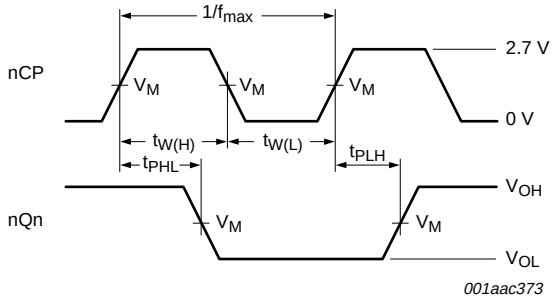
Table 9: Dynamic characteristics set-up requirements

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
$t_{su(H)}$, $t_{su(L)}$	set-up time nDn to nCP	see Figure 9				
		V_{CC} = 3.3 V ± 0.3 V	2.0	0.7	-	ns
		V_{CC} = 2.7 V	2.0	-	-	ns
$t_{h(H)}$, $t_{h(L)}$	hold time nDn to nCP	see Figure 9				
		V_{CC} = 3.3 V ± 0.3 V	0.8	0	-	ns
		V_{CC} = 2.7 V	0.1	-	-	ns
$t_{W(H)}$	nCP pulse width HIGH	see Figure 6				
		V_{CC} = 3.3 V ± 0.3 V	1.5	0.6	-	ns
		V_{CC} = 2.7 V	1.5	-	-	ns
$t_{W(L)}$	nCP pulse width LOW	see Figure 6				
		V_{CC} = 3.3 V ± 0.3 V	3.0	1.6	-	ns
		V_{CC} = 2.7 V	3.0	-	-	ns

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

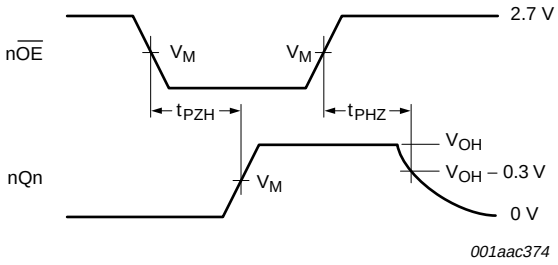
12. Waveforms



V_M = 1.5 V; V_I = GND to 3.0 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

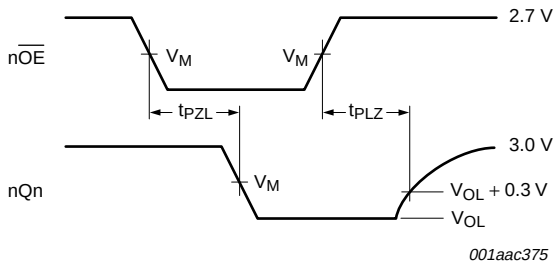
Fig 6. Propagation delay clock input to output, clock pulse width and maximum clock frequency



V_M = 1.5 V; V_I = GND to 3.0 V.

V_{OH} is typical voltage output drop that occur with the output load.

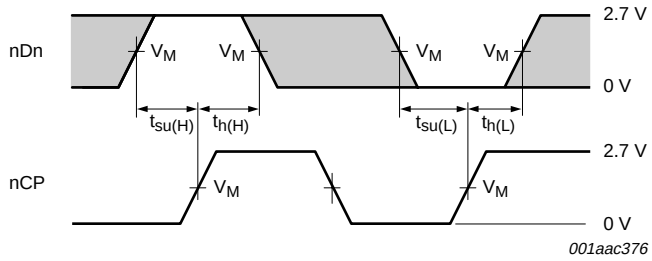
Fig 7. 3-state output enable time to HIGH-level and output disable time from HIGH-level



V_M = 1.5 V; V_I = GND to 3.0 V.

V_{OL} is typical voltage output drop that occur with the output load.

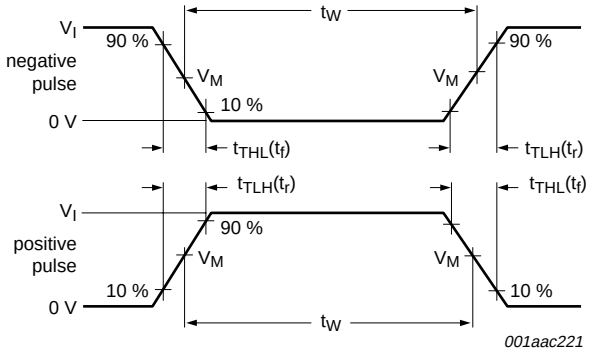
Fig 8. 3-state output enable time to LOW-level and output disable time from LOW-level



V_M = 1.5 V; V_I = GND to 3.0 V.

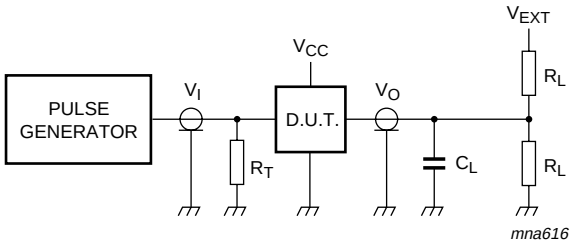
Remark: The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 9. Data set-up and hold times



V_M = 1.5 V.

a. Input pulse definition



Test data is given in Table 10.

Definitions:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

b. Test circuit

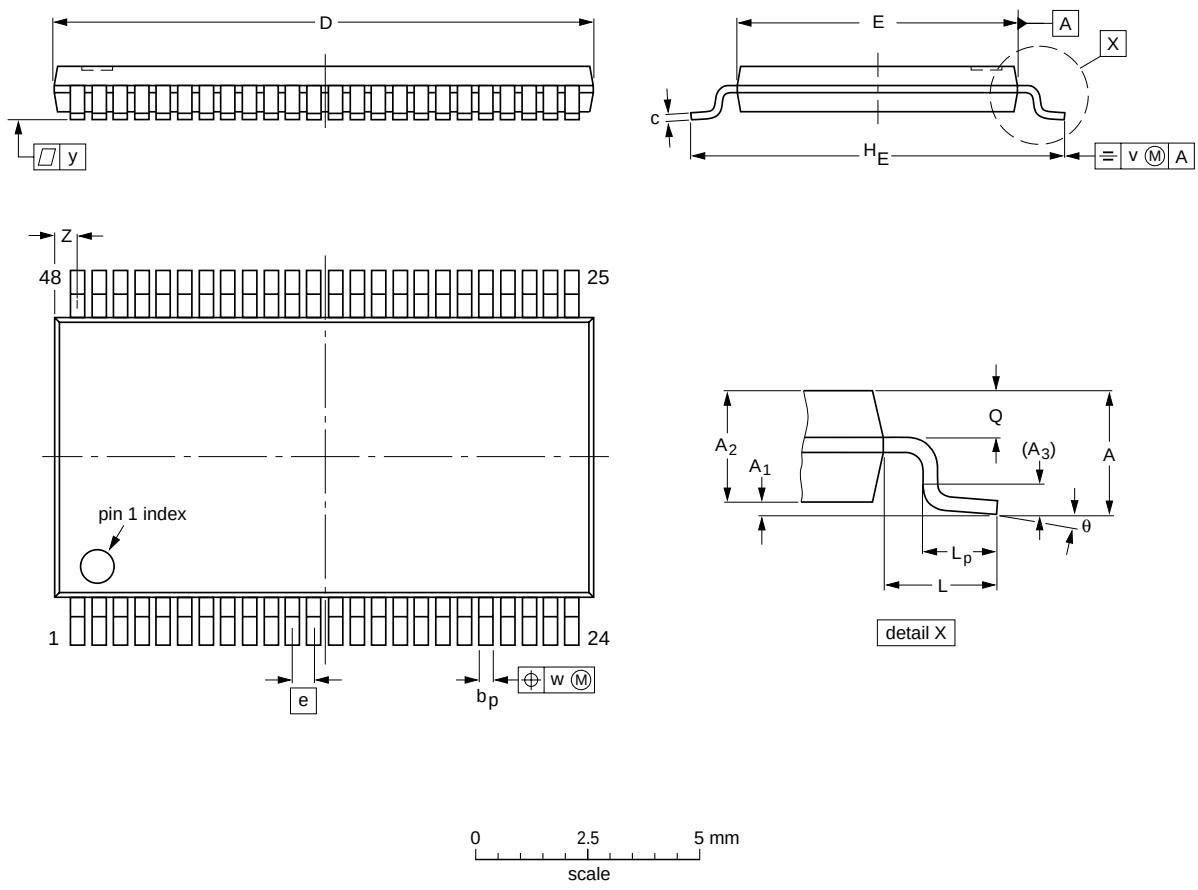
Fig 10. Load circuitry for switching times

Table 10: Test data

Supply voltage	Repetition rate	Input		Load		V_{EXT}		
		t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

13. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

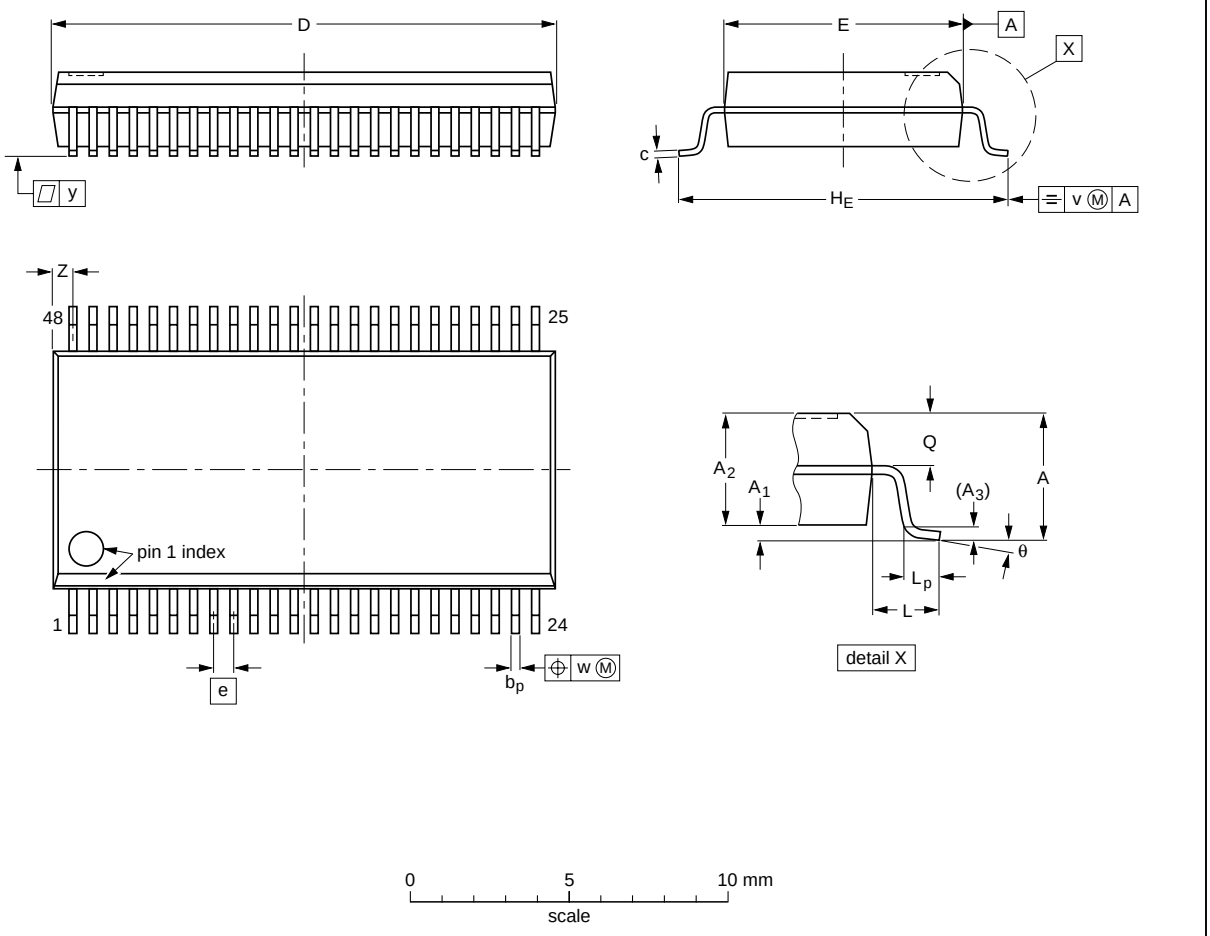
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT362-1 (TSSOP48)

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT370-1 (SSOP48)

14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVT162374_3	20050117	Product data sheet	-	9397 750 14401	74LVT162374_2
Modifications:	• The format of this data sheet is redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Section 2 “Features”: Changed JEDEC Std 17 into JESD78 • Table 1 “Quick reference data”:Changed t_{PLH} and t_{PHL} propagation delays nCP to nQn to 3.0 ns • Table 9 “Dynamic characteristics set-up requirements”: Changed the minimum values of $t_{h(H)}$ and $t_{h(L)}$ hold time nDn to nCP to 0.8 ns				
74LVT162374_2	20040922	Product specification	-	9397 750 14087	74LVT162374_1
74LVT162374_1	19990923	Product specification	-	9397 750 06508	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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18. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

19. Contents

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