

Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use <http://www.nexperia.com>

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use salesaddresses@nexperia.com (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via salesaddresses@nexperia.com). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia



PB5M5240PFH

40 V, 2 A PNP low V_{CEsat} (BISS) transistor with N-channel Trench MOSFET

Rev. 1 — 20 June 2012

Product data sheet

1. Product profile

1.1 General description

Combination of PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor and N-channel Trench Metal-Oxide Semiconductor Field- Effect Transistor (MOSFET). The device is housed in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package.

1.2 Features and benefits

- Very low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High energy efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- Load switch
- Power management
- Power switches (e.g. motors, fans)
- Battery-driven devices
- Charging circuits

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PNP low V_{CEsat} (BISS) transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	-40	V
I_C	collector current		[1]	-	-1.8	A
I_{CRM}	repetitive peak collector current		[1][5]	-	-2	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	[1]	-	-3	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -500$ mA; $I_B = -50$ mA	[2]	-	240	340 m Ω



Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N-channel Trench MOSFET						
V_{DS}	drain-source voltage	$T_{amb} = 25\text{ °C}$	-	-	30	V
V_{GS}	gate-source voltage	$T_{amb} = 25\text{ °C}$	-	-	± 8	V
I_D	drain current	$T_{amb} = 25\text{ °C};$ $V_{GS} = 10\text{ V}$	[3]	-	0.66	A
$R_{DS(on)}$	drain-source on-state resistance	$T_j = 25\text{ °C}; V_{GS} = 4.5\text{ V};$ $I_D = 0.2\text{ A}$	[4]	-	370	580 m Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm².

[2] Pulse test: $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$.

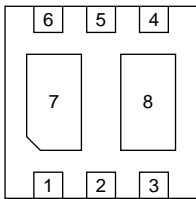
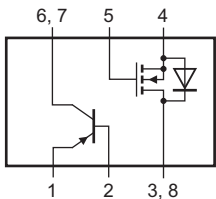
[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

[4] Pulse test: $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.01$.

[5] Pulse test: $t_p \leq 20\text{ ms}; \delta \leq 0.10$.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	emitter	 <p>Transparent top view</p>	 <p>017aaa079</p>
2	base		
3	drain		
4	source		
5	gate		
6	collector		
7	collector		
8	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PBSM5240PFH	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 × 2 × 0.65 mm	SOT1118

4. Marking

Table 4. Marking code

Type number	Marking code
PBSM5240PFH	1T

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

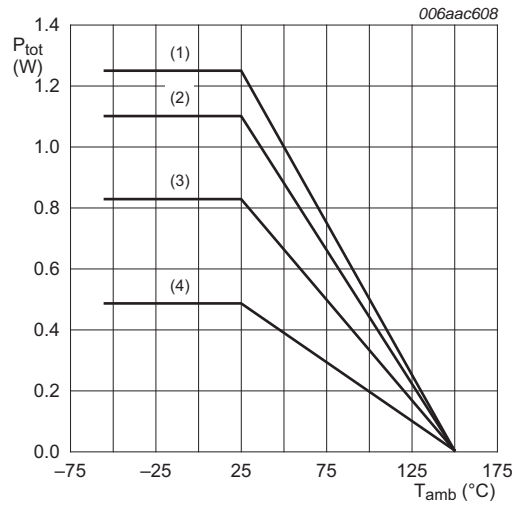
Symbol	Parameter	Conditions	Min	Max	Unit	
PNP low V_{CEsat} (BISS) transistor						
V_{CBO}	collector-base voltage	open emitter	-	-40	V	
V_{CEO}	collector-emitter voltage	open base	-	-40	V	
V_{EBO}	emitter-base voltage	open collector	-	-5	V	
I_C	collector current		[1]	-1.8	A	
I_{CRM}	repetitive peak collector current		[1][4]	-2	A	
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	[1]	-3	A	
I_B	base current		[1]	-300	mA	
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms	[1]	-1	A	
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	1.1	W	
			[2]	1.25	W	
N-channel Trench MOSFET						
V_{DS}	drain-source voltage	$T_{amb} = 25$ °C	-	30	V	
V_{DG}	drain-gate voltage	$T_{amb} = 25$ °C; $R_{GS} = 20$ k Ω	-	30	V	
V_{GS}	gate-source voltage	$T_{amb} = 25$ °C	-	± 8	V	
I_D	drain current	$V_{GS} = 10$ V	[3]			
			$T_{amb} = 25$ °C	-	660	mA
			$T_{amb} = 100$ °C	-	420	mA
I_{DM}	peak drain current	$T_{amb} = 25$ °C; single pulse; $t_p \leq 10$ μ s	-	3.56	A	
P_{tot}	total power dissipation	$T_{amb} = 25$ °C	[3]	760	mW	
Source-drain diode						
I_S	source current	$T_{amb} = 25$ °C	-	660	mA	
Per device						
T_j	junction temperature		-	150	°C	
T_{amb}	ambient temperature		-55	+150	°C	
T_{stg}	storage temperature		-65	+150	°C	

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm².

[2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated, mounting pad for collector 1 cm².

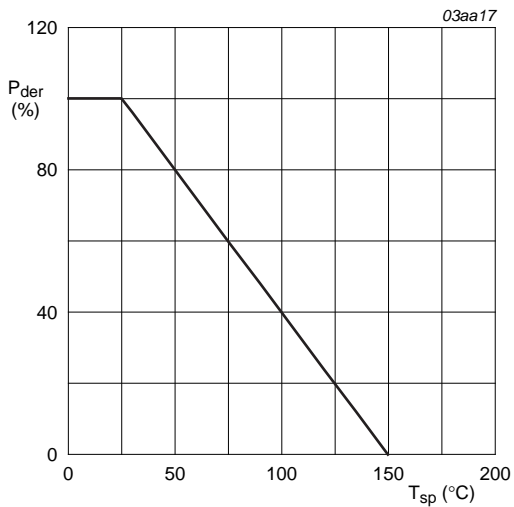
[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

[4] Pulse test: $t_p \leq 20$ ms; $\delta \leq 0.10$.



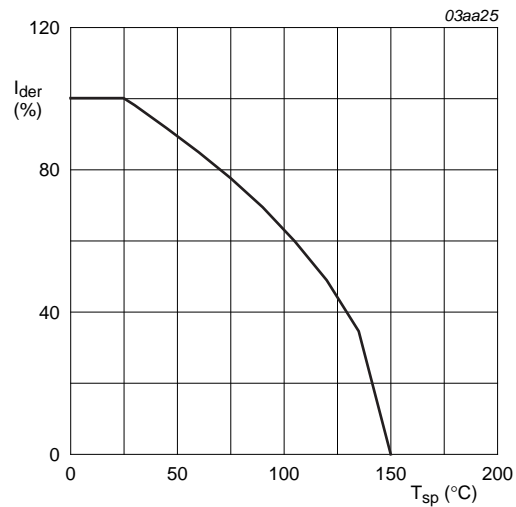
- (1) FR4 PCB, 4-layer copper, mounting pad for collector 1 cm²
- (2) FR4 PCB, single-sided copper, mounting pad for collector 6 cm²
- (3) FR4 PCB, single-sided copper, mounting pad for collector 1 cm²
- (4) FR4 PCB, single-sided copper, standard footprint

Fig 1. BISS transistor: Power derating curves



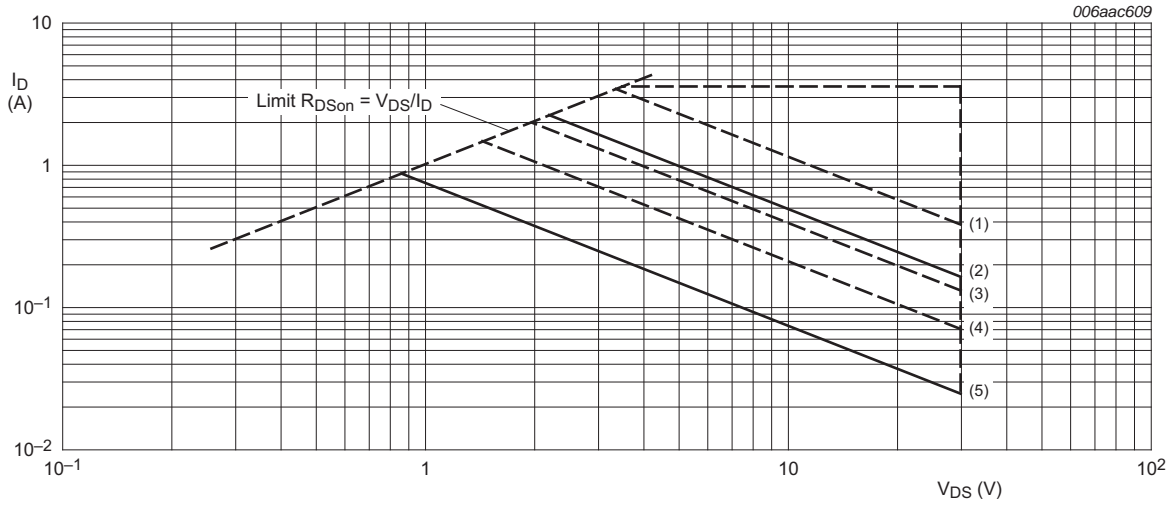
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig 2. MOSFET: Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

Fig 3. MOSFET: Normalized continuous drain current as a function of solder point temperature



- I_{DM} = single pulse
- (1) $t_p = 1$ ms
 - (2) DC; $T_{sp} = 25$ °C
 - (3) $t_p = 10$ ms
 - (4) $t_p = 100$ ms
 - (5) DC; $T_{amb} = 25$ °C; drain mounting pad 1 cm²

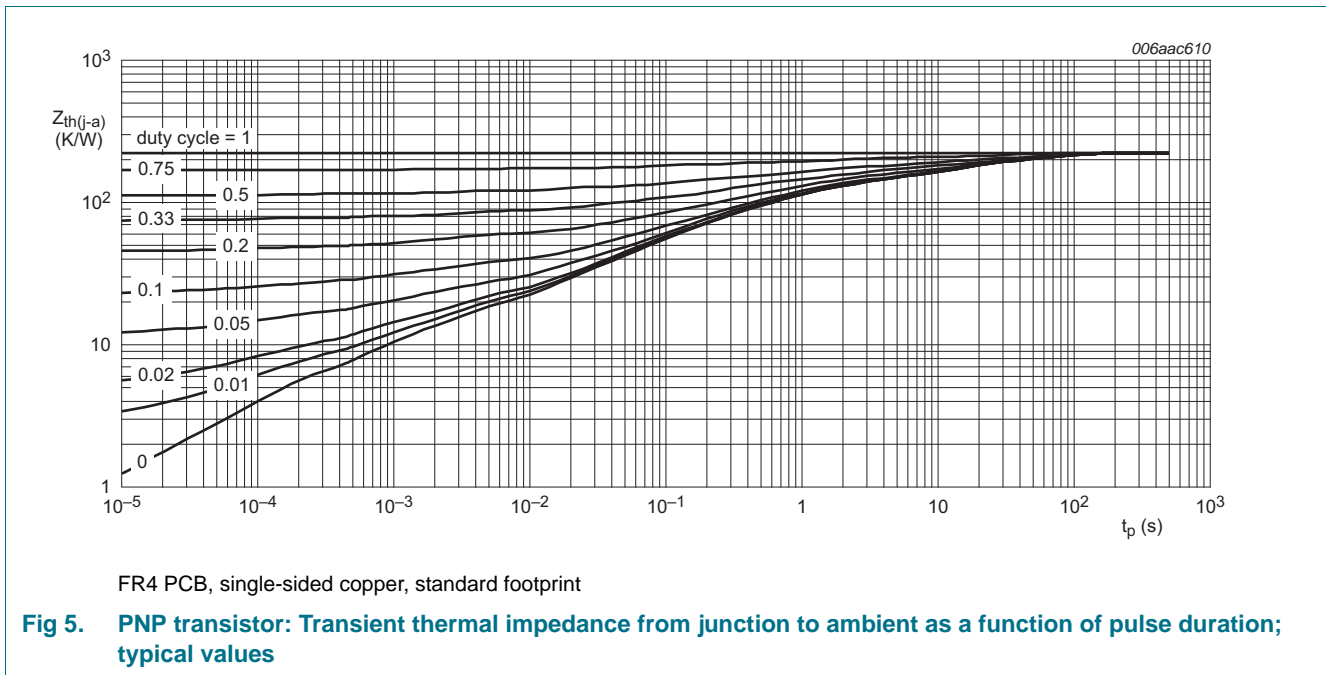
Fig 4. MOSFET: Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

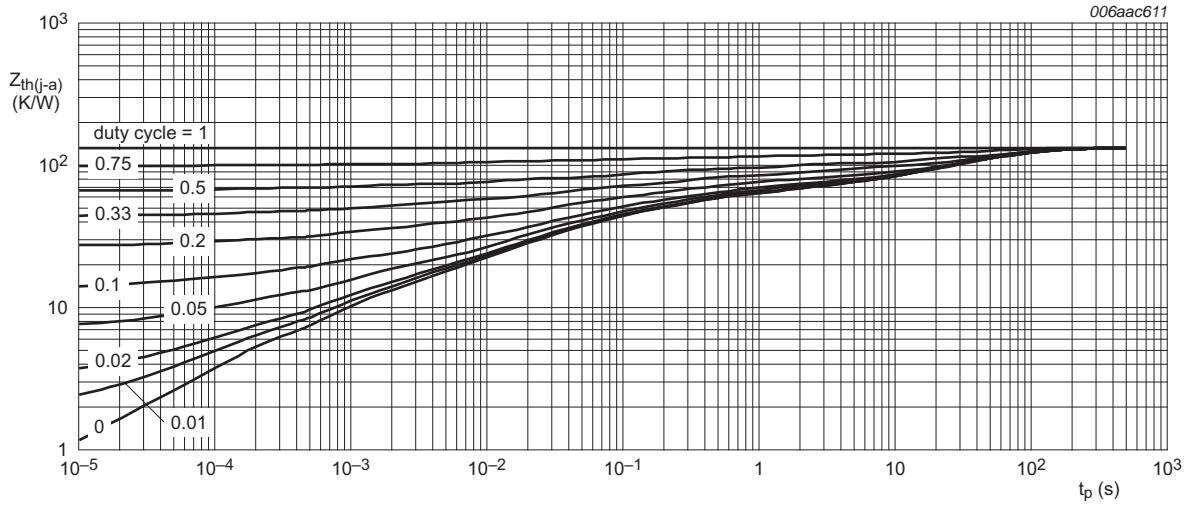
6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
PNP low V_{CEsat} (BISS) transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	115	K/W
			[2]	-	-	100	K/W
N-channel Trench MOSFET							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[3]	-	-	165	K/W

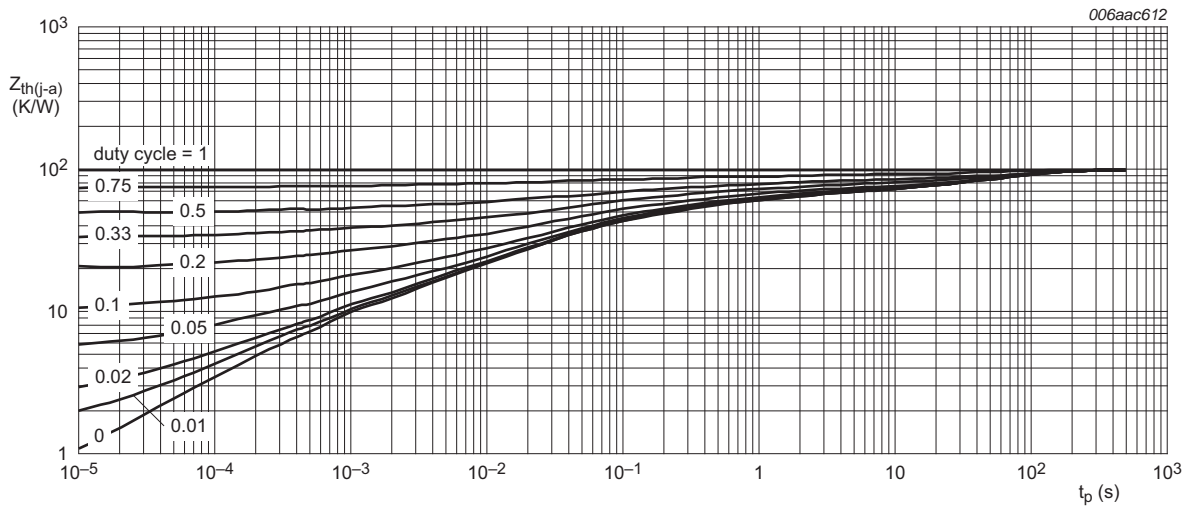
- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm².
- [2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².





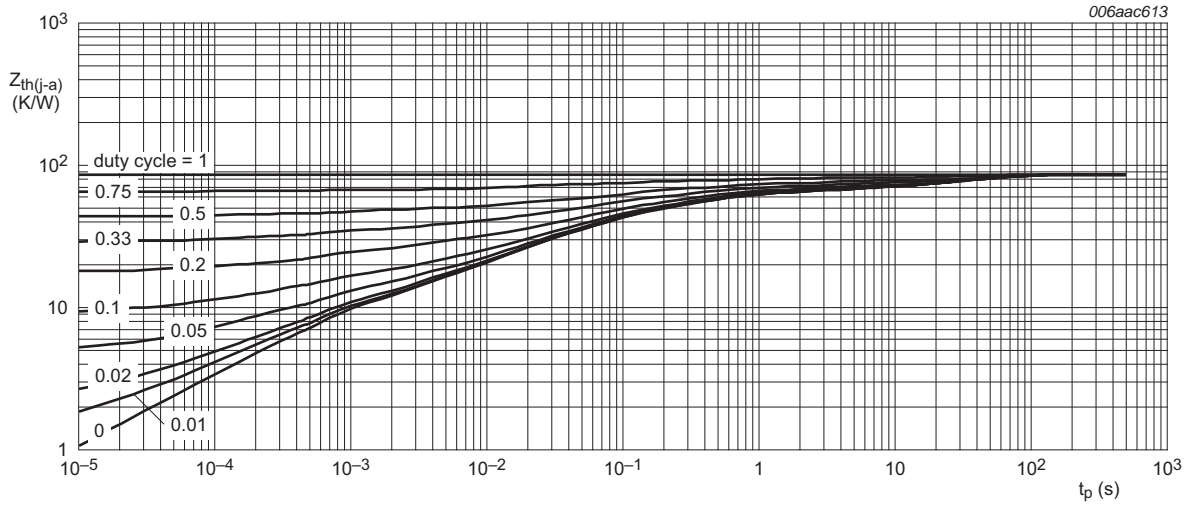
FR4 PCB, single-sided copper, mounting pad for collector 1 cm²

Fig 6. PNP transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



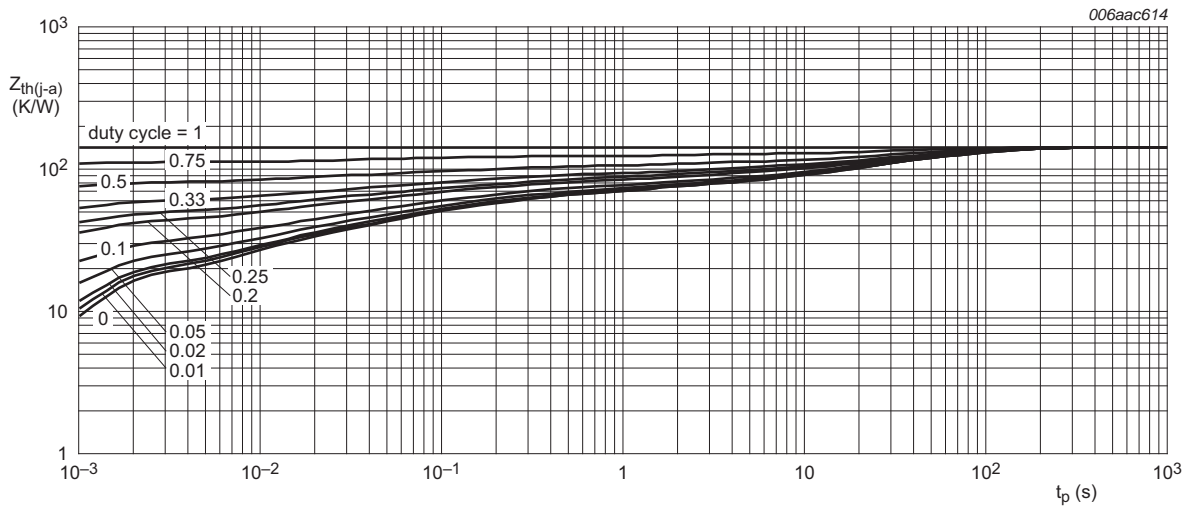
FR4 PCB, single-sided copper, mounting pad for collector 6 cm²

Fig 7. PNP transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, mounting pad for collector 1 cm²

Fig 8. PNP transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, single-sided copper, mounting pad for drain 1 cm²

Fig 9. MOSFET: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

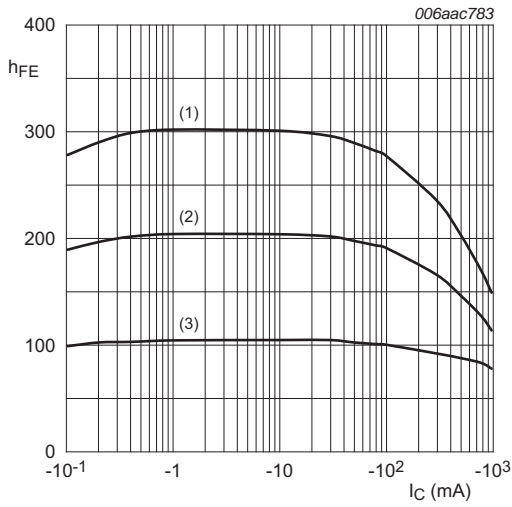
7. Characteristics

Table 7. Characteristics for PNP low V_{CEsat} transistor

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

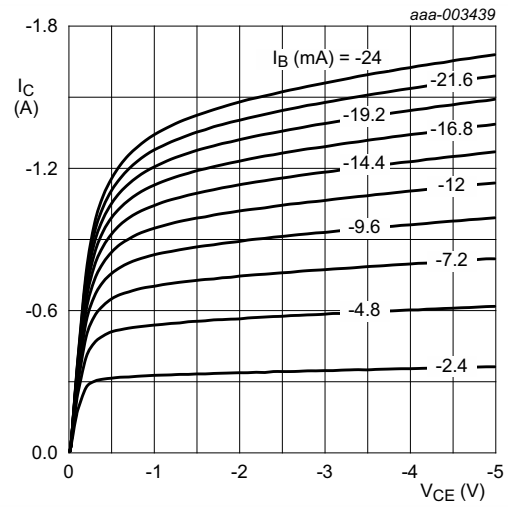
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
I_{CBO}	collector-base cut-off current	$V_{CB} = -30\text{ V}; I_E = 0\text{ A}$	-	-	-100	nA	
		$V_{CB} = -30\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	-50	μA	
I_{CES}	collector-emitter cut-off current	$V_{CE} = -30\text{ V}; I_B = 0\text{ A}$	-	-	-100	nA	
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	-	-	-100	nA	
h_{FE}	DC current gain	$V_{CE} = -5\text{ V}$	[1]				
		$I_C = -1\text{ mA}$	100	-	-		
		$I_C = -100\text{ mA}$	100	-	-		
		$I_C = -1\text{ A}$	75	-	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = -100\text{ mA}; I_B = -1\text{ mA}$	[1]	-	-85	-140	mV
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	[1]	-	-120	-170	mV
		$I_C = -1\text{ A}; I_B = -100\text{ mA}$	[1]	-	-200	-310	mV
R_{CEsat}	collector-emitter saturation resistance	$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	[1]	-	240	340	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = -1\text{ A}; I_B = -100\text{ mA}$	[1]	-	-	-1.1	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -5\text{ V}; I_C = -1\text{ A}$	[1]	-	-	-1	V
f_T	transition frequency	$V_{CE} = -10\text{ V}; I_C = -50\text{ mA}; f = 100\text{ MHz}$	100	-	-		MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0\text{ A}; f = 1\text{ MHz}$	-	-	15		pF

[1] Pulse test: $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$.



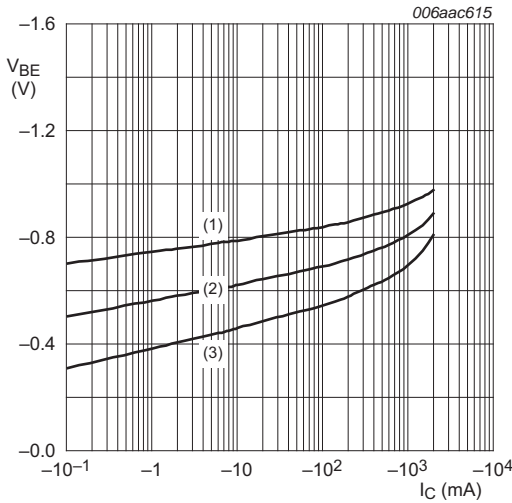
$V_{CE} = -5\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 10. PNP transistor: DC current gain as a function of collector current; typical values



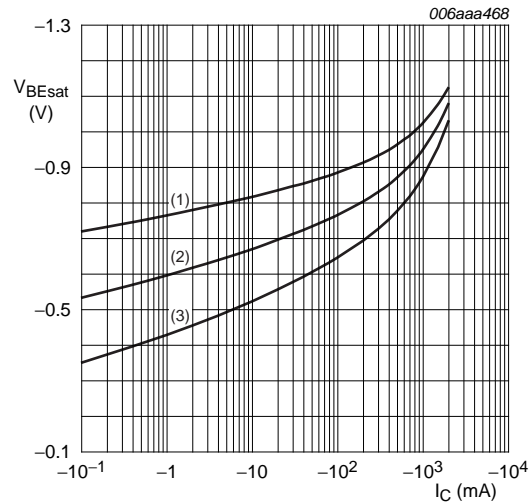
$T_{amb} = 25\text{ °C}$

Fig 11. PNP transistor: Collector current as a function of collector-emitter voltage; typical values



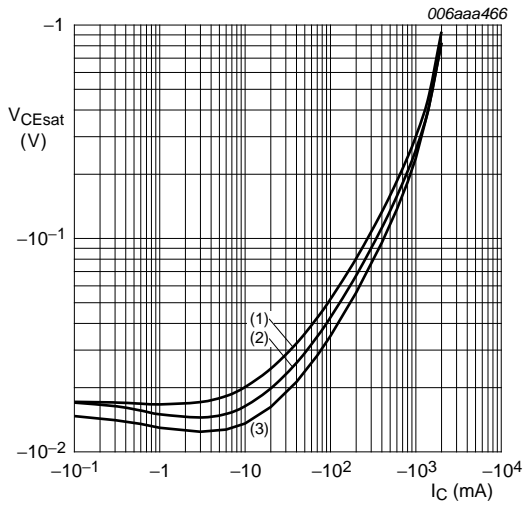
$V_{CE} = -5\text{ V}$
 (1) $T_{amb} = -55\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 12. PNP transistor: Base-emitter voltage as a function of collector current; typical values



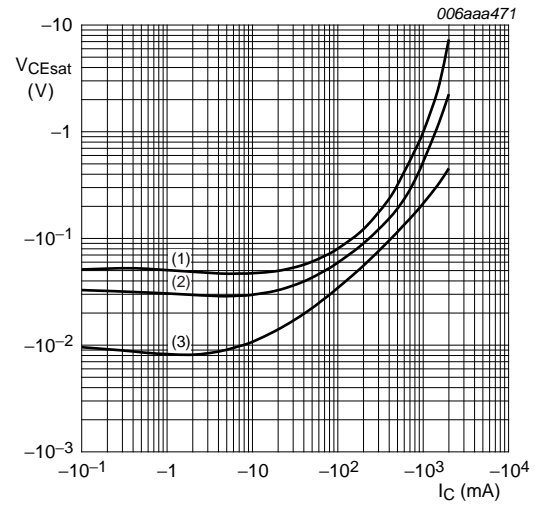
$I_C/I_B = 20$
 (1) $T_{amb} = -55\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 13. PNP transistor: Base-emitter saturation voltage as a function of collector current; typical values



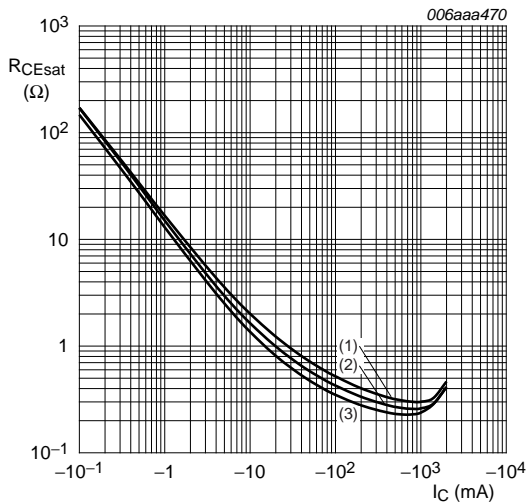
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 14. PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values



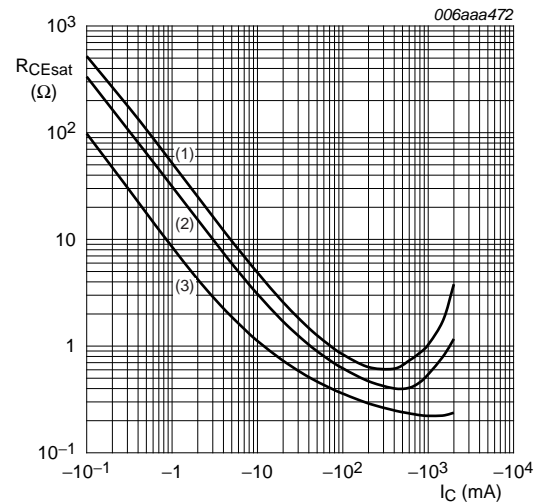
$T_{amb} = 25\text{ °C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig 15. PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values



$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 16. PNP transistor: Collector-emitter saturation resistance as a function of collector current; typical values



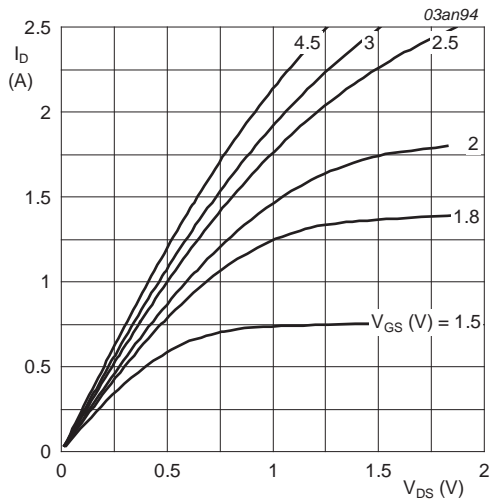
$T_{amb} = 25\text{ °C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig 17. PNP transistor: Collector-emitter saturation resistance as a function of collector current; typical values

Table 8. Characteristics for N-channel Trench MOSFET*T_j = 25 °C unless otherwise specified.*

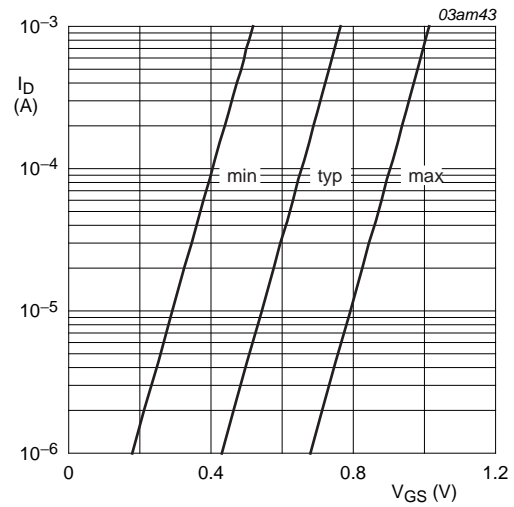
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 10 μA; V _{GS} = 0 V				
		T _j = 25 °C	30	-	-	V
		T _j = -55 °C	27	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS}				
		T _j = 25 °C	0.45	0.7	0.95	V
		T _j = 150 °C	0.25	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V				
		T _j = 25 °C	-	-	1	μA
		T _j = 150 °C	-	-	100	μA
I _{GSS}	gate leakage current	V _{GS} = ±8 V; V _{DS} = 0 V	-	10	±100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 0.2 A [1]				
		T _j = 25 °C	-	370	580	mΩ
		T _j = 150 °C	-	663	985	mΩ
		V _{GS} = 2.5 V; I _D = 0.1 A	-	440	690	mΩ
		V _{GS} = 1.8 V; I _D = 75 mA	-	540	920	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 1 A; V _{DS} = 15 V;	-	0.89	-	nC
Q _{GS}	gate-source charge	V _{GS} = 4.5 V	-	0.1	-	nC
Q _{GD}	gate-drain charge		-	0.2	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V;	-	43	-	pF
C _{oss}	output capacitance	f = 1 MHz	-	7.7	-	pF
C _{rss}	reverse transfer capacitance		-	4.8	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 15 V; R _L = 15 Ω;	-	4.0	-	ns
t _r	rise time	V _{GS} = 10 V; R _G = 6 Ω	-	7.5	-	ns
t _{d(off)}	turn-off delay time		-	18	-	ns
t _f	fall time		-	4.5	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 0.3 A; V _{GS} = 0 V	-	0.76	1.2	V

[1] Pulse test: t_p ≤ 300 μs; δ ≤ 0.01.



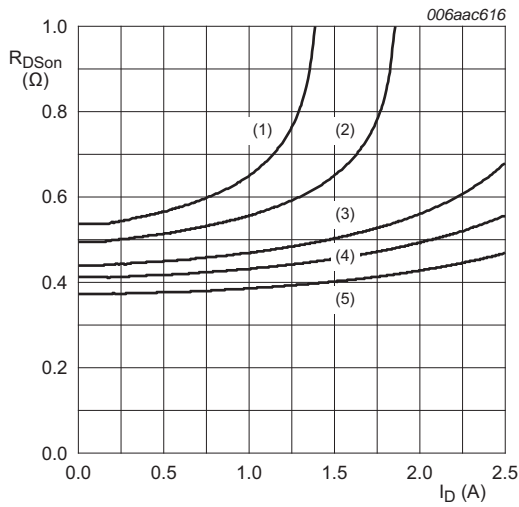
$T_j = 25\text{ }^\circ\text{C}$

Fig 18. MOSFET: Output characteristics: drain current as a function of drain-source voltage; typical values



$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$

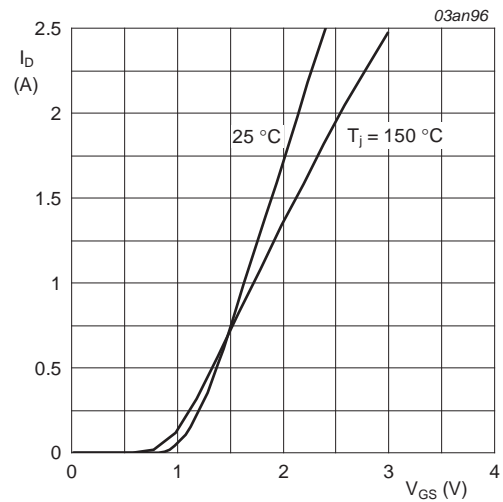
Fig 19. MOSFET: Subthreshold drain current as a function of gate-source voltage



$T_j = 25\text{ }^\circ\text{C}$

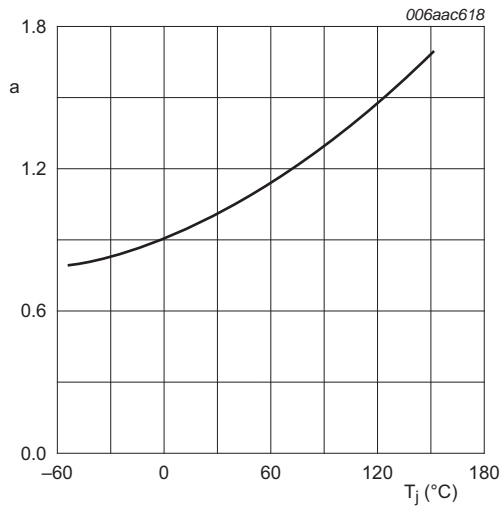
- (1) $V_{GS} = 1.8\text{ V}$
- (2) $V_{GS} = 2.0\text{ V}$
- (3) $V_{GS} = 2.5\text{ V}$
- (4) $V_{GS} = 3.0\text{ V}$
- (5) $V_{GS} = 4.5\text{ V}$

Fig 20. MOSFET: Drain-source on-state resistance as a function of drain current; typical values



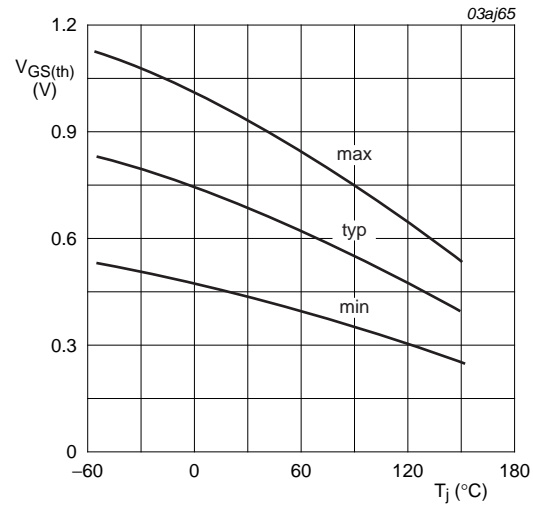
$V_{DS} > I_D \times R_{DSon}$

Fig 21. MOSFET: Transfer characteristics: drain current as a function of gate-source voltage; typical values



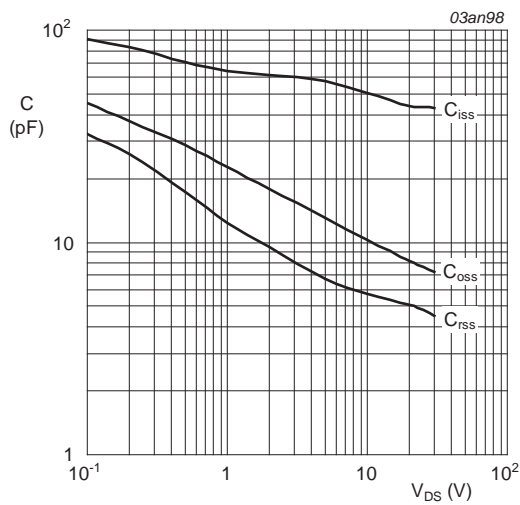
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 22. MOSFET: Normalized drain-source on-state resistance as a function of junction temperature; typical values



$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 23. MOSFET: Gate-source threshold voltage as a function of junction temperature



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

Fig 24. MOSFET: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

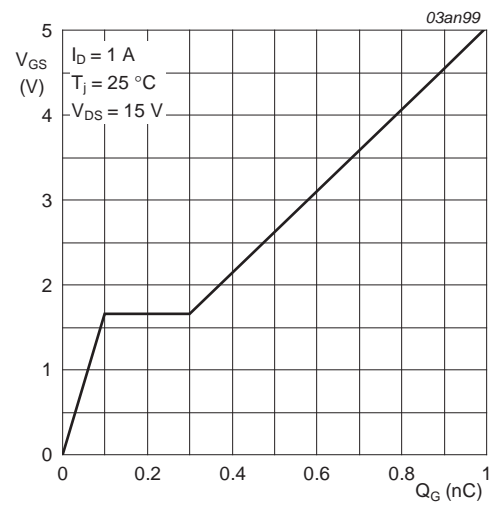


Fig 25. MOSFET: Gate-source voltage as a function of gate charge; typical values

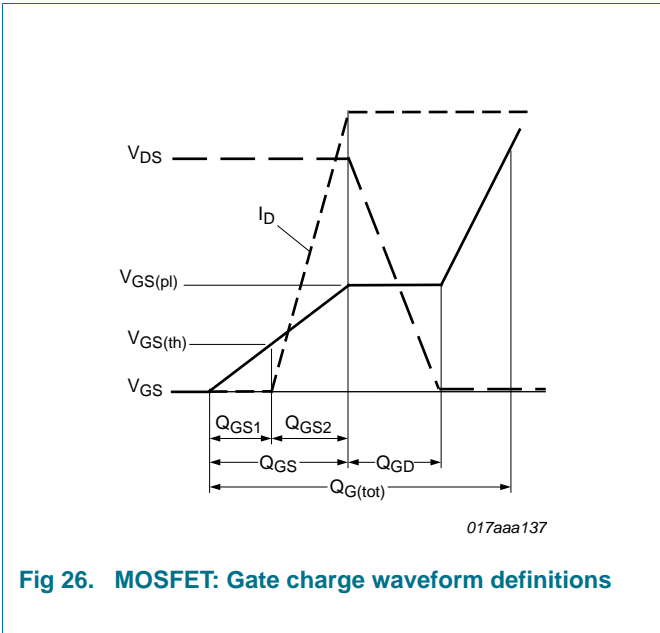


Fig 26. MOSFET: Gate charge waveform definitions

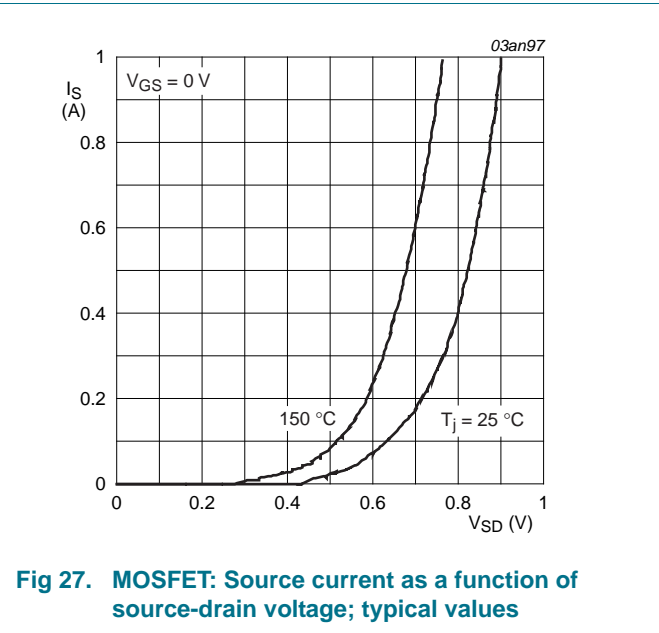


Fig 27. MOSFET: Source current as a function of source-drain voltage; typical values

8. Package outline

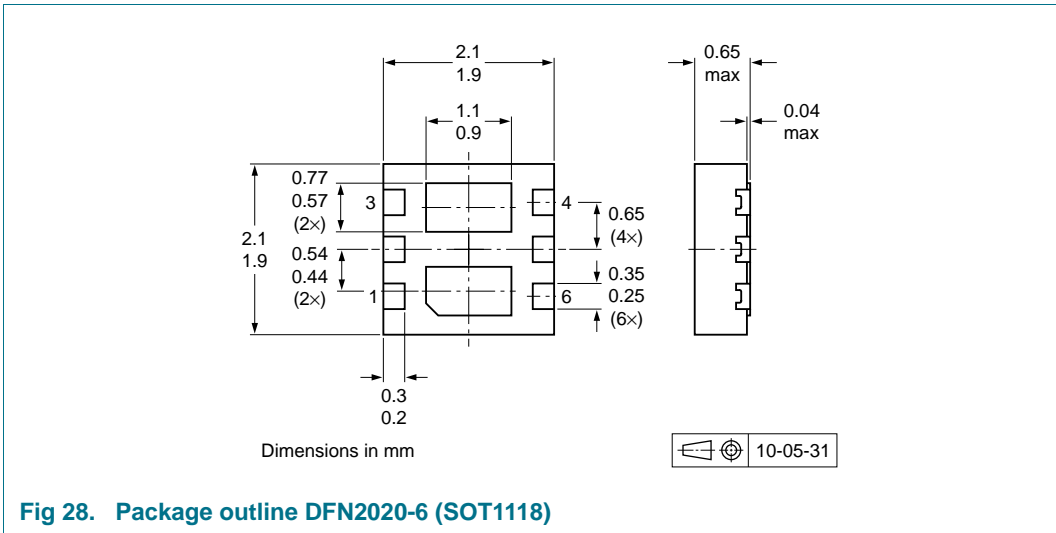


Fig 28. Package outline DFN2020-6 (SOT1118)

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity
PBSM5240PFH	DFN2020-6 (SOT1118)	4 mm pitch, 8 mm tape and reel	3000 -115

[1] For further information and the availability of packing methods, see Section 13.

10. Soldering

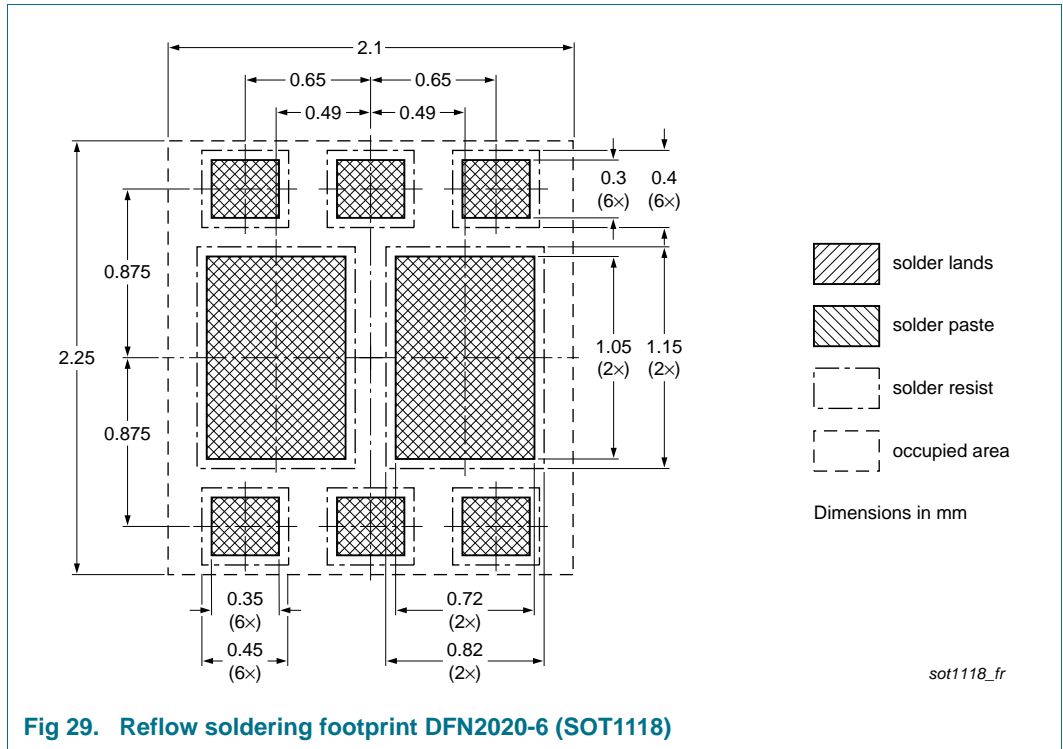


Fig 29. Reflow soldering footprint DFN2020-6 (SOT1118)

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PB5M5240PFH v.1	20120620	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

12.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

13. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

14. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Marking	2
5	Limiting values	3
6	Thermal characteristics	6
7	Characteristics	9
8	Package outline	15
9	Packing information	15
10	Soldering	16
11	Revision history	17
12	Legal information	18
12.1	Data sheet status	18
12.2	Definitions	18
12.3	Disclaimers	18
12.4	Trademarks	19
13	Contact information	19
14	Contents	20

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 20 June 2012

Document identifier: PBSM5240PFH