The NA853C is a core version of the high-performance V853 microcontroller that employs the advanced 32-bit RISC engine of NEC’s V850™ family and is suitable for real-time control applications with 38 Dhrystone MIPS of performance. The NA853C is supported by NEC’s 0.35-µm CMOS process technology and enables designers to specify the amount of on-board ROM, RAM, and flash memory. The architecture of the V853 is highly optimized for fast DSP-like operation and very efficient implementation of C programmability.

The NA853 core is fully supported by NEC’s sophisticated OpenCAD® design framework that combines popular third-party design tools with proprietary NEC tools, including advanced floorplanner and clock tree synthesis tools. A wide range of OpenCAD macros is available, including A/D and D/A converters, watchdog timer, I2C™ interface, parallel/serial controllers, and universal serial bus. NEC’s CB-C9 Titanium-Silicide process achieves 1.6 million usable gates with a 3.3V power supply and features a 5V tolerance interface with exceptionally low power dissipation (0.7 µW/MHz/gate).

**V853 ™ 32-BIT RISC MICROCONTROLLER CORE**

**NA853C**

Block Diagram
FEATURE DESCRIPTION

CPU
- 38 Dhrystone MIPS at 33 MHz
- Highly integrated microcontroller
  - 32-bit arithmetic logic unit (ALU)
  - Thirty-two general-purpose 32-bit registers
  - 32-bit barrel shifter
  - Single-cycle 16 x 16 -> 32-bit hardware multiplier
  - Powerful RISC instruction set
    - 74 RISC instructions: 16- and 32-bit
    - Two-cycle MAC function for DSP applications
    - Saturated operation instructions (over/underflow detection)
    - Single-cycle 32-bit shift instructions
    - Bit manipulation instructions
    - Load and store instructions with 8-/16-/32-bit data
  - Fast instruction execution: 30 ns at 33 MHz

MEMORY
- User-specifiable single-cycle internal flash memory or ROM
- User-specifiable single-cycle internal RAM

EXTERNAL BUS INTERFACE
- Multiplexed 24-bit address/16-bit data bus
- Multiple bus mastership
- 16-MB linear address space external expansion
- Programmable and external wait functions
- Idle state insertion for slow memory

INTERRUPTS
- 32 software traps
- 32 maskable interrupts plus NMI
- Eight programmable priority levels on all interrupts and traps
- Specifiable rising and/or falling edge detection

PERIPHERALS
- Real-time pulse unit
  - Four-channel 16-bit timer/event counter
  - Sixteen 16-bit capture/compare registers
  - Four 16-bit timers
  - One-channel 16-bit interval timer
- Serial interface
  - UART: two channels
  - Clocked serial interface: two to four channels
  - Dedicated baud rate generator: three channels
- Analog interface
  - Eight-channel A/D converter with 10-bit resolution
  - Two-channel D/A converter with 8-bit resolution
  - Two-channel pulse-width modulator with 8-/9/10-/12-bit resolution

TESTABILITY
- Dedicated test pin for each core pin
- Core isolated from user logic and tested through test bus

OTHER
- Power saving features
  - Halt/stop modes
  - Clock output stop function
  - Fully static operation

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