

National Semiconductor is now part of  
Texas Instruments.

Search <http://www.ti.com/> for the latest technical  
information and details on our current products and services.

## 54AC574 • 54ACT574 Octal D-Type Flip-Flop with TRI-STATE® Outputs

### General Description

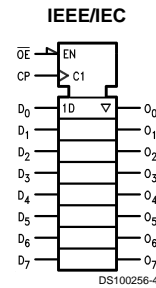
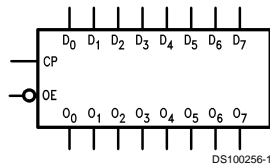
The 'AC/'ACT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ( $\overline{OE}$ ). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'AC/'ACT574 is functionally identical to the 'AC/'ACT374 except for the pinouts.

### Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'AC/'ACT374
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT574 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)  
— 'ACT574: 5962-89601

### Logic Symbols

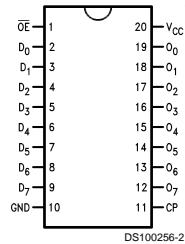


Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Outputs

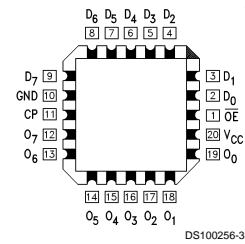
TRI-STATE® is a registered trademark of National Semiconductor Corporation.  
FACT™ is a trademark of Fairchild Semiconductor Corporation.

## Connection Diagrams

Pin Assignment for DIP, and Flatpak



Pin Assignment for LCC



## Functional Description

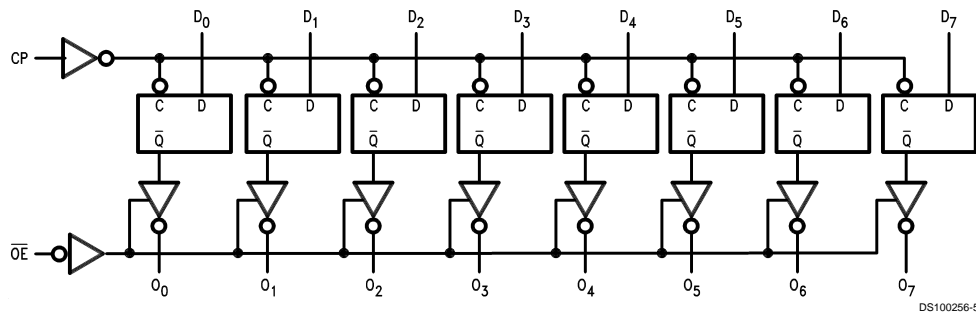
The 'AC/ACT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	$O_N$	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	N	L	L	Z	Load
H	N	H	H	Z	Load
L	N	L	L	L	Data Available
L	N	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 N = LOW-to-HIGH Transition  
 NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current Per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
CDIP	175°C

### Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	(Unless Otherwise Specified) (AC)	2.0V to 6.0V
	(ACT)	4.5V to 5.5V
Input Voltage ( $V_I$ )		0V to $V_{CC}$
Output Voltage ( $V_O$ )		0V to $V_{CC}$
Operating Temperature ( $T_A$ )	54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	'AC Devices	
	$V_{IN}$ from 30% to 70% of $V_{CC}$	
	$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	'ACT Devices	
	$V_{IN}$ from 0.8V to 2.0V	
	$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

### DC Characteristics for 'AC Family Devices

Symbol	Parameter	$V_{CC}$ (V)	54AC		Units	Conditions
			$T_A =$ -55°C to +125°C			
			Guaranteed Limits			
$V_{IH}$	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	3.15			
		5.5	3.85			
$V_{IL}$	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	1.35			
		5.5	1.65			
$V_{OH}$	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.4			
		5.5	5.4			
	(Note 2)		3.0	2.4	V	$V_{IN} = V_{IL}$ or $V_{IH}$ -12 mA
			4.5	3.7		
			5.5	4.7		
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.1			
		5.5	0.1			
	(Note 2)		3.0	0.50	V	$V_{IN} = V_{IL}$ or $V_{IH}$ 12 mA
			4.5	0.50		
			5.5	0.50		
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0	μA	$V_I = V_{CC}, GND$	
$I_{OZ}$	Maximum TRI-STATE Leakage Current	5.5	±5.0	μA	$V_I$ (OE) = $V_{IL}, V_{IH}$ $V_I = V_{CC}, V_{GND}$ $V_O = V_{CC}, GND$	

### DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	54AC	Units	Conditions
			T <sub>A</sub> = -55°C to +125°C		
			Guaranteed Limits		
I <sub>OLD</sub>	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	V <sub>OLD</sub> = 1.65V
I <sub>OHD</sub>		5.5	-50	mA	V <sub>OHD</sub> = 3.85V
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

### DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	54ACT	Units	Conditions
			T <sub>A</sub> = -55°C to +125°C		
			Guaranteed Limits		
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	2.0		
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	0.8		
V <sub>OH</sub>	Minimum High Level	4.5	4.4	V	I <sub>OUT</sub> = -50 μA
		5.5	5.4		
		4.5	3.70	V	(Note 4) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> -24 mA -24 mA
		5.5	4.70		
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.1	V	I <sub>OUT</sub> = 50 μA
		5.5	0.1		
		4.5	0.50	V	(Note 4) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> 24 mA 24 mA
		5.5	0.50		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	5.5	±5.0	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	1.6	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	(Note 5) Minimum Dynamic Output Current	5.5	50	mA	V <sub>OLD</sub> = 1.65V
I <sub>OHD</sub>		5.5	-50	mA	V <sub>OHD</sub> = 3.85V
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

**Note 4:** All outputs loaded; thresholds on input associated with output under test.

**Note 5:** Maximum test duration 2.0 ms, one output loaded at a time.

### AC Electrical Characteristics for 'AC Family Devices

Symbol	Parameter	V <sub>CC</sub> (V) (Note 6)	54AC		Units
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		
			Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	3.3 5.0	55 85		MHz
t <sub>PLH</sub>	Propagation Delay CP to O <sub>n</sub>	3.3 5.0	1.0 1.5	16.5 11.5	ns
t <sub>PHL</sub>	Propagation Delay CP to O <sub>n</sub>	3.3 5.0	1.0 1.5	15.0 10.5	ns
t <sub>PZH</sub>	Output Enable Time	3.3 5.0	1.0 1.5	13.0 9.5	ns
t <sub>PZL</sub>	Output Enable Time	3.3 5.0	1.0 1.5	12.5 9.5	ns
t <sub>PHZ</sub>	Output Disable Time	3.3 5.0	1.0 1.5	14.0 11.5	ns
t <sub>PLZ</sub>	Output Disable Time	3.3 5.0	1.0 1.5	10.5 9.0	ns

**Note 6:** Voltage Range 3.3 is 3.3V ± 0.3V  
Voltage Range 5.0 is 5.0V ± 0.5V

### AC Operating Requirements for 'AC Family Devices

Symbol	Parameter	V <sub>CC</sub> (V) (Note 7)	54AC		Units
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		
			Guaranteed Minimum		
t <sub>s</sub>	Set-Up Time, HIGH or LOW D <sub>n</sub> to CP	3.3 5.0	4.5 3.5		ns
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	3.3 5.0	2.5 2.5		ns
t <sub>w</sub>	CP Pulse Width HIGH or LOW	3.3 5.0	7.5 5.0		ns

**Note 7:** Voltage Range 3.3 is 3.3V ± 0.3V  
Voltage Range 5.0 is 5.0V ± 0.5V

## AC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	54ACT		Units
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		
			Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	5.0	70		ns
t <sub>PLH</sub>	Propagation Delay CP to O <sub>n</sub>	5.0	1.5	13.5	ns
t <sub>PHL</sub>	Propagation Delay CP to O <sub>n</sub>	5.0	1.5	12.5	ns
t <sub>PZH</sub>	Output Enable Time	5.0	1.5	11.0	ns
t <sub>PZL</sub>	Output Enable Time	5.0	1.5	11.0	ns
t <sub>PHZ</sub>	Output Disable Time	5.0	1.5	12.0	ns
t <sub>PLZ</sub>	Output Disable Time	5.0	1.5	10.0	ns

Note 8: Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements for 'ACT Family Devices

Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	54ACT		Units
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		
			Guaranteed Minimum		
t <sub>s</sub>	Set-Up Time, HIGH or LOW D <sub>n</sub> to CP	5.0	3.5		ns
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	2.0		ns
t <sub>w</sub>	CP Pulse Width HIGH or LOW	5.0	5.0		ns

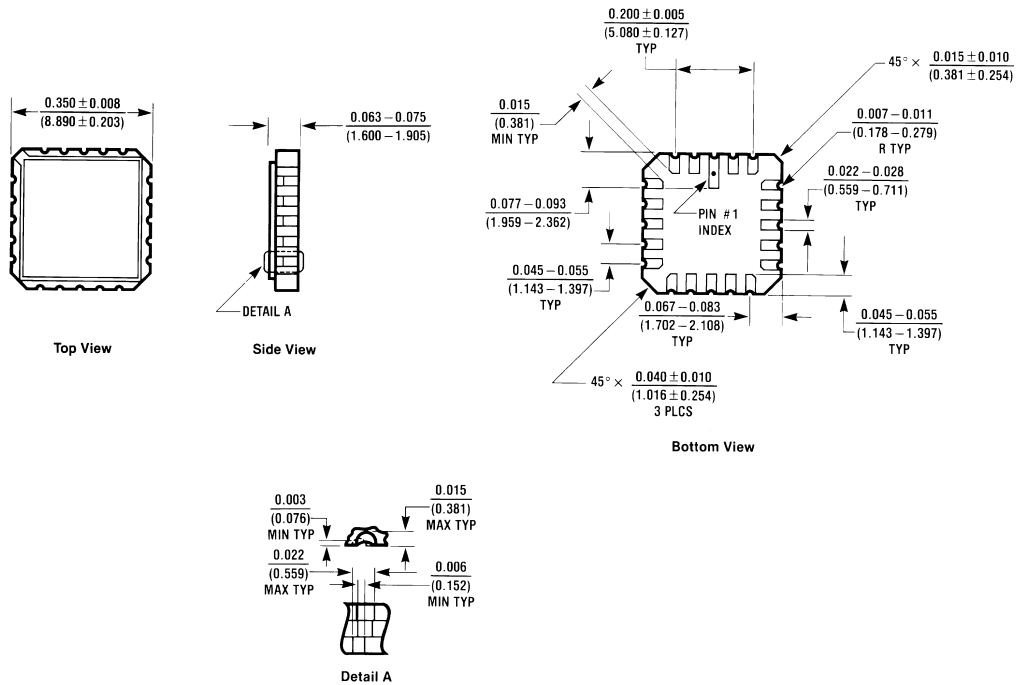
Note 9: Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	40.0	pF	V <sub>CC</sub> = 5.0V



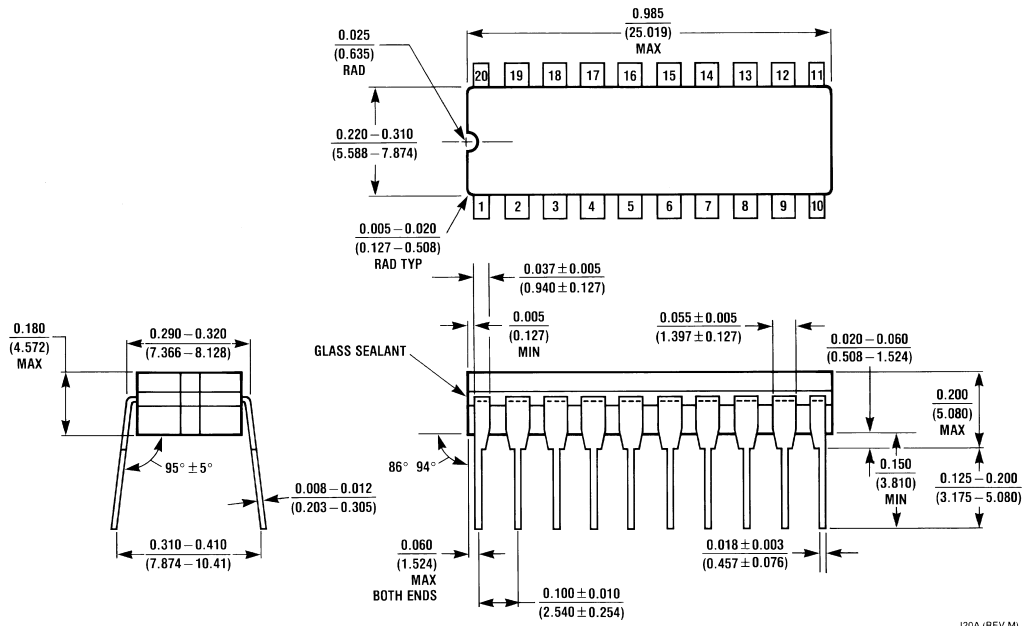
**Physical Dimensions** inches (millimeters) unless otherwise noted



E20A (REV D)

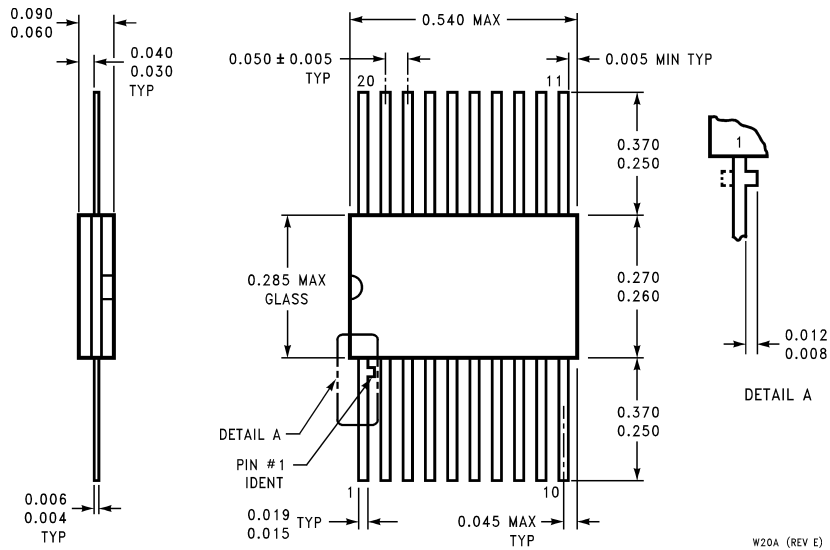
**20 Terminal Ceramic Leadless Chip Carrier (L)  
 NS Package Number E20A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



J20A (REV M)

**20 Lead Ceramic Dual-In-Line Package (D)**  
**NS Package Number J20A**



W20A (REV E)

**20 Lead Ceramic Flatpak (F)**  
**NS Package Number W20A**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com

[www.national.com](http://www.national.com)

**National Semiconductor Europe**  
Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 1 80-530 85 85  
English Tel: +49 (0) 1 80-532 78 32  
Français Tel: +49 (0) 1 80-532 93 58  
Italiano Tel: +49 (0) 1 80-534 16 80

**National Semiconductor Asia Pacific Customer Response Group**  
Tel: 65-2544466  
Fax: 65-2504466  
Email: sea.support@nsc.com

**National Semiconductor Japan Ltd.**  
Tel: 81-3-5620-6175  
Fax: 81-3-5620-6179

[Products](#) > [Military/Aerospace](#) > [Logic](#) > [FACT AC](#) > [54AC574](#)

# 54AC574 Product Folder

## Octal D Flip-Flop with TRI-STATE Outputs

[General Description](#)[Features](#)[Datasheet](#)[Package & Models](#)[Samples & Pricing](#)

### Datasheet

Title	Size in Kbytes	Date	<a href="#">View Online</a>	<a href="#">Download</a>	<a href="#">Receive via Email</a>
54AC574 54ACT574 Octal D-Type Flip-Flop with TRI-STATE Outputs	166 Kbytes	24-Sep-98	<a href="#">View Online</a>	<a href="#">Download</a>	<a href="#">Receive via Email</a>
54AC574 Mil-Aero Datasheet MN54AC574-X	17 Kbytes		<a href="#">View Online</a>	<a href="#">Download</a>	<a href="#">Receive via Email</a>

If you have trouble printing or viewing PDF file(s), see [Printing Problems](#).

### Package Availability, Models, Samples & Pricing

Part Number	Package			Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size	<a href="#">Package Marking</a>
	Type	Pins	MSL		SPICE	IBIS		Qty	\$US each		
54AC574LMQB	<a href="#">LCC</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A	<a href="#">Buy Now</a>	50+	\$8.8000	rail of 50	[logo]cZcSc4cA54AC574LMQB/QcMSE
54AC574DMQB	<a href="#">CERDIP</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A	<a href="#">Buy Now</a>	50+	\$6.4000	rail of 20	[logo]cZcSc4cA54AC574DMQBQcM
54AC574FMQB	<a href="#">CERPACK</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A	<a href="#">Buy Now</a>	50+	\$8.8000	rail of 19	[logo]cZcSc4cA54AC574FMQB/QcM
54AC574WG-QML	Ceramic SOIC	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$9.0000	tray of 30	[logo]cZcSc4cA54AC574WG-QML 5962-9677301QZA
JM38510/75604B2	<a href="#">LCC</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$13.6000	rail of 50	[logo] JM38510/75604B2A 27014 QS cZcSc4cA5E
JM38510R75604B2	<a href="#">LCC</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$75.0000	rail of 50	[logo] JM38510R75604B2A 27014 QS cZcSc4cA5E

JM38510R75604BR	<a href="#">CERDIP</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$73.0000	rail of 20	[logo]cZcSc4cASE JM38510R75604 BRA 27014 QS
JM38510/75604BS	<a href="#">CERPACK</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$13.6000	rail of 19	[logo]cZcSc4cASE JM38510/75604BSA 27014 QS
JM38510R75604BS	<a href="#">CERPACK</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$75.0000	rail of 19	[logo]cZcSc4cASE JM38510R75604BSA 27014 QS
JM38510R75604S2	<a href="#">LCC</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$138.0000	rail of 50	[logo]cZcSc4cA 27014 QSE JM38510R75604S2A
JM38510R7560SRA	<a href="#">CERDIP</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$138.0000	rail of 20	[logo]cZcSc4cASE JM38510R75604SRA 27014 Q
RM54AC574SSA	<a href="#">CERPACK</a>	20	<a href="#">MSL</a>	Preliminary	N/A	N/A				rail of N/A	[logo]cZcSc4cASE RM54AC574 SSA cR WAFER #
JM38510R75604SS	<a href="#">CERPACK</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$138.0000	rail of 19	[logo]cZcSc4cASE 27014 Q JM38510R75604SSA

## General Description

The 'AC/'ACT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (OE#). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'AC/'ACT574 is functionally identical to the 'AC/'ACT374 except for the pinouts.

## Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'AC/'ACT374
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT574 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
  - 'ACT574: 5962-89601

[Information as of 5-Aug-2002]

[Search](#)

[Design](#)

[Purchasing](#)

[Quality](#)

[Company](#)

[Home](#)

[About Languages](#) . [Website Guide](#) . [About "Cookies"](#) . National is [QS 9000 Certified](#) . [Privacy/Security Statement](#) . [Contact Us](#) . [Site Terms & Conditions of Use](#) . Copyright 2002 © National Semiconductor Corporation . [My Preferences](#) .

[Feedback](#)