National Semiconductor

August 1998

54AC175 • 54ACT175
Quad D Flip-Flop

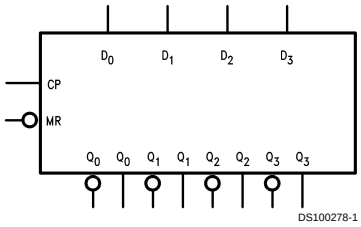
General Description

The 'AC/'ACT175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

Features

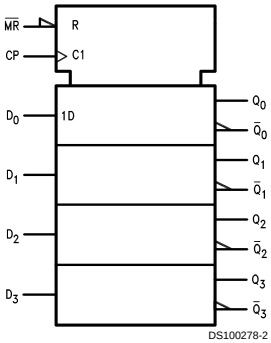
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output
- Outputs source/sink 24 mA
- 'ACT175 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
  - — 'AC175: 5962-89552
  - — 'ACT175: 5962-89693

Logic Symbols



DS100278-1

IEEE/IEC

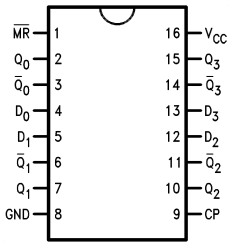


DS100278-2

Pin Names	Description
D_0–D_3	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_3	True Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complement Outputs

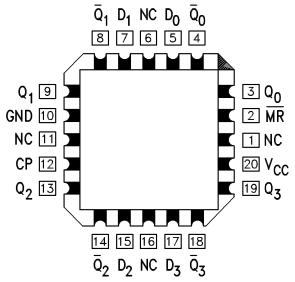
Connection Diagrams

Pin Assignment for DIP and Flatpak



DS100278-3

Pin Assignment for LCC



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Functional Description

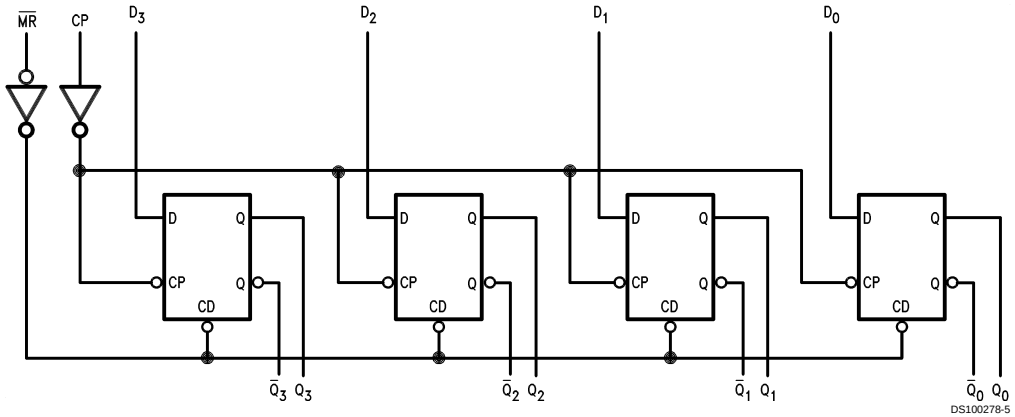
The 'AC/'ACT175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The 'AC/'ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

Inputs	Outputs	
@ t_n, $\overline{MR}$ = H	@ t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	−55˚C to +125˚C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	I_{OUT} = −50 μA
		4.5	4.4		
		5.5	5.4		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4	V	I_{OH} = −12 mA
		4.5	3.7		I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	I_{OUT} = 50 μA
		4.5	0.1		
		5.5	0.1		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50	V	I_{OL} = 12 mA
		4.5	0.50		I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V_I = V_{CC}, GND
	(Note 3)				
I_{OLD}	Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current	5.5	−50	mA	V_{OHD} = 3.85V Min

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ Guaranteed Limits	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	5.5	160.0	µA	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.4 5.4	V	I_{OUT} = −50 µA
					(Note 5) $V_{IN} = V_{IL}$ or V_{IH}
		4.5	3.70	V	I_{OH} = −24 mA
		5.5	4.70		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.1 0.1	V	I_{OUT} = 50 µA
					(Note 5) $V_{IN} = V_{IL}$ or V_{IH}
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	$V_I = V_{CC}$ − 2.1V
	(Note 6)				
I_{OLD}	Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current	5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	160.0	µA	$V_{IN} = V_{CC}$ or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

Note 7: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 8)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Clock Frequency	3.3	95		MHz	
		5.0	95			
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3	1.0	14.5	ns	
		5.0	1.5	10.5		
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3	1.0	15.0	ns	
		5.0	1.5	11.5		
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	3.3	1.0	15.0	ns	
		5.0	1.5	11.0		
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3	1.0	13.5	ns	
		5.0	1.5	10.5		

Note 8: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 9)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW D_n to CP	3.3	5.0	ns	
		5.0	3.5		
t_h	Hold Time, HIGH or LOW D_n to CP	3.3	2.0	ns	
		5.0	2.5		
t_w	CP Pulse Width HIGH or LOW	3.3	6.0	ns	
		5.0	5.0		
t_w	$\overline{MR}$ Pulse Width, LOW	3.3	5.5	ns	
		5.0	5.0		
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3	1.5	ns	
		5.0	1.5		

Note 9: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 10)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Clock Frequency	5.0	95		MHz	
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	5.0	1.5	11.5	ns	
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	5.0	1.5	12.5	ns	
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	5.0	1.5	11.5	ns	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.5	11.0	ns	

Note 10: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

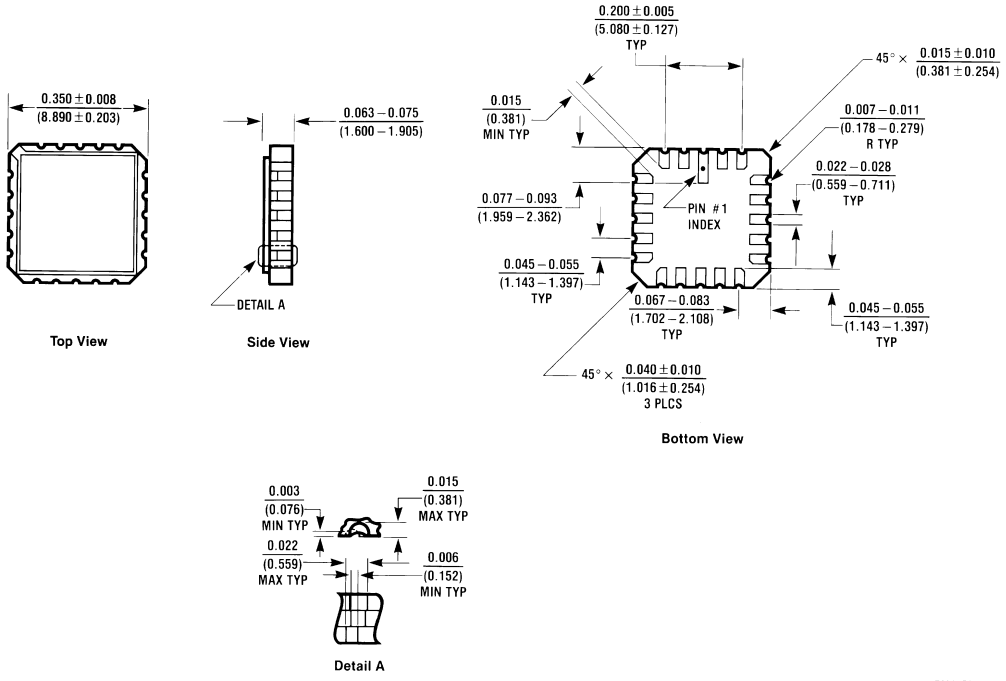
Symbol	Parameter	V_{CC} (V) (Note 11)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum		
t_s (H) t_s (L)	Setup Time D_n to CP	5.0	3.5 3.5	ns	
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.5	ns	
t_w	CP Pulse Width HIGH or LOW	5.0	5.0	ns	
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	5.0	ns	
t_{rec}	Recovery Time, $\overline{MR}$ to CP	5.0	1.5	ns	

Note 11: Voltage Range 5.0 is 5.0V ±0.5V

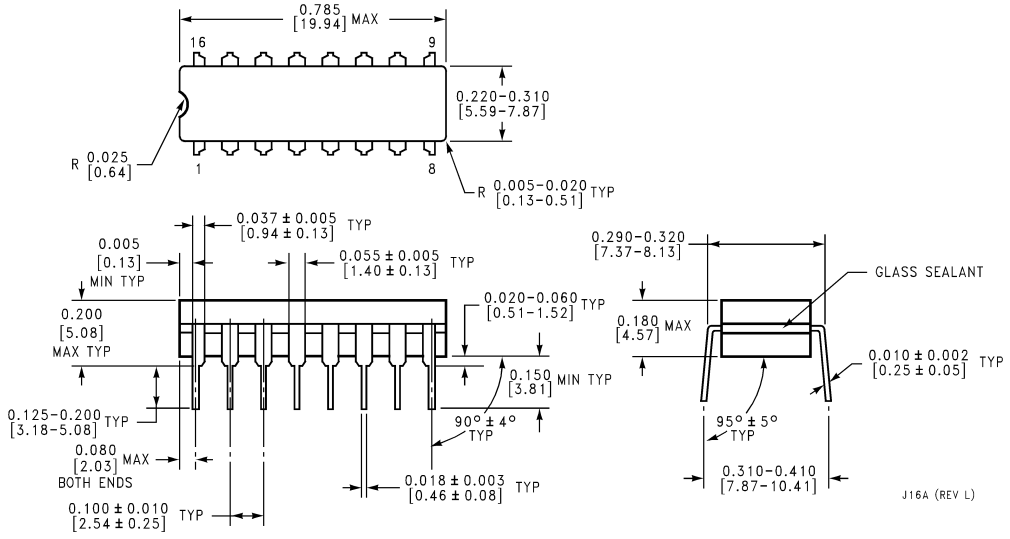
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	45.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

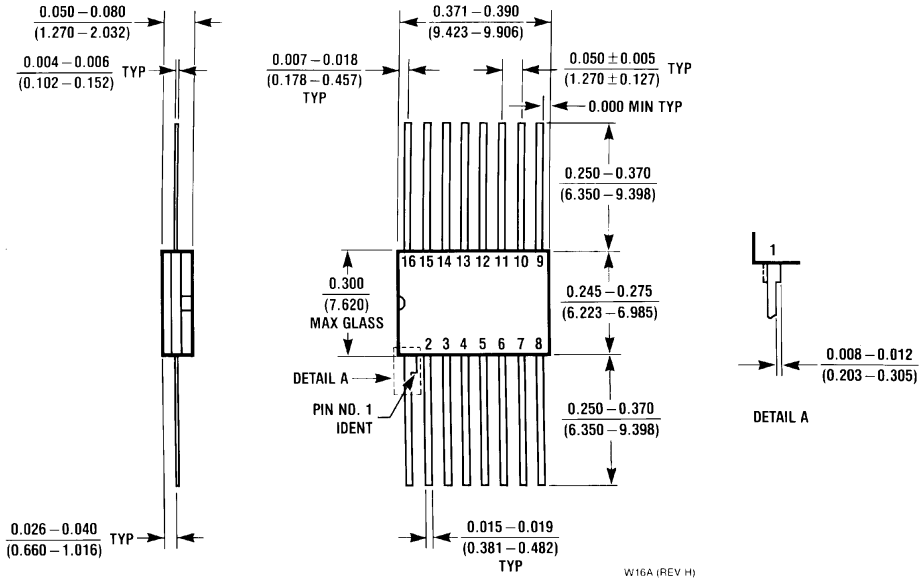


20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flatpak (F)
NS Package Number W16A

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54ACT175 Quad D Flip-Flop

Contents

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- 'ACT175 has TTL-compatible inputs

- Standard Microcircuit Drawing (SMD) -'AC175: 5962-89552 -'ACT175: 5962-89693

Datasheet

Title	Size (in Kbytes)	Date	View Online	Download	Receive via Email
54AC175 54ACT175 Quad D Flip-Flop	141 Kbytes	14-Aug-98	View Online	Download	Receive via Email

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Package Availability, Models, Samples & Pricing

Part Number	Package		Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size	Package Marking
	Type	# pins		SPICE	IBIS		Quantity	$US each		
5962-89693012A	LCC	20	Full production	N/A	N/A	.	50+	$8.0000	tube of 50	[logo]¢Z¢S¢4¢A 54ACT175 LMQB /Q¢M$E 5962-89693012A
5962R89693012A	LCC	20	Full production	N/A	N/A	.	50+	$82.0000	tube of 50	[logo]¢Z¢S¢4¢A 54ACT175 LMQB-RH R89693012A Q¢M$E
5962-8969301EA	Cerdip	16	Full production	N/A	N/A	.	50+	$6.0000	tube of 25	[logo]¢Z¢S¢4¢A$E 54ACT175DMQB /Q¢M 5962-8969301EA
5962R8969301EA	Cerdip	16	Full production	N/A	N/A	.	50+	$76.0000	tube of 25	[logo]¢Z¢S¢4¢A$E 54ACT175DMQB-RH Q¢M 5962R8969301EA

5962-8969301FA	Cerpack	16	Full production	N/A	N/A	.	50+	$7.0000	tube of 19	[logo]¢Z¢S¢4¢A$E 54ACT175FMQB Q¢M 5962-8969301FA
5962R8969301FA	Cerpack	16	Full production	N/A	N/A	.	50+	$76.0000	tube of 19	[logo]¢Z¢S¢4¢A$E 54ACT175FMQB -RH /Q¢M 5962 R8969301FA
5962R8969301V2A	LCC	20	Full production	N/A	N/A	.	50+	$138.0000	tube of 50	[logo]¢Z¢S¢4¢A 54ACT175E RQMLV $E 5962R 8969301V2A
5962R8969301VEA	Cerdip	16	Full production	N/A	N/A	.	50+	$138.0000	tube of 25	[logo]¢Z¢S¢4¢A$E 54ACT175JRQMLV 5962R8969301VEA
RM54ACT175VFA	Cerpack	16	Preliminary	N/A	N/A	.			tube of N/A	[logo]¢Z¢S¢4¢A$E RM54ACT175 VFA WAFER # ¢R
5962R8969301VFA	Cerpack	16	Full production	N/A	N/A	.	50+	$138.0000	tube of 19	[logo]¢Z¢S¢4¢A$E 54ACT175W RQMLV 5962 R8969301VFA
54ACT175DM-MLS	Cerdip	16	Lifetime buy	N/A	N/A	.	50+	$152.0000	tube of 25	[logo]¢Z¢S¢4¢A$E 54ACT175DM-MLS
54ACT175FM-MLS	Cerpack	16	Lifetime buy	N/A	N/A	.	50+	$152.0000	tube of 19	[logo]¢Z¢S¢4¢A$E 54ACT175FM -MLS

Application Notes

Title	Size (in Kbytes)	Date	View Online	Download	Receive via Email
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