

54ACTQ241

Quiet Series Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

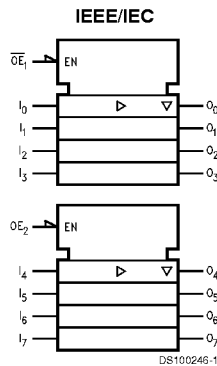
The ACTQ241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/ACT241
- 4 kV minimum ESD immunity ('ACTQ)
- Standard Microcircuit Drawing (SMD) 5962-92185

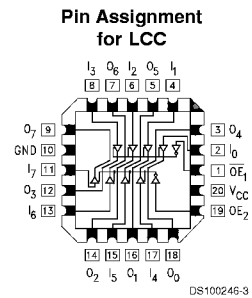
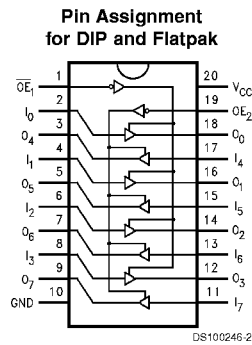
Features

- I_{CC} and I_{OZ} reduced by 50%

Logic Symbol



Connection Diagrams



Pin Names	Description
\overline{OE}_1, OE_2	TRI-STATE Output Enable Inputs
I_0-I_7	Inputs
O_0-O_7	Outputs

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 TRI-STATE® is a registered trademark of National Semiconductor Corporation.
 FACT® is a registered trademark of Fairchild Semiconductor Corporation.
 FACT Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
\overline{OE}_1	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
OE_2	I_n	
H	L	L
H	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C

DC Latch-Up Source or Sink Current	± 300 mA
Junction Temperature (T_J)	
CDIP	175°C

Recommended Operating Conditions

Supply Voltage (V_{CC}) 'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A) 54ACTQ	-55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$ 'ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

Note 2: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from -40°C to +125°C.

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	54ACTQ		Units	Conditions
			$T_A =$ -55°C to +125°C			
			Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5	2.0		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	2.0			
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	0.8			
V_{OH}	Minimum High Level Output Voltage	4.5	4.4		V	$I_{OUT} = -50 \mu A$
		5.5	5.4			
		4.5	3.70		V	(Note 3) $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA $I_{OH} = -24$ mA
		5.5	4.70			
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1		V	$I_{OUT} = 50 \mu A$
		5.5	0.1			
		4.5	0.50		V	(Note 3) $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24$ mA $I_{OL} = 24$ mA
		5.5	0.50			
I_{IN}	Maximum Input Leakage Current	5.5	± 1.0		μA	$V_I = V_{CC}, GND$
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5	± 5.0		μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$
I_{CCT}	Maximum I_{CC}/I_{IN}	5.5	1.6		mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	(Note 4) Minimum Dynamic Output Current	5.5	50		mA	$V_{OLD} = 1.65V$ Max
		5.5	-50		mA	$V_{OHD} = 3.85V$ Min

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	54ACTQ		Units	Conditions
			T _A = -55°C to +125°C			
			Guaranteed Limits			
I _{CC}	Maximum Quiescent Supply Current	5.5	80.0		μA	V _{IN} = V _{CC} or GND (Note 5)
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	1.5		V	(Notes 6, 7)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	-1.2		V	(Notes 6, 7)

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 6: Plastic DIP package.

Note 7: Max number of outputs defined as (n). Data Inputs are driven 0V to 3V. One output @ GND.

Note 8: Max number of Data Inputs (n) switching. n-1 Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 9)	54ACTQ		Units	Fig. No.
			T _A = -55°C to +125°C			
			C _L = 50 pF			
			Min	Max		
t _{PHL} , t _{PLH}	Propagation Delay Data to Output	5.0	1.5	8.0	ns	Figure 4
t _{PZL} , t _{PZH}	Output Enable Time	5.0	1.5	10.5	ns	Figure 5
t _{PHZ} , t _{PLZ}	Output Disable Time	5.0	1.5	9.5	ns	Figure 5

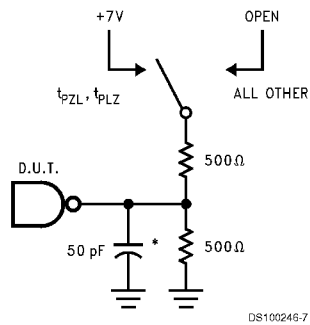
Note 9: Voltage Range 5.0 is 5.0V ±0.5V.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	70	pF	V _{CC} = 5.0V

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

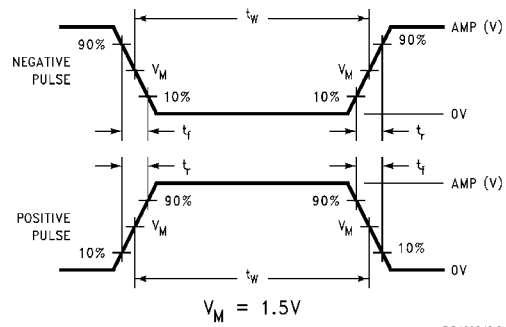


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

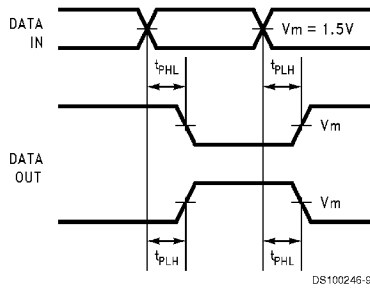


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

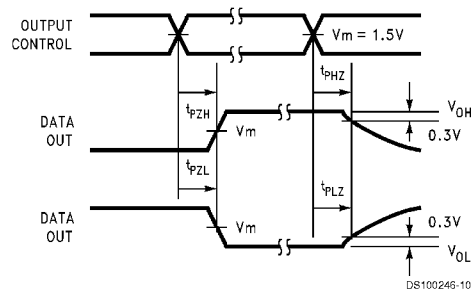
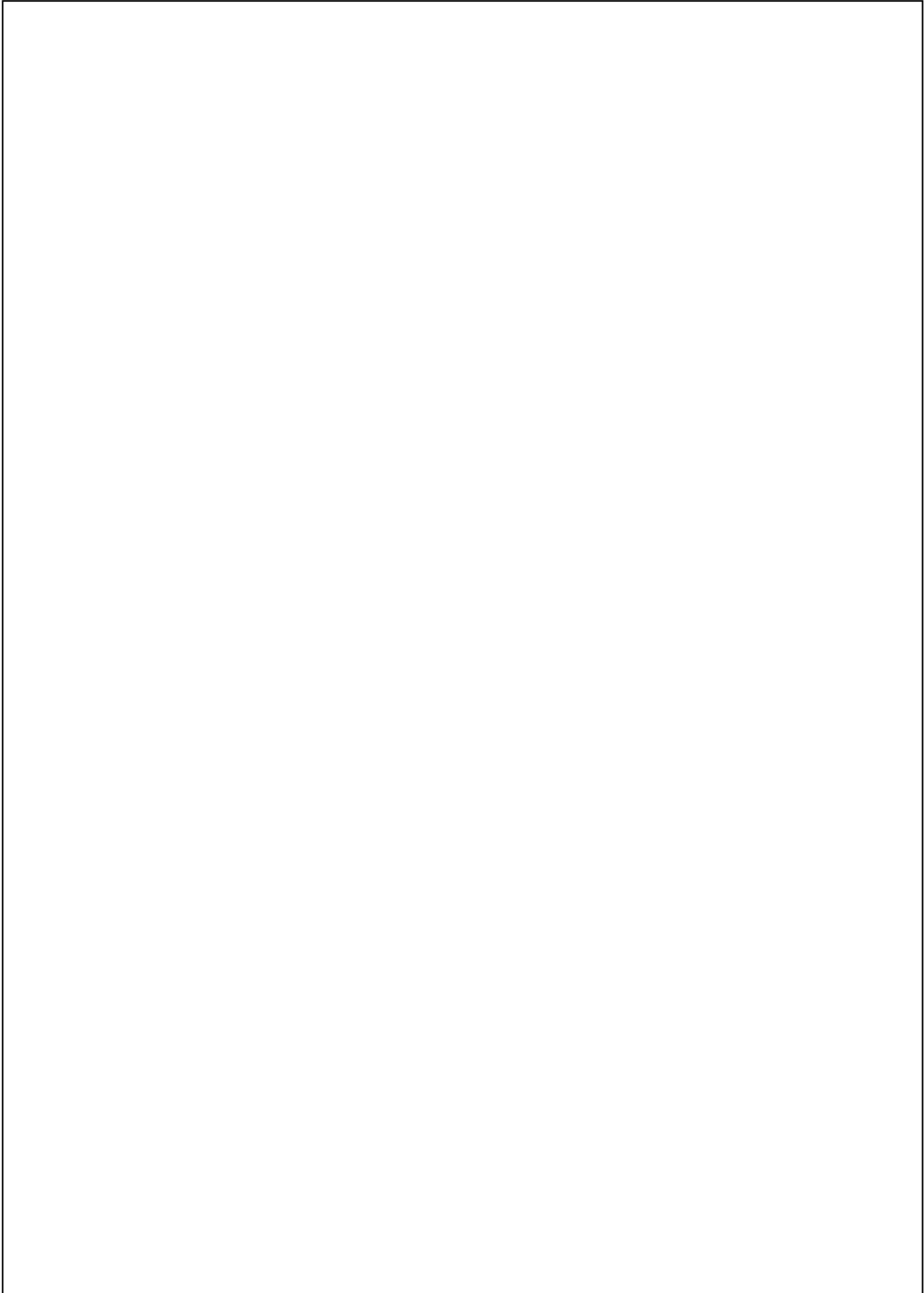
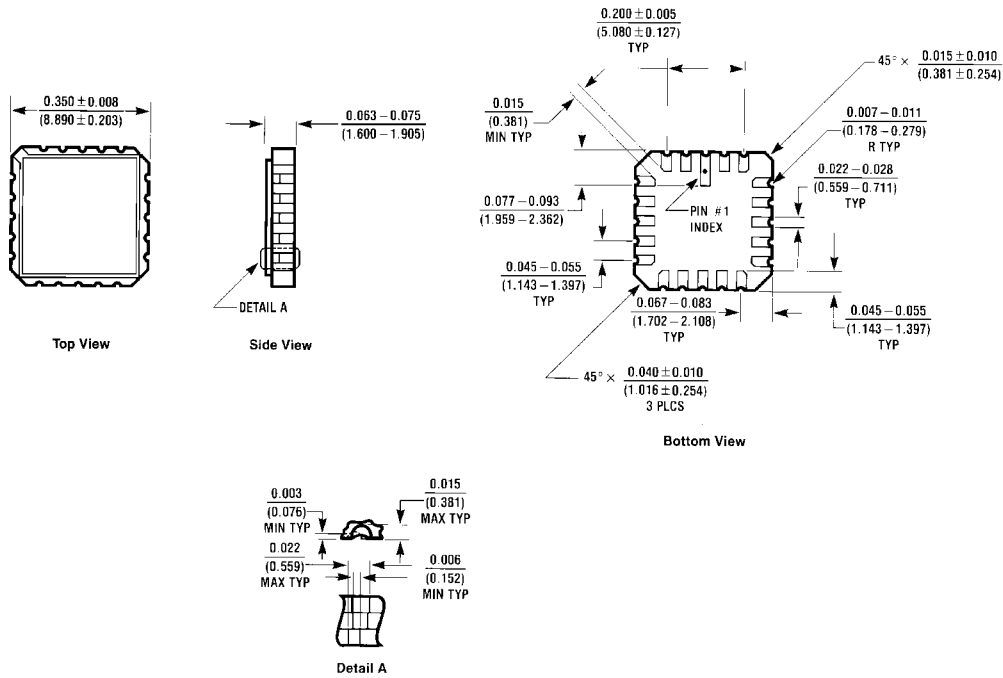


FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Time

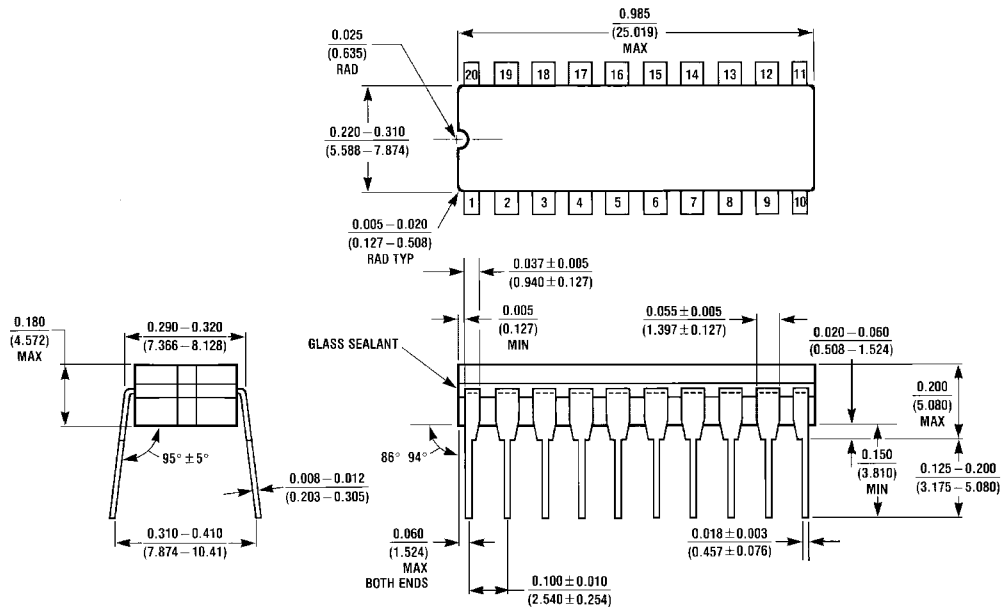


Physical Dimensions inches (millimeters) unless otherwise noted



E20A (REV D)

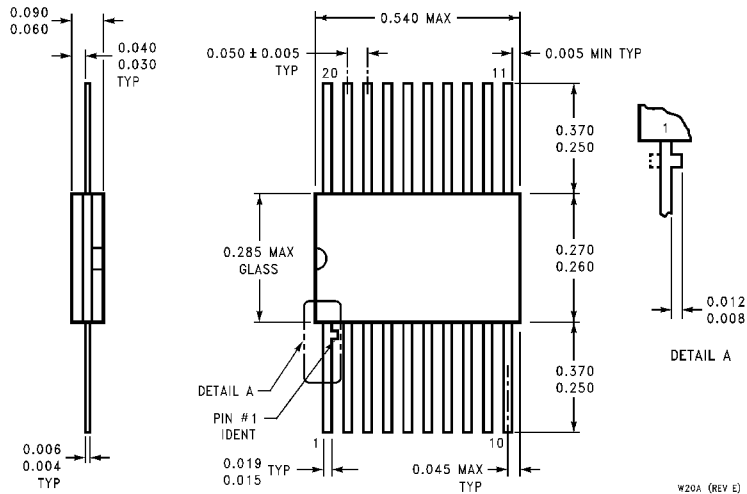
**20-Terminal Ceramic Leadless Chip Carrier (L)
 NS Package Number E20A**



J20A (REV M)

**20-Lead Ceramic Dual-In-Line Package (D)
 NS Package Number J20A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpak (F)
NS Package Number W20A**

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