NATIONAL SEMICOND {LOGIC} 02E D 6501122 0062715 8

54AC/74AC841 • 54ACT/74ACT841
54AC/74AC842 • 54ACT/74ACT842

T-46-07-12

10-Bit Transparent Latch

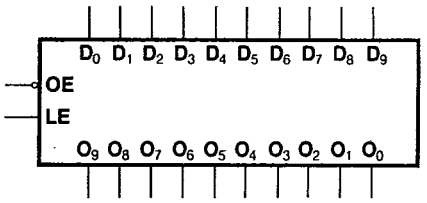
Description

The 'AC/'ACT841 and 'AC/'ACT842 bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'AC/'ACT841 is a 10-bit transparent latch, a 10-bit version of the 'AC/'ACT373.

- **'ACT841 and 'ACT842 have TTL-Compatible Inputs**

Ordering Code: See Section 6

Logic Symbol ('AC/'ACT841)*

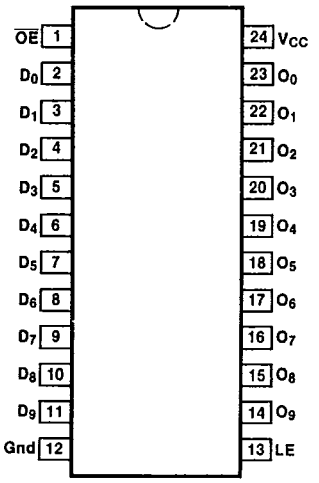


*The 'AC/'ACT842 has inverting outputs.

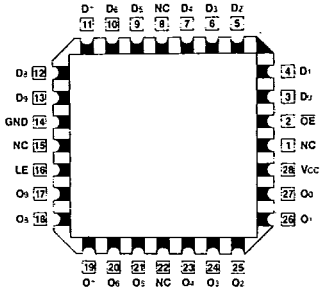
Pin Names

D_0 - D_9	Data Inputs
O_0 - O_9	Data Outputs ('AC/'ACT841)
$\overline{O}_0$ - $\overline{O}_9$	Data Outputs ('AC/'ACT842)
$\overline{OE}$	Output Enable
LE	Latch Enable

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

5

Functional Description

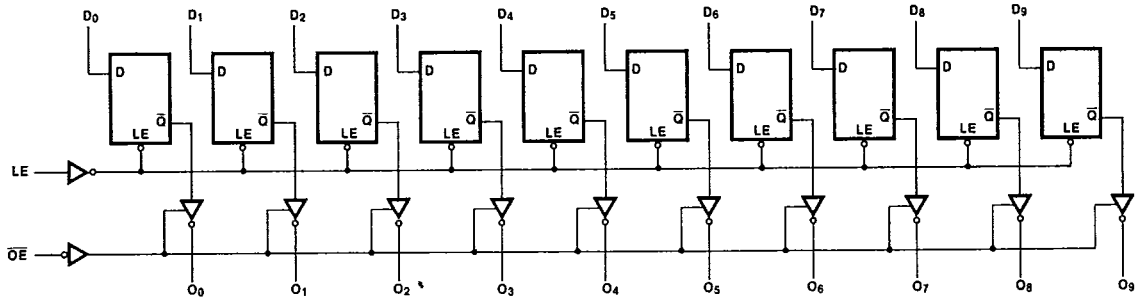
The 'AC/'ACT841 and 'AC/'ACT842 consist of ten D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable ($\overline{LE}$) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

Function Table

Inputs			Internal	Output		Function
$\overline{OE}$	LE	D	Q	O ('841)	$\overline{O}$ ('842)	
X	X	X	X	Z	Z	High Z
H	H	L	L	Z	Z	High Z
H	H	H	H	Z	Z	High Z
H	L	X	NC	Z	Z	Latched
L	H	L	L	L	H	Transparent
L	H	H	H	H	L	Transparent
L	L	X	NC	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram ('AC/'ACT841)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate progagation delays. The 'AC/'ACT842 has the same logic diagram with inverting outputs.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	V_{IN} = Vcc or Ground, Vcc = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	V_{IN} = Vcc or Ground, Vcc = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional Icc/Input ('ACT841/842)	1.6	1.5	mA	V_{IN} = Vcc − 2.1 V Vcc = 5.5 V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC T_A = +25°C C_L = 50 pF			54AC T_A = −55°C to +125°C C_L = 50 pF		74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3 5.0		17.0 12.0						ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	3.3 5.0		16.5 11.0						ns	3-5
t_{PLH}	Propagation Delay LE to O_n	3.3 5.0		18.5 13.0						ns	3-6
t_{PHL}	Propagation Delay LE to O_n	3.3 5.0		17.0 12.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		14.5 10.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		11.5 8.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		13.0 9.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		13.0 9.0						ns	3-8

5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

T-46-07-12

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF	54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	4.0 2.5			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	0 0			ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.5			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0		12.0						ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	5.0		11.0						ns	3-5
t_{PLH}	Propagation Delay LE to O_n	5.0		13.0						ns	3-6
t_{PHL}	Propagation Delay LE to O_n	5.0		12.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0		10.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0		8.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

T-46-07-12

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF	54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	2.5			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0			ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.5			ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

5

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V