National Semiconductor

June 1989

54AC/74AC845 • 54ACT/74ACT845
8-Bit Transparent Latch with TRI-STATE® Outputs

General Description

The 'AC/'ACT845 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide easy expansion through multiple $\overline{OE}$ controls.

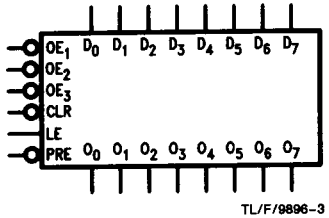
The 'AC/'ACT845 is functionally and pin compatible with AMD's Am29845.

The information for the 'AC845 is Advanced Information only.

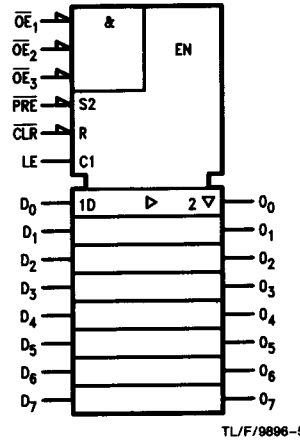
Features

- 'ACT845 has TTL-compatible inputs

Logic Symbols



TL/F/9896–3

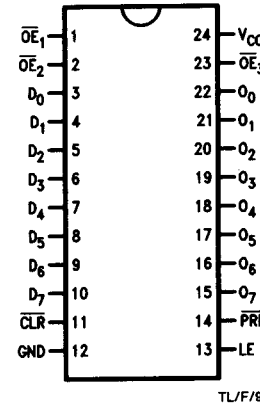


TL/F/9896–5

Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}_1$–$\overline{OE}_3$	Output Enables
LE	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset

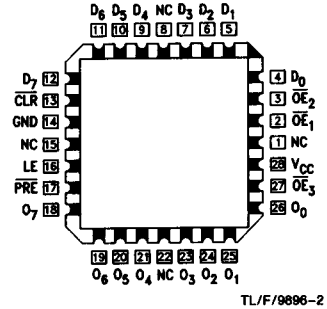
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9896–1

Pin Assignment for LCC



TL/F/9896–2

TRI-STATE® is a registered trademark of National Semiconductor Corporation
FACT™ is a trademark of National Semiconductor Corporation

Functional Description

The 'ACT845 consists of eight D latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition.

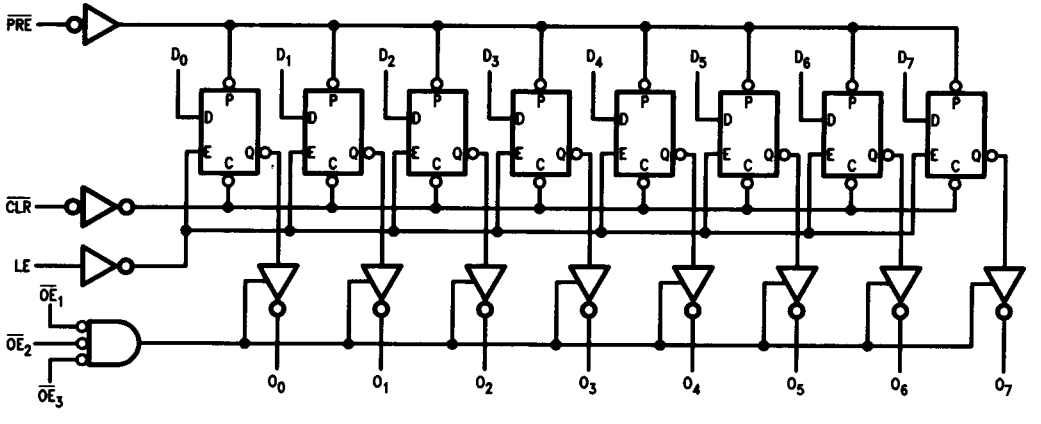
On the LE HIGH-to-LOW transition, the data that meets the setup times is latched Data appears on the bus when the Output Enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) are LOW. When any one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the bus output is in the high impedance state.

Function Table

Inputs					Internal	Output	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}_n$	LE	D	Q	O	
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Clear/High Z
H	L	H	L	X	H	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



TL/F/9696–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temerature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACT	−40°C to +85°C
54ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (Note 2) (Typical) (Except Schmitt Inputs) (t_r, t_f) V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: Individual data sheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	74ACT T_A = 25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units (V)	V_{CC}	Conditions
		Typ	Guaranteed Limits					
V_{IH}	Minimum High Level Input Voltage	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	4.5 5.5	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	4.5 5.5	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	4.5 5.5	I_{OUT} = −50 μA
			3.86 4.86	3.70 4.70	3.76 4.76	V	4.5 5.5	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	4.5 5.5	I_{OUT} = 50 μA
			0.36 0.36	0.50 0.50	0.44 0.44	V	4.5 5.5	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current		±0.1	±1.0	±1.0	μA	5.5	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current		±0.5	±10.0	±5.0	μA	5.5	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	0.6		1.6	1.5	mA	5.5	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current			50	75	mA	5.5	V_{OLD} = 1.65V Max
I_{OHD}				−50	−75	mA	5.5	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current		8.0	160	80	μA	5.5	V_{IN} = V_{CC} or Ground (Note 1)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	V_{CC}* (V)
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	2.0	5.5	9.5			2.0	10.0	ns	5.0
t_{PHL}	Propagation Delay D_n to O_n	2.0	5.5	9.5			2.0	10.0	ns	5.0
t_{PLH}	Propagation Delay LE to O_n	2.0	5.5	9.0			2.0	10.0	ns	5.0
t_{PHL}	Propagation Delay LE to O_n	2.0	5.5	9.0			2.0	10.0	ns	5.0
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	2.0	6.5	14.0			2.0	16.0	ns	5.0
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	2.0	7.5	15.5			2.0	17.5	ns	5.0
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	2.0	5.5	9.5			2.0	10.5	ns	5.0
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	2.0	5.5	9.5			2.0	10.5	ns	5.0
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	2.0	6.0	10.5			2.0	11.0	ns	5.0
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	2.0	6.0	10.5			2.0	11.0	ns	5.0
t_{PHL}	Propagation Delay $\overline{PRE}$ to O_n	2.0	6.0	10.5			2.0	11.0	ns	5.0
t_{PLH}	Propagation Delay $\overline{CLR}$ to O_n	2.0	5.5	9.5			2.0	10.5	ns	5.0

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	V_{CC}* (V)
		Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	−0.5	0.5		1.0	ns	5.0
t_h	Hold Time, HIGH or LOW D_n to LE	0.5	2.0		2.0	ns	5.0
t_w	LE Pulse Width, HIGH	2.0	3.5		3.5	ns	5.0
t_w	$\overline{PRE}$ Pulse Width, LOW	5.0	8.5		10.0	ns	5.0
t_w	$\overline{CLR}$ Pulse Width, LOW	5.5	9.5		11.0	ns	5.0
t_{rec}	$\overline{PRE}$ Recovery Time	0.5	2.0		2.0	ns	5.0
t_{rec}	$\overline{CLR}$ Recovery Time	0	1.0		1.0	ns	5.0

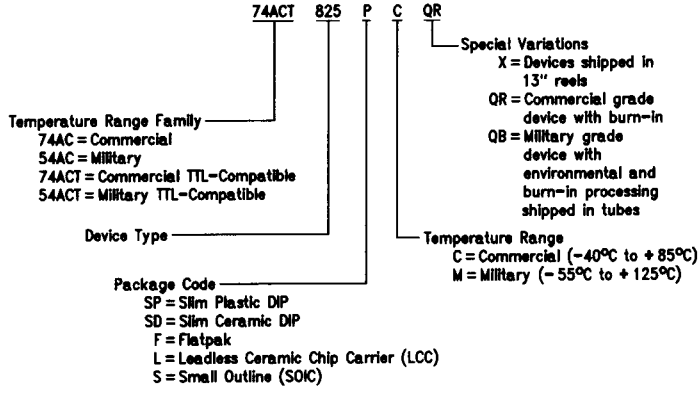
*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	54/74ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	44	pF	V_{CC} = 5.0V

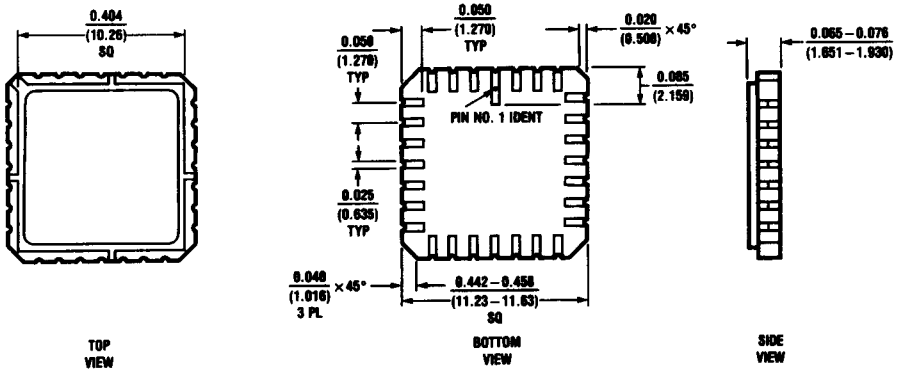
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



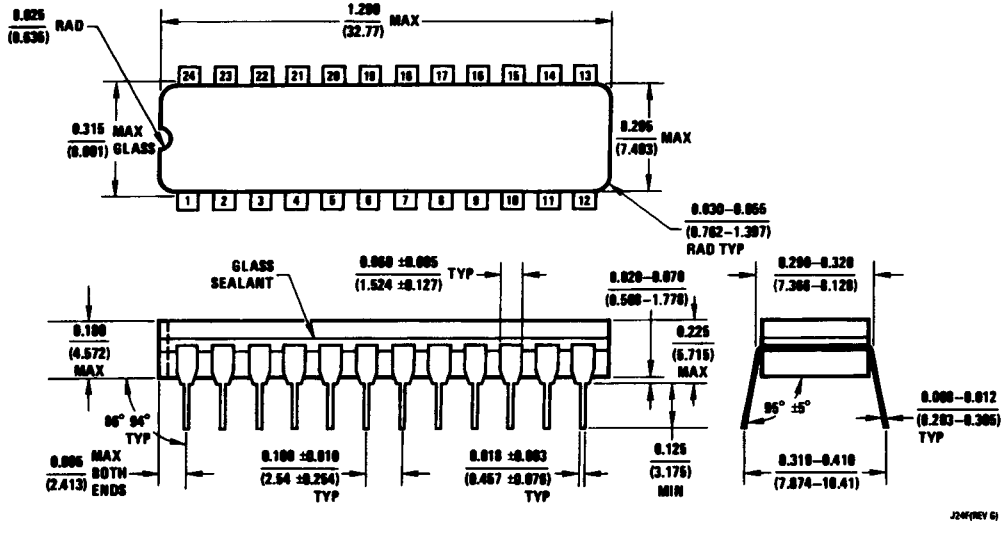
TL/F/9896–7

Physical Dimensions inches (millimeters)



E28A (REV C)

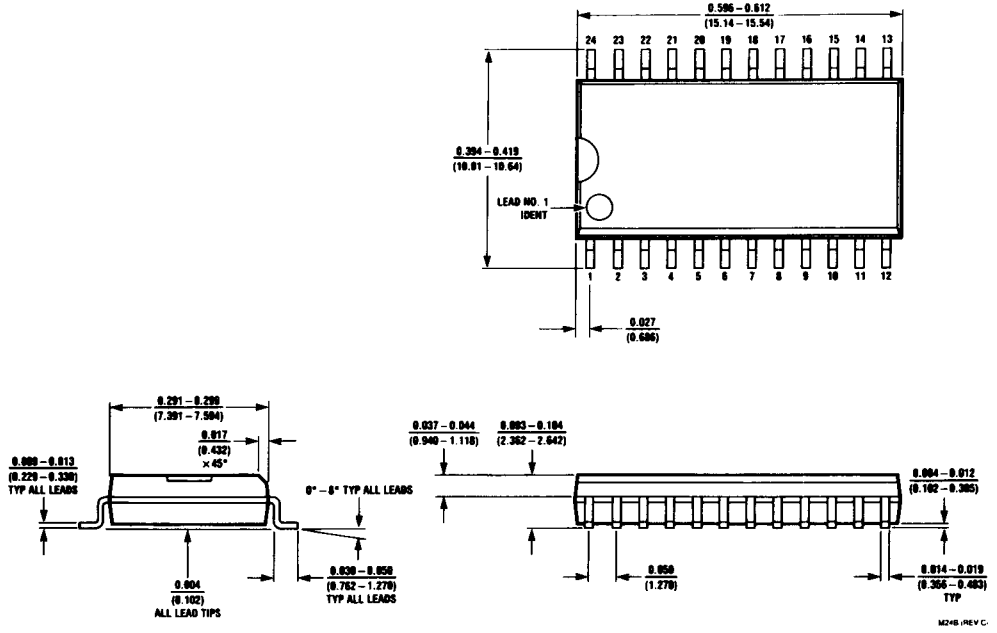
28 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E28A



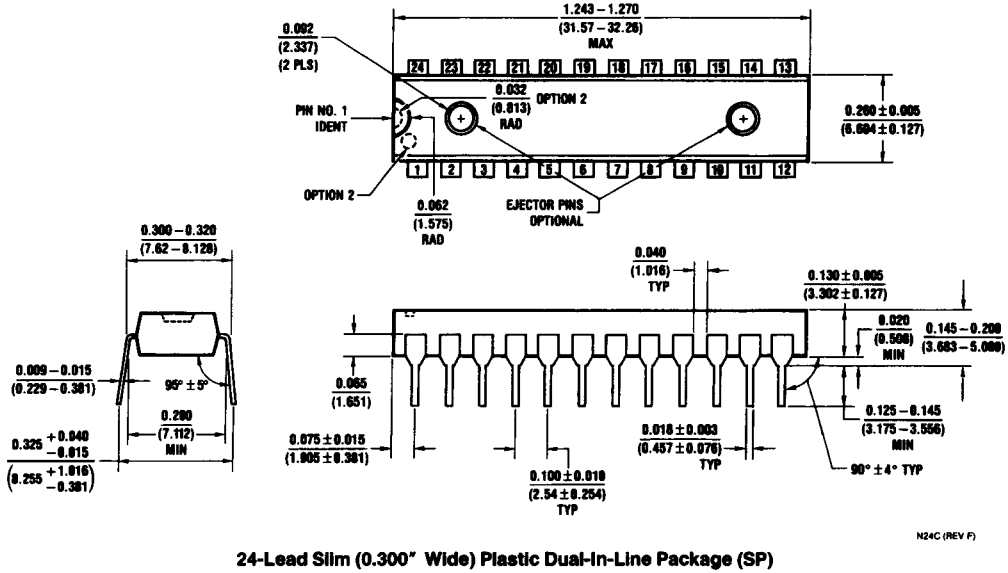
J24F(REV G)

24-Lead Slim (0.300″ Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F

Physical Dimensions inches (millimeters) (Continued)

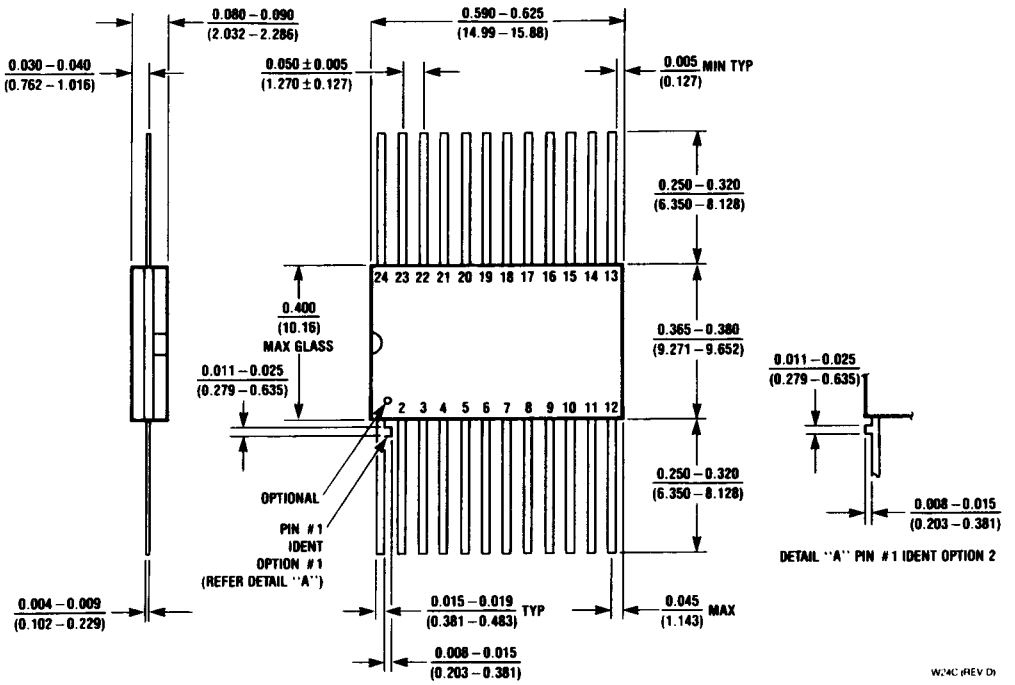


24-Lead Small Outline Integrated Circuit (S)
NS Package Number M24B



24-Lead Slim (0.300" Wide) Plastic Dual-In-Line Package (SP)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)



24-Lead Ceramic Flatpak (F)
NS Package Number W24C

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: (408) 721-5000
TWX: (910) 339-9240

National Semiconductor GmbH
Westendstrasse 193-195
D-8000 Munchen 21
West Germany
Tel: (089) 5 70 95 01
Telex: 522772

NS Japan Ltd.
Sanseido Bldg. 5F
4-15 Nishi Shinjuku
Shinjuku-Ku,
Tokyo 160, Japan
Tel: 3-299-7001
FAX: 3-299-7000

National Semiconductor Hong Kong Ltd.
Southeast Asia Marketing
Austin Tower, 4th Floor
22-26A Austin Avenue
Tsimshatsui, Kowloon, H.K.
Tel: 3-7231290, 3-7243645
Cable: NSSEAMKTG
Telex: 52996 NSSEA HX

National Semiconductores Do Brasil Ltda.
Av. Brig. Faria Lima, 830
8 Andar
01452 Sao Paulo, SP. Brasil
Tel: (55/11) 212-5066
Telex: 391-1131931 NSBR BR

National Semiconductor (Australia) PTY, Ltd.
21/3 High Street
Bayswater, Victoria 3153
Australia
Tel: (03) 729-6333
Telex: AA32096