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# 54F/74F164 Serial-In, Parallel-Out Shift Register

## General Description

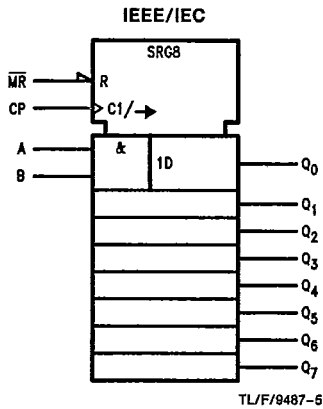
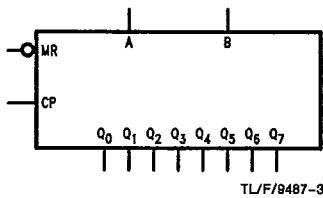
The 'F164 is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock.

## Features

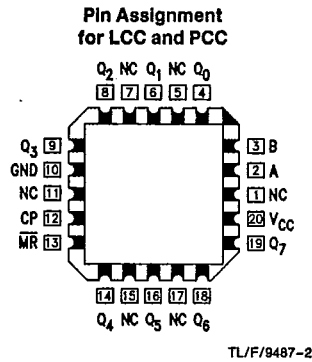
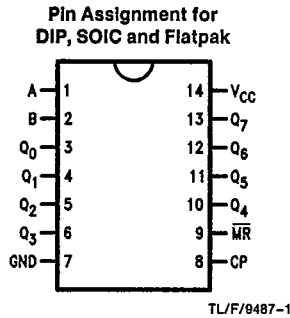
- Typical shift frequency of 90 MHz
- Asynchronous Master Reset
- Gated serial data input
- Fully synchronous data transfers

**Ordering Code:** See Section 5

## Logic Symbols



## Connection Diagrams



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A, B	Data Inputs	1.0/1.0	20 $\mu$ A / -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A / -0.6 mA
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A / -0.6 mA
$Q_0-Q_7$	Outputs	50/33.3	-1 mA / 20 mA

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### Functional Description

The 'F164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

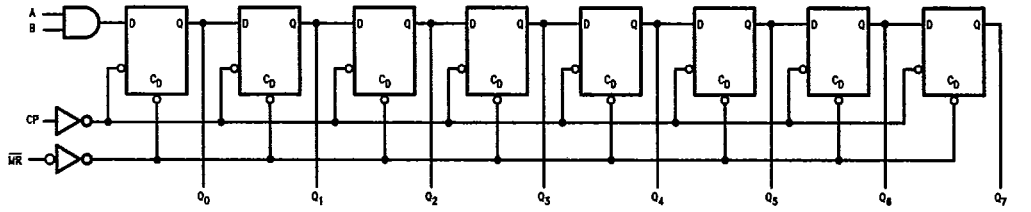
Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q<sub>0</sub> the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset ( $\overline{MR}$ ) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

Mode Select Table

Operating Mode	Inputs			Outputs	
	$\overline{MR}$	A	B	Q <sub>0</sub>	Q <sub>1</sub> -Q <sub>7</sub>
Reset (Clear)	L	X	X	L	L-L
Shift	H	l	l	L	q <sub>0</sub> -q <sub>8</sub>
	H	l	h	L	q <sub>0</sub> -q <sub>8</sub>
	H	h	l	L	q <sub>0</sub> -q <sub>8</sub>
	H	h	h	H	q <sub>0</sub> -q <sub>8</sub>

H(h) = HIGH Voltage Levels  
 L(l) = LOW Voltage Levels  
 X = Immaterial  
 q<sub>n</sub> = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			20	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CEX</sub>	Output HIGH Leakage Current			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>CC</sub>	Power Supply Current		35	55	mA	Max	CP = HIGH MR = GND, A, B = GND

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**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig No
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	80	90		50		80		MHz	2-1
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>	3.5	6.0	8.0	3.5	11.0	4.5	9.0	ns	2-3
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	5.5	10.5	13.0	5.5	16.0	5.5	14.0	ns	2-3

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig No
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max	Min	Max		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW A or B to CP	7.0		7.0		7.0		ns	2-6
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW A or B to CP	1.0		1.0		1.0			
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse Width HIGH or LOW	4.0		4.0		4.0			
t <sub>w</sub> (L)	MR Pulse Width, LOW	7.0		7.0		7.0		ns	2-4
t <sub>rec</sub>	Recovery Time MR to CP	7.0		7.0		7.0		ns	2-6

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