National Semiconductor

PRELIMINARY

# NMC6504 4096-Bit (4096 x 1) Static RAM

## General Description

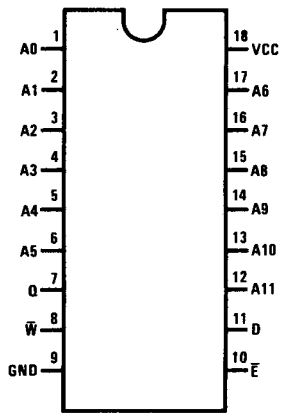
The NMC6504 is a static CMOS random access read/write memory organized as 4096 words of 1 bit each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible to the TTL environment. Synchronous operation is provided by on-chip address, data, and write latches. The ENABLE input serves as the device strobe controlling the latching functions. The TRI-STATE® output, in conjunction with the ENABLE input, allows easy memory expansion.

## Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- Common I/O — high density packaging
- Output data latches
- Input data latches
- Select latch for microprocessor interface

## Connection Diagram

**Dual-In-Line Package**

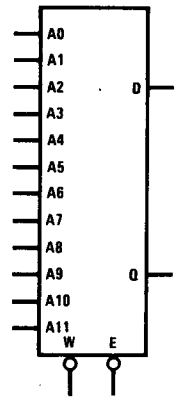



TOP VIEW

**Order Number NMC6504J-2, NMC6504J-9 or NMC6504J-5**
**See NS Package J18A**

**Order Number NMC6504N-5**
**See NS Package N18A**

## Logic Symbol




**Pin Names**

| | |
|---|---|
| A0–A11 | Address Inputs |
| Ē | Chip Enable |
| W̄ | Write Enable |
| D | Data Input |
| Q | Data Output |

4

## Functional Description

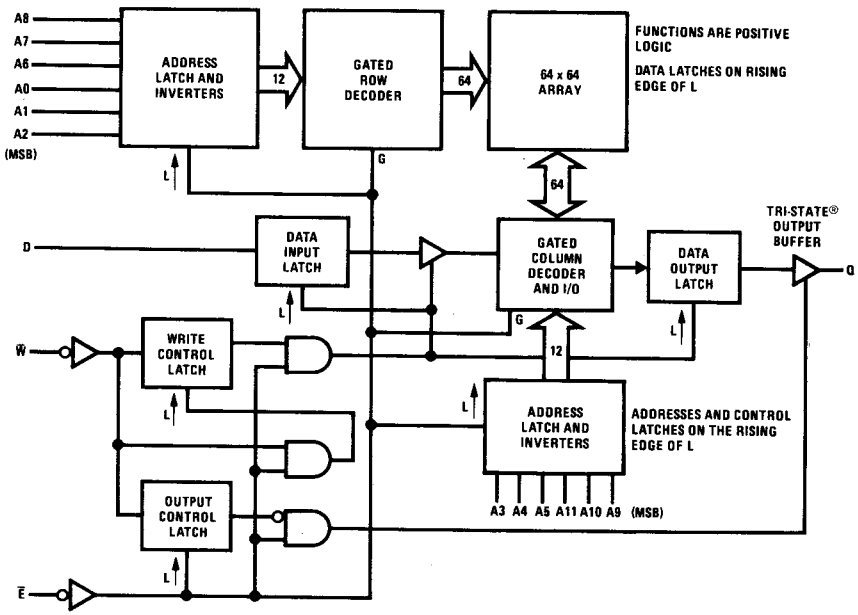
An NMC6504 memory cycle is initiated by the falling edge of the ENABLE ($\overline{E}$) input which latches the address information into the on-chip registers. On-chip latches allow selection of a read, early write, or read-modify-write cycle as a function of the ENABLE and WRITE ($\overline{W}$) input levels and timing. Data output is enabled by the falling edge of the ENABLE input and disabled by the rising edge except when performing an early write cycle. The input and output data latches are transparent except during the write pulse (not the WRITE input).

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the output. This minimum LOW time is defined as the enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next cycle.

An early write cycle is performed by preceding the ENABLE with the HIGH to LOW transition of the WRITE input. The WRITE input level is latched, and set-up and hold times must be met. The data output is not enabled during an early write cycle. The input data set-up and hold times are referenced to the leading edge of the write pulse, which is initiated by the falling edge of the ENABLE input and terminated by the rising edge of the ENABLE.

A read-modify-write cycle is performed as a read cycle, for the enable access time, followed by the write pulse which is initiated by the falling edge of the WRITE input and terminated by the rising edge of either the ENABLE or WRITE input, whichever occurs first. The input data set-up and hold times are referenced to the falling edge of the WRITE input. Data is latched when the WRITE input goes LOW, allowing the modified data to be written into the memory while continuing to read the original data.

## Block Diagram



## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage VCC | 7V |
| Voltage at Any Pin | −0.3V to VCC +0.3V |
| Storage Temperature Range | −65°C to +150°C |
| Package Dissipation | 500 mW |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

## Operating Range

| | Min | Max |
|---|---|---|
| Supply Voltage | | |
| NMC6504-9 | 4.5V | 5.5V |
| NMC6504-2 | 4.5V | 5.5V |
| NMC6504-5 | 4.75V | 5.25V |
| Temperature | | |
| NMC6504-9 | −40°C | 85°C |
| NMC6504-2 | −55°C | 125°C |
| NMC6504-5 | 0°C | 75°C |

## DC Electrical Characteristics over the operating range, unless otherwise noted

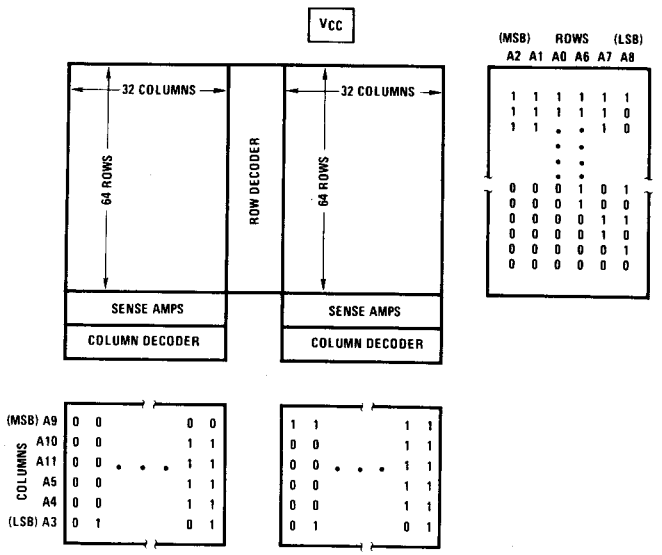
| Symbol | Parameter | Conditions | NMC6504-9, NMC6504-2 | | NMC6504-5 | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| VCCDR | Data Retention Supply Voltage | VI = VCC, GND | 2.0 | | 2.0 | | V |
| ICCSB | Standby Supply Current | | | 50 | | 500 | μA |
| ICCOP* | Operating Supply Current | f = 1 MHz, IO = 0, VI = VCC or GND | | 10 | | 10 | mA |
| ICCDR | Data Retention Supply Current | VCC = 3.0V, IO = 0, VI = VCC or GND | | 25 | | 500 | μA |
| II | Input Leakage Current | VI = VCC, GND | −1.0 | +1.0 | −10 | +10 | μA |
| VIL | Input Low Voltage | | −0.3 | 0.8 | −0.3 | 0.8 | V |
| VIH | Input High Voltage | | VCC − 2.0 | VCC + 0.3 | VCC − 2 | VCC + 0.3 | V |
| IOZ | Output Leakage Current | VI = VCC, GND | −1.0 | +1.0 | −10 | +10 | μA |
| VOL | Output Low Voltage | IOL = 2.0 mA | | 0.4 | | 0.45 | V |
| VOH | Output High Voltage | IOH = −1.0 mA | 2.4 | | 2.4 | | V |
| CI | Input Capacitance | f = 1 MHz | | 8 | | 8 | pF |
| CO | Output Capacitance | f = 1 MHz | | 10 | | 10 | pF |

* ICCOP is proportional to operating frequency.

## AC Test Conditions

Input Rise and Fall Times: ≤20 ns
All Timing Reference Levels: 1/2 VCC
Output Load: 1 TTL Load, 50 pF

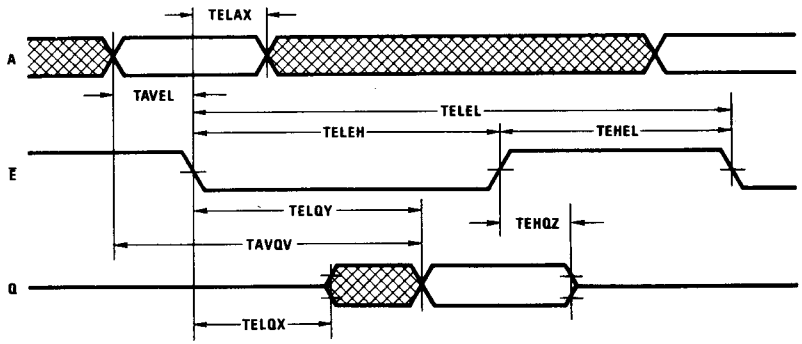
## NMC6504 Bit Map and Address Decoding



## Read Cycle AC Electrical Characteristics over the operating range

| Symbol | Parameter | NMC6504-9, NMC6504-2 | | NMC6504-5 | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| TAVEL | Address Set-up Time | 20 | | 20 | | ns |
| TELAX | Address Hold Time | 50 | | 50 | | ns |
| TELQV | Enable Access Time | | 300 | | 350 | ns |
| TAVQV | Address Access Time | | 320 | | 370 | ns |
| TELEH | Enable ($\bar{E}$) Minimum Low Time | 300 | | 350 | | ns |
| TELEL | Read or Write Cycle Time | 420 | | 500 | | ns |
| TEHEL | Enable ($\bar{E}$) Minimum High Time | 120 | | 150 | | ns |
| TELQX | Output Enable from Enable ($\bar{E}$) | | 100 | | 100 | ns |
| TEHQZ | Output Disable from Enable ($\bar{E}$) | | 100 | | 100 | ns |

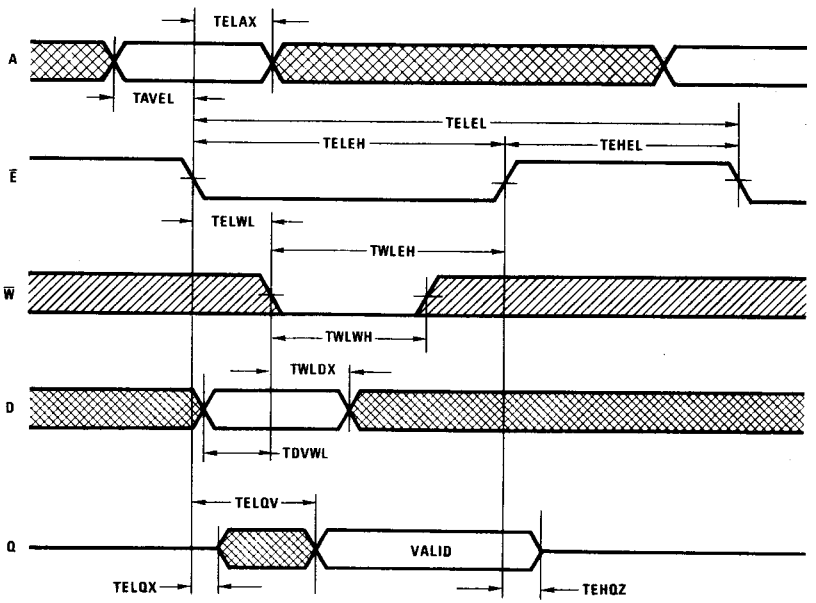
## Read Cycle Waveforms



## Write Cycle AC Electrical Characteristics over the operating range

| Symbol | Parameter | NMC6504-9, NMC6504-2 | | NMC6504-5 | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| TAVEL | Address Set-up Time | 20 | | 20 | | ns |
| TELAX | Address Hold Time | 50 | | 50 | | ns |
| TWLWH | Write Pulse Width ($\overline{W}$ Low) | 80 | | 100 | | ns |
| TELEL | Read or Write Cycle Time | 420 | | 500 | | ns |
| TELEH | Enable ($\overline{E}$) Minimum Low Time | 300 | | 350 | | ns |
| TDVWL | Data Set-up Time | 0 | | 30 | | ns |
| TEHEL | Enable ($\overline{E}$) Minimum High Time | 120 | | 150 | | ns |
| TWLDX | Data Hold Time | 80 | | 100 | | ns |
| TELWH | Write Pulse Width ($\overline{E}$ and $\overline{W}$ Low) | 80 | | 100 | | ns |
| TELWL | Early Write Output Hi-Z Time | 0 | | 0 | | ns |
| TWLEH | Write Pulse Width ($\overline{W}$ and $\overline{E}$ Low) | 200 | | 250 | | ns |
| TELQX | Output Enable from $\overline{E}$ | | 100 | | 100 | ns |
| TELQV | Enable Access Time | | 300 | | 350 | ns |
| TEHQZ | Output Disable from $\overline{E}$ | | 100 | | 100 | ns |

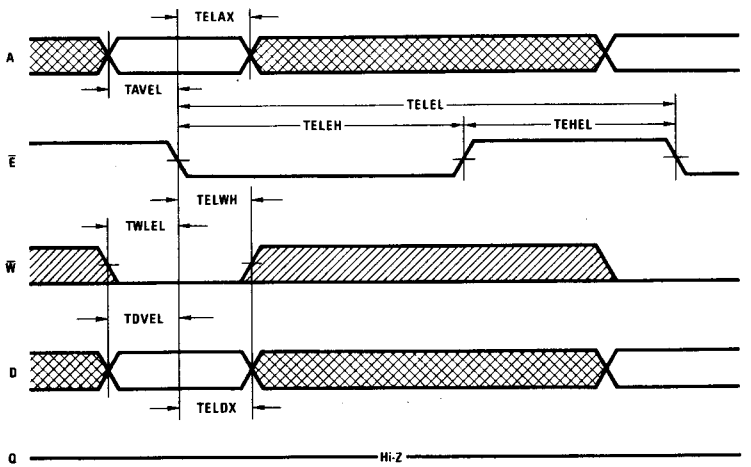
## Write Cycle Waveforms



## Early Write Cycle AC Electrical Characteristics over the operating range

| Symbol | Parameter | NMC6504-9, NMC6504-2 | | NMC6504-5 | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| TAVEL | Address Set-up Time | 20 | | 20 | | ns |
| TELAX | Address Hold Time | 50 | | 50 | | ns |
| TELWH | Write Pulse Width ($\bar{E}$ and $\bar{W}$ Low) | 80 | | 100 | | ns |
| TDVEL | Early Write Data Set-up Time | 0 | | 30 | | ns |
| TELEH | Enable ($\bar{E}$) Minimum Low Time | 300 | | 350 | | ns |
| TWLEL | Early Write Set-up Time | 0 | | 0 | | ns |
| TEHEL | Enable ($\bar{E}$) Minimum High Time | 120 | | 150 | | ns |
| TELDX | Early Write Data Hold Time | 80 | | 100 | | ns |
| TELEL | Read or Write Cycle Time | 420 | | 500 | | ns |

## Early Write Cycle Waveforms



## Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

| Symbol | Parameter | NMC6504-9, NMC6504-2 | | NMC6504-5 | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| TAVEL | Address Set-up Time | 20 | | 20 | | ns |
| TELAX | Address Hold Time | 50 | | 50 | | ns |
| TELQV | Enable Access Time | | 300 | | 350 | ns |
| TAVQV | Address Access Time | | 320 | | 370 | ns |
| TEHEL | Enable ($\bar{E}$) Minimum High Time | 120 | | 150 | | ns |
| TWHEL | $\overline{W}$ Read Mode Set-up Time | 0 | | 0 | | ns |
| TWLEH | Write Pulse Width ($\overline{W}$ and $\bar{E}$ Low) | 200 | | 250 | | ns |
| TQVWL | Data Valid to Write Time | 0 | | 0 | | ns |
| TWLWH | Write Pulse Width ($\overline{W}$ Low) | 80 | | 100 | | ns |
| TWLDX | Data Hold Time | 80 | | 100 | | ns |
| TELQX | Output Enable from Enable ($\bar{E}$) | | 100 | | 100 | ns |
| TEHQZ | Output Disable from Enable ($\bar{E}$) | | 100 | | 100 | ns |
| TDVWL | Data Set-up Time | 0 | | 30 | | ns |

## Read-Modify-Write Cycle Waveforms