National Semiconductor

MOS ROMs

MM52116 (2316E) 16,384-Bit Read Only Memory

General Description

The MM52116 is a static MOS 16,384-bit read-only memory organized in an 2048-word-by-8-bit format. It is fabricated using N-channel enhancement and depletion-mode technology which provides complete DTL/TTL compatibility and single power-supply operation.

Three programmable chip selects controlling the TRI-STATE® outputs allow for memory expansion.

Programming of the memory array and chip-select active levels is accomplished by changing two masks during fabrication.

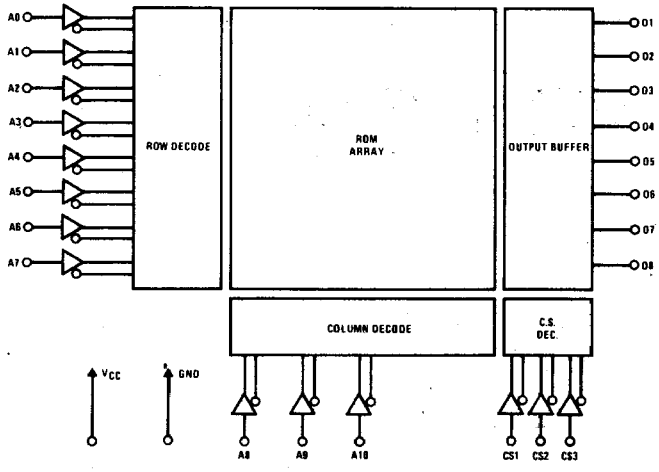
Features

- Fully decoded
- Single 5V power supply ±10% tolerance
- Inputs and outputs TTL compatible
- Outputs drive 2 TTL loads and 100 pF
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip selects
- 2048-word-by-8-bit organization
- Maximum access time – 450 ns
- Industry standard pin outs (2316E)
- Compatible to standard EPROMs

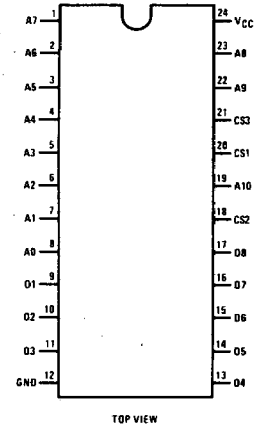
Applications

- Microprocessor instruction store
- Control logic
- Table look-up

Block and Connection Diagrams



Dual-In-Line Package



Order Number MM52116D
See NS Package D24C

Order Number MM52116N
See NS Package N24B

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +7.0V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Operating Temperature Range	0°C to 70°C

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified).

PARAMETER (Note 2)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
I_{LI}	Input Current	V_{IN} = 0 to V_{CC}			10	μA
V_{IH}	Logical "1" Input Voltage	0°C	2.0		V_{CC}+1.0	V
V_{IH}	Logical "1" Input Voltage	−40°C	2.2		V_{CC}+1.0	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.8	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 3.2 mA			0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 4V, Chip Deselected			10	μA
I_{LOL}	Output Leakage Current	V_{OUT} = 0.45V, Chip Deselected			−10	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, Data Output Open		70	100	mA

Capacitance

PARAMETER (Note 3)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified). See AC test circuit and switching time waveforms.

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
t_{AC}	Chip Select Access Time	See AC Test Circuit; t_{AC} and t_A Measured to Valid Output Levels with t_r and t_f of Input <20 ns, t_{OFF} Measured to <±20 μA Output Current			120	ns
t_{OFF}	Output Turn OFF Delay				100	ns
t_A	Address Access Time				450	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Positive true logic notation is used; logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

Switching Time Waveforms and AC Test Circuit

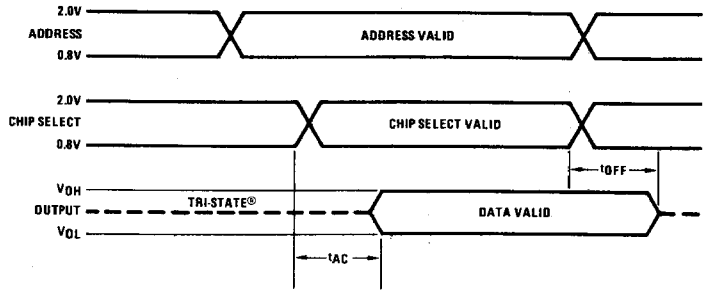


FIGURE 1. Address Precedes Chip Select

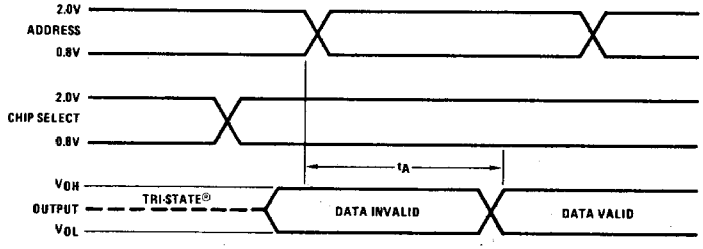
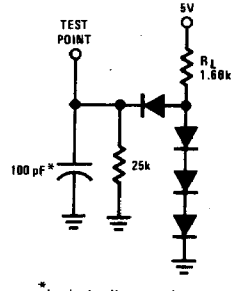


FIGURE 2. Address Follows Chip Select



*Includes jig capacitance

ROM Programming Information

ROM programs for the MM52116 can be supplied to National in a number of means:

A. 2708 PROM sets

B. 2516 PROM (or equivalent)

C. 2716 PROM (or equivalent)

D. Intellec HEX punched paper tape

E. Binary punched paper tape

Since the MM52116 has programmable chip selects, it is imperative that chip select information be provided along with the ROM program. The information should be supplied as shown:

CS1 is to be programmed logical_____(Hi or Lo)

CS2 is to be programmed logical_____(Hi or Lo)

CS3 is to be programmed logical_____(Hi or Lo)

Given any of the above means of program data is received by National, verification of ROM programs is handled internally via a sophisticated computerized system. The original input device (PROM, tape, etc.) is read, the data is reprocessed to formats required by various production machines, and the final reconstructed data is then compared back to the original input device.

The verification package returned to the customer for approval will consist of a listing of the program and a PROM or tape which matches the data National will use to create the programmed MM52116. In a normal situation, the verification package returned to the customer for approval, because of the system described, may consist of the original PROM or tape submitted by the customer. This program data, now in National's production format, is stored in archives for future customer re-orders.