

## DM10470/DM10470A 4096-Bit (4096 x 1) ECL RAMs

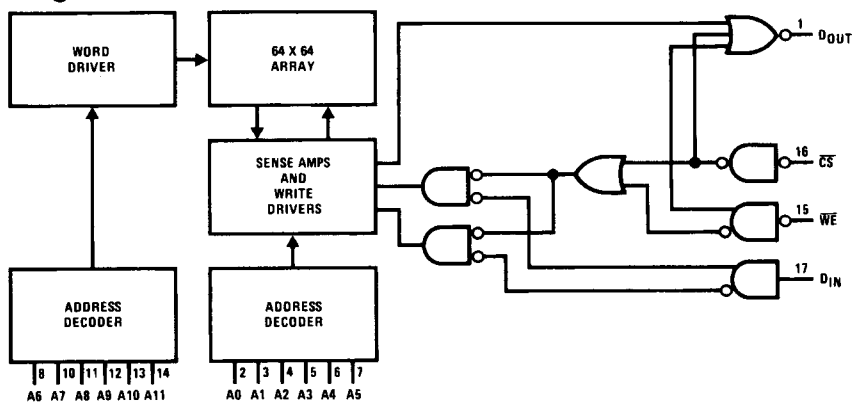
### General Description

The DM10470/DM10470A is a fully decoded 4096-bit, 10K and 10 KH compatible, ECL read/write random access memory designed for high-speed scratch pad and buffer storage applications. This device is organized as 4096 words by 1 bit and has separate Data In and Data Out pins. On-chip voltage compensation is provided for improved noise margin. The active low Chip Select and unterminated emitter-follower outputs allow for easy expansion.

### Features

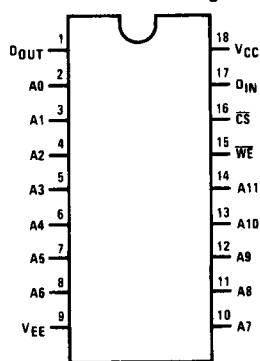
- Two speed selected offerings for maximum cost-performance:
  - DM10470 25 ns/200 mA max
  - DM10470A 15 ns/200 mA max
- 4096 x 1 bit organization
- 10K and 10 KH logic compatible
- On-chip voltage compensation for improved noise margin
- Oxide isolation process
- Unterminated emitter-follower outputs for easy memory expansion
- Compatible with HM10470, MBM10470 and F10470

### Logic Diagram



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### Connection Diagram

**Dual-In-Line Package**

**Top View**

TL/L/7723-2

Order Numbers DM10470J, DM10470AJ  
See NS Package Number J18A

### Truth Table

Inputs			Output	Mode
CS	WE	D <sub>IN</sub>	Open Emitter	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D <sub>OUT</sub>	Read

H = High Voltage Level

L = Low Voltage Level

X = Don't Care

### Pin Names

CS	Chip Select Input
A0-A11	Address Inputs
WE	Write Enable
D <sub>IN</sub>	Data Input
D <sub>OUT</sub>	Data Output

## Functional Description

Addressing the DM10470/DM10470A is achieved by means of the twelve address lines (A0–A11). Each of the  $2^{12}$  possible combinations of address inputs corresponds to a unique bit location in memory. The memory array can be expanded by wire-ORing the unterminated emitter-follower outputs of two or more devices and using the active-low Chip Select ( $\overline{CS}$ ) inputs as address lines.

The device is selected with  $\overline{CS}$  low and deselected with  $\overline{CS}$  high. A 50 $\Omega$  resistor to  $-2V$  (or an equivalent network) is required to provide a logic low at the output when the device is turned off. This termination is required for both single device and wire-ORed operation. The  $\overline{CS}$  input is internally pulled low so that in cases where no memory expansion is needed, no external connections are required.

The read and write operations are controlled by the state of the active-low Write Enable ( $\overline{WE}$ ). With  $\overline{WE}$  and  $\overline{CS}$  held low, the data at the Data Input ( $D_{IN}$ ) is written into the addressed location.  $\overline{WE}$  low also disables the output; the termination will then pull the output low. To read,  $\overline{WE}$  is held high while  $\overline{CS}$  is held low. The rising edge of  $\overline{WE}$  causes data at the addressed location to be transferred to the Data Output ( $D_{OUT}$ ). The Data presented at  $D_{OUT}$  is non-inverted.

## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias (Ambient)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
$V_{EE}$ Relative to $V_{CC}$	-7.0V to +0.5V
Any Input Relative to $V_{CC}$	$V_{EE}$ to +0.5V
Output Current (Output High)	-30 mA to +0.1 mA
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating is to be determined.	

## Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{EE}$ )	-5.46	-4.94	V
Ambient Temperature ( $T_A$ )	0	+75	°C

## DC Electrical Characteristics

$V_{EE} = -5.2V$ ,  $R_T = 50\Omega$  to  $-2.0V$ ,  $T_A = 0^\circ C$  to  $+75^\circ C$ , airflow exceeding 500 LFM

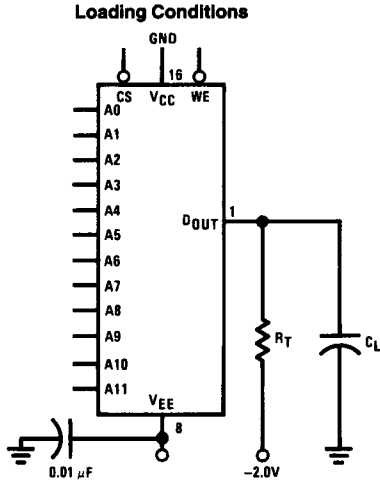
Symbol	Parameter	Conditions	$T_A$	Min	Max	Units
$V_{OH}$	Output Voltage High	$V_{IN} = V_{IH}$ Max or $V_{IL}$ Min	0°C 25°C 75°C	-1000 -960 -900	-840 -810 -720	mV
$V_{OL}$	Output Voltage Low	$V_{IN} = V_{IH}$ Max or $V_{IL}$ Min	0°C 25°C 75°C	-1870 -1850 -1830	-1665 -1650 -1625	mV
$V_{OHC}$	Output Voltage High	$V_{IN} = V_{IH}$ Min or $V_{IL}$ Max	0°C 25°C 75°C	-1020 -980 -920		mV
$V_{OLC}$	Output Voltage Low	$V_{IN} = V_{IH}$ Min or $V_{IL}$ Max	0°C 25°C 75°C		-1645 -1630 -1605	mV
$V_{IH}$	Input Voltage High	Guaranteed Input Voltage High for All Inputs	0°C 25°C 75°C	-1145 -1105 -1045	-840 -810 -720	mV
$V_{IL}$	Input Voltage Low	Guaranteed Input Voltage Low for All Inputs	0°C 25°C 75°C	-1870 -1850 -1830	-1490 -1475 -1450	mV
$I_{IH}$	Input Current High	$V_{IN} = V_{IH}$ Max	0°C to 75°C		220	$\mu A$
$I_{IL}$	Input Current Low, $\overline{CS}$ All Others	$V_{IN} = V_{IL}$ Min	0°C to 75°C	0.5 to -50	170	$\mu A$
$I_{EE}$	Power Supply Current Pin 9 (Note 1)	All Inputs & Outputs Open	0°C to 75°C	-200		mA

Note 1: Typical values at  $T_A = 0^\circ C$ ,  $I_{EE} = -160$  mA;  $T_A = 25^\circ C$ ,  $I_{EE} = 155$  mA,  $T_A = 75^\circ C$ ,  $I_{EE} = 140$  mA,  $V_{EE} = -5.2V$ , output load = 50 $\Omega$  and 30 pF to  $-2.0V$ .

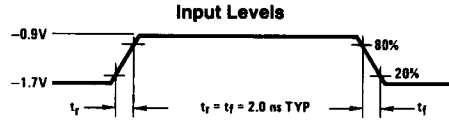
# AC Electrical Characteristics

$V_{EE} = -5.2V \pm 5\%$ ,  $R_T = 50\Omega$  to  $-2.0V$ ,  $C_L = 30\text{ pF}$ ,  $T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ , airflow exceeding 500 LFM

## Test Circuit and Input Waveform



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TL/L/7723-9

All timing measurements referenced from 50% of input levels to 50% of input/output levels

$C_L = 30\text{ pF}$  including jig and stray capacitance

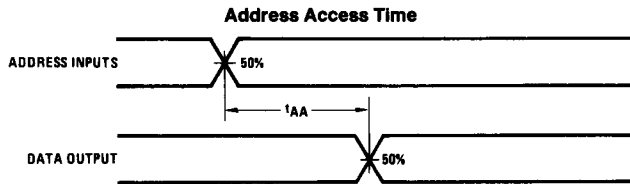
$R_T = 50\Omega$

## Read Cycle

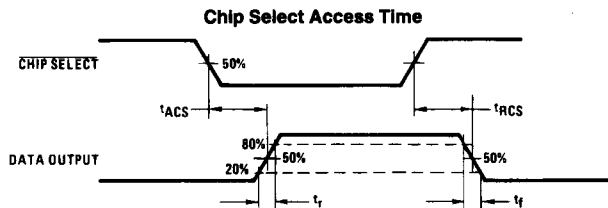
Symbol	Parameter	Conditions	DM10470		DM10470A		Units
			Min	Max	Min	Max	
$t_{AA}$	Address Access Time	Measured at 50% of Input to 50% of Output (Note 2)		25		15	ns
$t_{ACS}$	Chip Select Access Time			10		8	ns
$t_{RCS}$	Chip Select Recovery Time			10		8	ns

**Note 2:** The maximum address access time is guaranteed to be the worst-case bit in the memory using a pseudorandom testing pattern.

## Read Cycle Timing Diagrams



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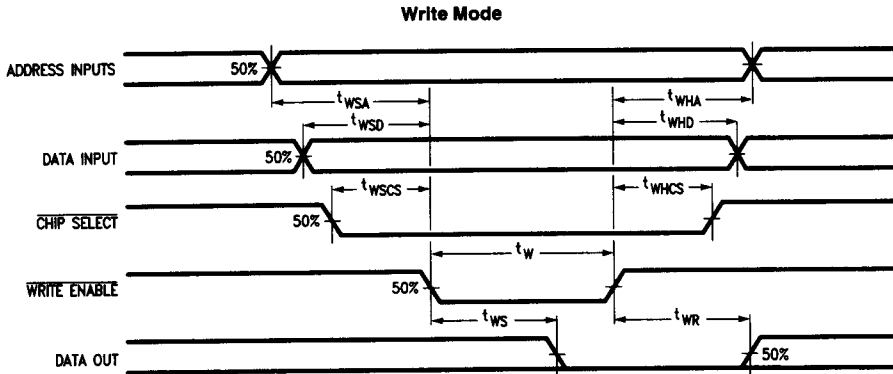


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## Write Cycle

Symbol	Parameter	DM10470		DM10470A		Units
		Min	Max	Min	Max	
$t_w$	Write Pulse Width (to Guarantee Writing)	15		10		ns
$t_{WSD}$	Data Set-Up Time Prior To Write	2		2		ns
$t_{WHD}$	Data Hold Time After Write	2		2		ns
$t_{WSA}$	Address Set-Up Time Prior to Write	3		3		ns
$t_{WHA}$	Address Hold Time After Write	2		2		ns
$t_{WSCS}$	Chip Select Set-Up Time Prior to Write	2		2		ns
$t_{WHCS}$	Chip Select Hold Time After Write	2		2		ns
$t_{WS}$	Write Disable Time		8		8	ns
$t_{WR}$	Write Recovery Time		8		8	ns

## Write Cycle Timing Diagram



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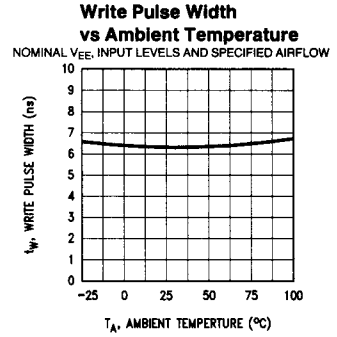
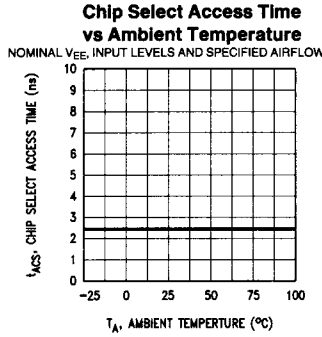
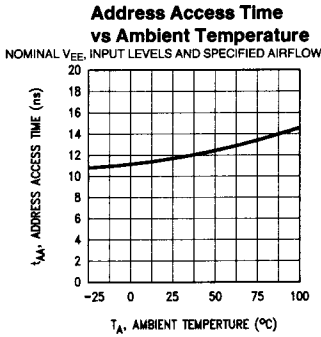
## Rise Time and Fall Time

Symbol	Parameter	Conditions	DM10470		DM10470A		Units
			Min	Max	Min	Max	
$t_r$	Output Rise Time	Measured Between 20% and 80% Points	1	3.5	1	3.5	ns
$t_f$	Output Fall Time		1	3.5	1	3.5	ns

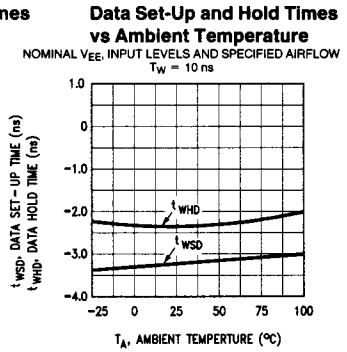
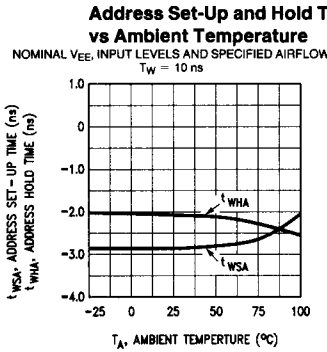
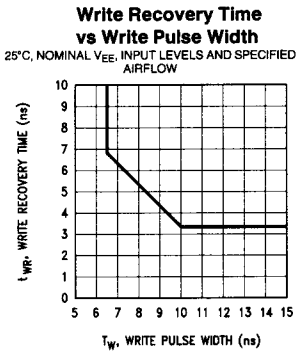
## Capacitance

Symbol	Parameter	Conditions	DM10470		DM10470A		Units
			Min	Max	Min	Max	
$C_{IN}$	Input Pin Capacitance	Measure With a Pulse Technique		5		5	pF
$C_{OUT}$	Output Pin Capacitance		8		8		pF

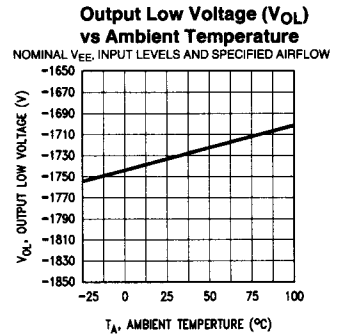
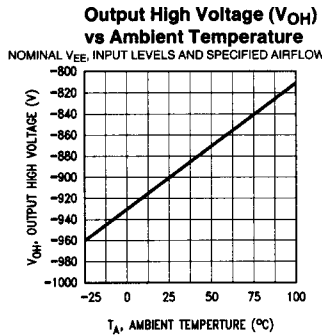
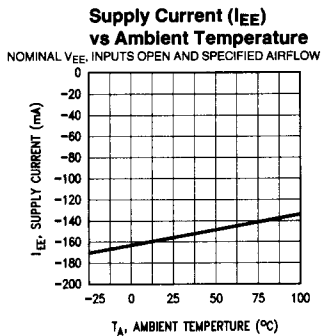
## Typical Performance Characteristics



TL/L/7723-10



TL/L/7723-11



TL/L/7723-12