

NDP7052 / NDB7052

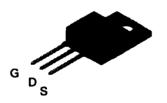
N-Channel Enhancement Mode Field Effect Transistor

General Description

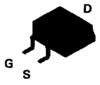
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

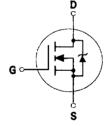
- 75A, 50V. $R_{DS(ON)} = 0.01\Omega$ @ $V_{GS}=10V$.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low R_{DS(ON)}.
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.



TO-220 NDP Series



TO-263AB NDB Series



Absolute Maximum Ratings T_c = 25°C unless otherwise noted

Symbol	Parameter	NDP7052	ND87052	Units
V _{DSS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \le 1 M\Omega$)	50		V
V _{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive (t _P < 50 μs)	± 40		
l _D	Drain Current - Continuous	75		Α
	- Pulsed	22		
P_{D}	Maximum Power Dissipation @T _C = 25°C	150		w
	Derate above 25°C	1		W/°C
T_J , T_{STG}	Operating and Storage Temperature Range	-65 to	175	୯
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	2	75	℃

Symbol	Parameter	Conditions		Min	Тур	Max	Units
DRAIN-S	OURCE AVALANCHE RATINGS (Note 1)						
W _{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25 \text{ V}, I_{D} = 75 \text{ A}$				550	mJ
AR	Maximum Drain-Source Avalanche	Current				75	A
OFF CHA	RACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	-	50			٧
l _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$				10	μΑ
I _{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$				100	пA
I _{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nΑ
ON CHAP	RACTERISTICS (Note 1)	•					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu\text{A}$		2		4	V
			T _J = 125℃	1.4		3.6	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V, } I_D = 37.5 \text{ A}$			0.008	0.01	Ω
			T _J = 150°C		0.014	0.018	
Dioni	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 10 \text{ V}$		60			Α
DRAIN-S	OURCE DIODE CHARACTERISTICS						
l _s	Maximum Continuos Drain-Source Diode Forward Current				75	Α	
l _{sm}	Maximum Pulsed Drain-Source Diode Forward Current				225	Α	
V _{SD}	Drain-Source Diode Forward	$V_{GS} = 0 \text{ V, } I_S = 37.5 \text{ A (Note 1)}$				1.3	V
	Voltage		T _J = 125°C			1.2	
THERMA	L CHARACTERISTICS						
R _{eJC}	Thermal Resistance, Junction-to-Case					1	•CW
R _{eja}	Thermal Resistance, Junction-to-Ambient					62.5	°C/W

Note:

^{1.} Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.