National Semiconductor™

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**ADVANCE INFORMATION**

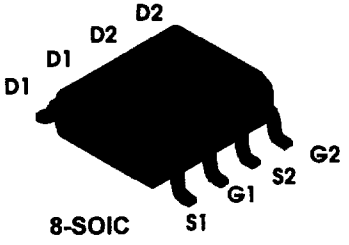
# NDS9925A
# Dual N-Channel Enhancement Mode Field Effect Transistor

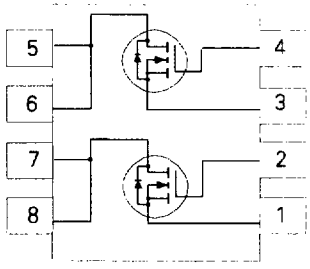
## General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

## Features

- 4.5A, 20V. $R_{DS(ON)}$ = 0.06Ω @ $V_{GS}$ = 4.5V
  $R_{DS(ON)}$ = 0.075Ω @ $V_{GS}$ = 2.7V.
- *High density cell design for extremely low* $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.




**Absolute Maximum Ratings** $T_A$ = 25°C unless otherwise not

| Symbol | Parameter | NDS9925A | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | 20 | V |
| $V_{GSS}$ | Gate-Source Voltage | 8 | V |
| $I_D$ | Drain Current - Continuous (Note 1a) | 4.5 | A |
| | - Pulsed | 15 | |
| $P_D$ | Power Dissipation for Dual Operation | 2 | W |
| | Power Dissipation for Single Operation (Note 1a) | 1.6 | |
| | (Note 1b) | 1 | |
| | (Note 1c) | 0.9 | |
| $T_J$,$T_{STG}$ | Operating and Storage Temperature Range | -55 to 150 | °C |
| **THERMAL CHARACTERISTICS** | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1a) | 78 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case (Note 1) | 40 | °C/W |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 20 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 16 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $T_J$ = 55°C | | | 10 | µA |
| $I_{GSSF}$ | Gate - Body Leakage, Forward | $V_{GS}$ = 8 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate - Body Leakage, Reverse | $V_{GS}$ = -8 V, $V_{DS}$ = 0 V | | | -100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 0.4 | | 1 | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 4.5 V, $I_D$ = 4.5 A | | | 0.06 | Ω |
| | | $V_{GS}$ = 2.7 V, $I_D$ = 1 A | | | 0.075 | |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS}$ = 4.5 V, $V_{DS}$ = 5 V | 15 | | | A |
| | | $V_{GS}$ = 2.7 V, $V_{DS}$ = 5 V | 5 | | | |
| **DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | | | 1.3 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.3 A (Note 2) | | | 1.2 | V |

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

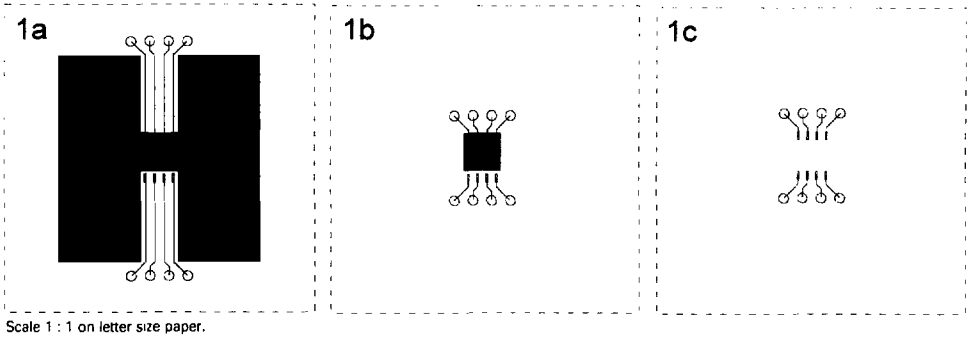
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.




Scale 1 : 1 on letter size paper.

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.