National Semiconductor™

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ADVANCE INFORMATION

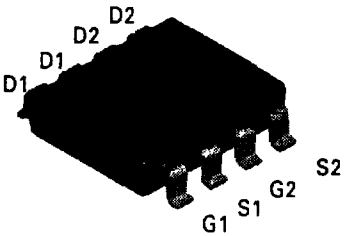
NDH8301N
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

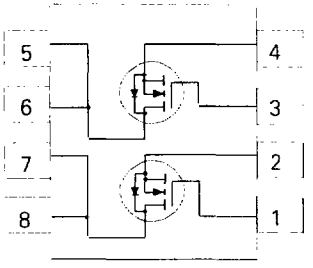
These N-Channel enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 3A, 30V. $R_{DS(ON)}$ = 0.06Ω @ V_{GS} = 4.5V
  $R_{DS(ON)}$ = 0.075Ω @ V_{GS} = 2.7V.
- Proprietary SuperSOT™-8 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-8



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	NDH8301N	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	8	V
I_D	Drain Current - Continuous (Note 1)	3	A
	- Pulsed	9	
P_D	Maximum Power Dissipation (Note 1)	0.9	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	135	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA		20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V				1	µA
			T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V				100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V				-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA		0.4		1	V
			T_J = 125°C	0.3		0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 3 A				0.06	Ω
			T_J = 125°C			0.11	
		V_{GS} = 2.7 V, I_D = 2.7 A				0.075	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V		9			A
		V_{GS} = 2.7 V, V_{DS} = 5 V		3			
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current					0.75	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.75 A (Note 2)				1.2	V

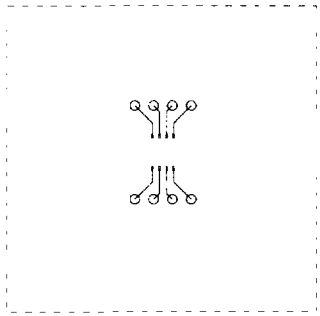
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

135°C/W when mounted on a 0.0025in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.