

CD4072BM/CD4072BC Dual 4-Input OR Gate, CD4082BM/CD4082BC Dual 4-Input AND Gate

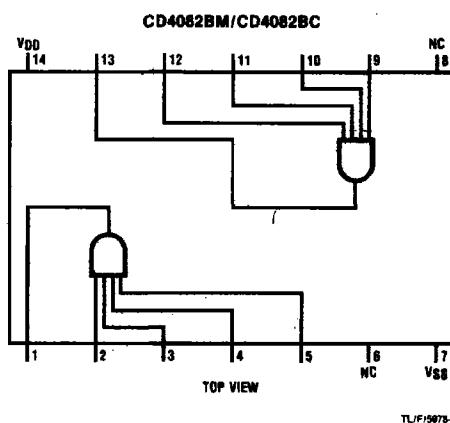
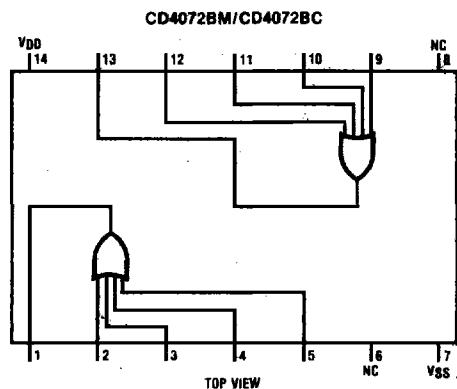
General Description

These dual gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45V_DD (typ.)
- Low power TTL fanout of 2 driving 74L
- compatibility or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μ A at 15V over full temperature range

Connection Diagram



Order Number CD4072BMJ, CD4072BCJ, CD4082BMJ
or CD4082BCJ
See NS Package J14A

Order Number CD4072BMN, CD4072BCN,
CD4082BMN or CD4082BCN
See NS Package N14A

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD} Supply Voltage	-0.5 to +18 V
V_{IN} Input Voltage	-0.5 to V_{DD} 0.5 V
T_S Storage Temperature Range	-65°C to +150°C
P_D Package Dissipation	500mW
T_L Lead Temperature (soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3.0 to 15 V
V_{IN} Input Voltage	0 V to V_{DD} V
T_A Operating Temperature Range	-55°C to +125°C
CD4072BM, CD4082BM	-40°C to +85°C
CD4072BC, CD4082BC	

DC Electrical Characteristics (Note 2) — CD4072BM, CD4082BM

Sym	Parameter	Conditions	-55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5.0\text{V}$		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10\text{V}$		0.5		0.005	0.5		15	
		$V_{DD} = 15\text{V}$		1.0		0.006	1.0		30	
V_{OL}	Low Level Output Voltage	$V_{DD} = 5.0\text{V}$		0.05		0	0.05		0.05	V
		$V_{DD} = 10\text{V}$		0.05		0	0.05		0.05	
		$V_{DD} = 15\text{V}$		0.05		0	0.05		0.05	
V_{OH}	High Level Output Voltage	$V_{DD} = 5.0\text{V}$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10\text{V}$	9.95		9.95	10		9.95		
		$V_{DD} = 15\text{V}$	14.95		14.95	15		14.95		
V_{IL}	Low Level Input Voltage	$V_{DD} = 5.0\text{V}, V_O = 0.5\text{V}$ or 4.5V		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10\text{V}, V_O = 1.0\text{V}$ or 9.0V		3.0		4.50	3.0		3.0	
		$V_{DD} = 15\text{V}, V_O = 1.5\text{V}$ or 13.5V		4.0		6.75	4.0		4.0	
V_{IH}	High Level Input Voltage	$V_{DD} = 5.0\text{V}, V_O = 0.5\text{V}$ or 4.5V	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10\text{V}, V_O = 1.0\text{V}$ or 9.0V	7.0		7.0	5.50		7.0		
		$V_{DD} = 15\text{V}, V_O = 1.5\text{V}$ or 13.5V	11.0		11.0	8.25		11.0		
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5.0\text{V}, V_O = 0.4\text{V}$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10\text{V}, V_O = 0.5\text{V}$	1.8		1.3	2.2		0.80		
		$V_{DD} = 15\text{V}, V_O = 1.5\text{V}$	4.2		3.4	8.0		2.4		
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5.0\text{V}, V_O = 4.6\text{V}$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10\text{V}, V_O = 9.5\text{V}$	-1.6		-1.3	-2.2		-0.90		
		$V_{DD} = 15\text{V}, V_O = 13.5\text{V}$	-4.2		-3.4	-8.0		-2.4		
I_{IN}	Input Current	$V_{DD} = 15\text{V}, V_{IN} = 0\text{V}$		-0.10		-10 ⁻⁵	-0.10		-1.0	μA
		$V_{DD} = 15\text{V}, V_{IN} = 15\text{V}$		0.10		10 ⁻⁵	0.10		1.0	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0\text{V}$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics (Note 2) — CD4072BC, CD4082BC

Sym	Parameter	Conditions	-40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		1.0 2.0 4.0		0.004 0.005 0.006	1.0 2.0 4.0		7.5 15 30	μA μA μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		0.05 0.05 0.05		0 0 0	0.05 0.05 0.05	0.05 0.05 0.05	V V V	
V_{OH}	High Level Output Voltage	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	4.95 9.95 14.95		4.95 9.95 14.95	5.0 10 15		4.95 9.95 14.95		V V V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5\text{V}, V_O = 0.5\text{V}$ or 4.5V $V_{DD} = 10\text{V}, V_O = 1.0\text{V}$ or 9.0V $V_{DD} = 15\text{V}, V_O = 1.5\text{V}$ or 13.5V		1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	V V V
V_{IH}	High Level Input Voltage	$V_{DD} = 5.0\text{V}, V_O = 0.5\text{V}$ or 4.5V $V_{DD} = 10\text{V}, V_O = 1.0\text{V}$ or 9.0V $V_{DD} = 15\text{V}, V_O = 1.5\text{V}$ or 13.5V	3.5 7.0 11.0		3.5 7.0 11.0	2.75 5.50 8.25		3.5 7.0 11.0		V V V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5.0\text{V}, V_O = 0.4\text{V}$ $V_{DD} = 10\text{V}, V_O = 0.5\text{V}$ $V_{DD} = 15\text{V}, V_O = 1.5\text{V}$	0.52 1.3 3.6		0.44 1.1 3.0	0.88 2.2 8.0		0.36 0.90 2.4		mA mA mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5.0\text{V}, V_O = 4.6\text{V}$ $V_{DD} = 10\text{V}, V_O = 9.5\text{V}$ $V_{DD} = 15\text{V}, V_O = 13.5\text{V}$	-0.52 -1.3 -3.6		-0.44 -1.1 -3.0	-0.88 -2.2 -8.0		-0.36 -0.90 -2.4		mA mA mA
I_{IN}	Input Current	$V_{DD} = 15\text{V}, V_{IN} = 0\text{V}$ $V_{DD} = 15\text{V}, V_{IN} = 15\text{V}$		-0.3 0.3		-10^{-5} 10^{-5}	-0.3 0.3		-1.0 1.0	μA μA

AC Electrical Characteristics $T_A = 25^\circ\text{C}$, $C_L = 50\text{pF}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay, High to Low Level	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		125 80 45	250 100 70	ns ns ns
t_{PLH}	Propagation Delay, Low to High Level	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		125 80 45	250 100 70	ns ns ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 50 40	200 100 80	ns ns ns
C_{IN}	Average Input Capacitance (Note 4)	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacity (Note 5)	Any Gate		20		pF

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics, Application Note AN-90.