National Semiconductor

54F/74F676
16-Bit Serial/Parallel-In, Serial-Out Shift Register

General Description

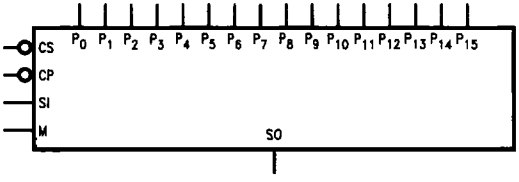
The 'F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is HIGH, information present on the parallel data (P_0–P_{15}) inputs is entered on the falling edge of the Clock Pulse ($\overline{CP}$) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select ($\overline{CS}$) input prevents both parallel and serial operations.

Features

- 16-bit parallel-to-serial conversion
- 16-bit serial-in, serial-out
- Chip select control
- Slim 24 lead 300 mil package

Ordering Code: See Section 5

Logic Symbols



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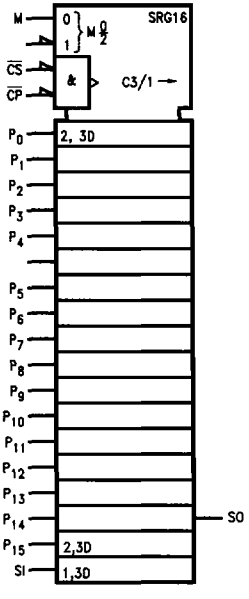
IEEE/IEC



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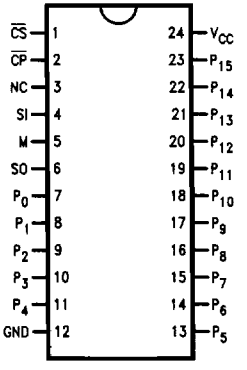
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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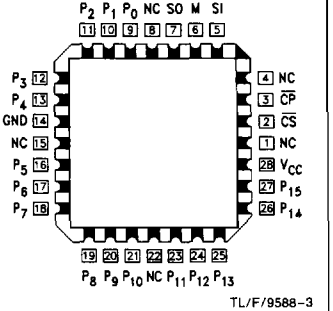
Pin Assignment for LCC and PCC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
P_0-P_{15}	Parallel Data Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{CP}$	Clock Pulse Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
M	Mode Select Input	1.0/1.0	20 μA/−0.6 mA
SI	Serial Data Input	1.0/1.0	20 μA/−0.6 mA
SO	Serial Output	50/33.3	−1 mA/20 mA

Functional Description

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

HOLD—a HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the sixteen registers.

Shift/Serial Load—data present on the SI pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks, finally appearing on the SO pin.

Parallel Load—data present on P_0-P_{15} are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

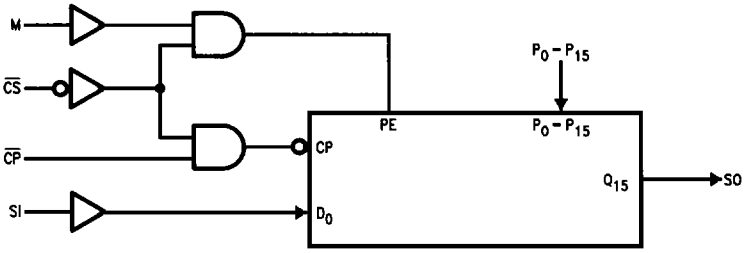
To prevent false clocking, $\overline{CP}$ must be LOW during a LOW-to-HIGH transition of $\overline{CS}$.

Shift Register Operations Table

Control Input			Operating Mode
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	↘	Shift/Serial Load
L	H	↘	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↘ = HIGH-to-LOW Transition

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA
I_{IH}	Input HIGH Current				20	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				100	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current				250	μA	Max	V_{OUT} = V_{CC}
I_{CC}	Power Supply Current				52	mA	Max	

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			54F $T_A, V_{CC} =$ Mil $C_L = 50$ pF		74F $T_A, V_{CC} =$ Com $C_L = 50$ pF		Units	Fig No
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	110		45		90		MHz	2-1
t_{PLH}	Propagation Delay	4.5	9.0	11.0	4.5	17.0	4.5	12.0	ns	2-3
t_{PHL}	$\overline{CP}$ to SO	5.0	9.0	12.5	5.0	14.5	5.0	13.5		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} =$ Mil		74F $T_A, V_{CC} =$ Com		Units	Fig No
		Min	Max	Min	Max	Min	Max		
$t_s(H)$	Setup Time, HIGH or LOW	4.0		4.0		4.0		ns	2-6
$t_s(L)$	SI to $\overline{CP}$	4.0		4.0		4.0			
$t_h(H)$	Hold Time, HIGH or LOW	4.0		4.0		4.0			
$t_h(L)$	SI to $\overline{CP}$	4.0		4.0		4.0			
$t_s(H)$	Setup Time, HIGH or LOW	3.0		3.0		3.0		ns	2-6
$t_s(L)$	P_n to $\overline{CP}$	3.0		3.0		3.0			
$t_h(H)$	Hold Time, HIGH or LOW	4.0		4.0		4.0			
$t_h(L)$	P_n to $\overline{CP}$	4.0		4.0		4.0			
$t_s(H)$	Setup Time, HIGH or LOW	8.0		8.0		8.0		ns	2-6
$t_s(L)$	M to $\overline{CP}$	8.0		8.0		8.0			
$t_h(H)$	Hold Time, HIGH or LOW	2.0		2.0		2.0			
$t_h(L)$	M to $\overline{CP}$	2.0		2.0		2.0			
$t_s(L)$	Setup Time, LOW $\overline{CS}$ to $\overline{CP}$	10.0		12.0		10.0		ns	2-6
$t_h(H)$	Hold Time, HIGH $\overline{CS}$ to $\overline{CP}$	10.0		10.0		10.0			
$t_w(H)$	$\overline{CP}$ Pulse Width	4.0		5.0		4.0		ns	2-4
$t_w(L)$	HIGH or LOW	6.0		9.0		6.0			