National Semiconductor

54F/74F323 Octal Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

General Description

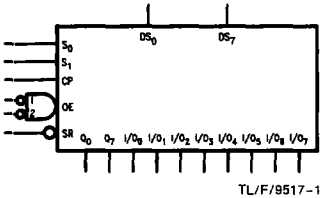
The 'F323 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Its function is similar to the 'F299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

Features

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications

Ordering Code: See Section 5

Logic Symbols



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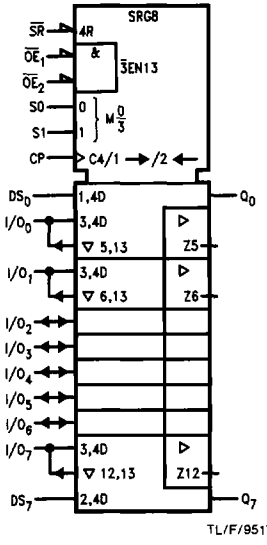
IEEE/IEC



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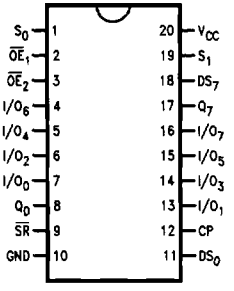
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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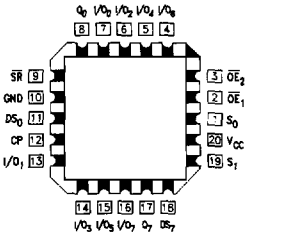
Pin Assignment for LCC and PCC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/ −0.6 mA
DS_0	Serial Data Input for Right Shift	1.0/1.0	20 μA/ −0.6 mA
DS_7	Serial Data Input for Left Shift	1.0/1.0	20 μA/ −0.6 mA
S_0, S_1	Mode Select Inputs	1.0/2.0	20 μA/ −1.2 mA
$\overline{SR}$	Synchronous Reset Input (Active LOW)	1.0/1.0	20 μA/ −0.6 mA
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs (Active LOW)	1.0/1.0	20 μA/ −0.6 mA
I/O_0–I/O_7	Multiplexed Parallel Data Inputs	3.5/1.083	70 μA/ −0.65 mA
	TRI-STATE Parallel Data Outputs	150/40 (33.3)	−3 mA/24 mA (20 mA)
Q_0, Q_7	Serial Outputs	50/33.3	−1 mA/20 mA

Functional Description

The 'F323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

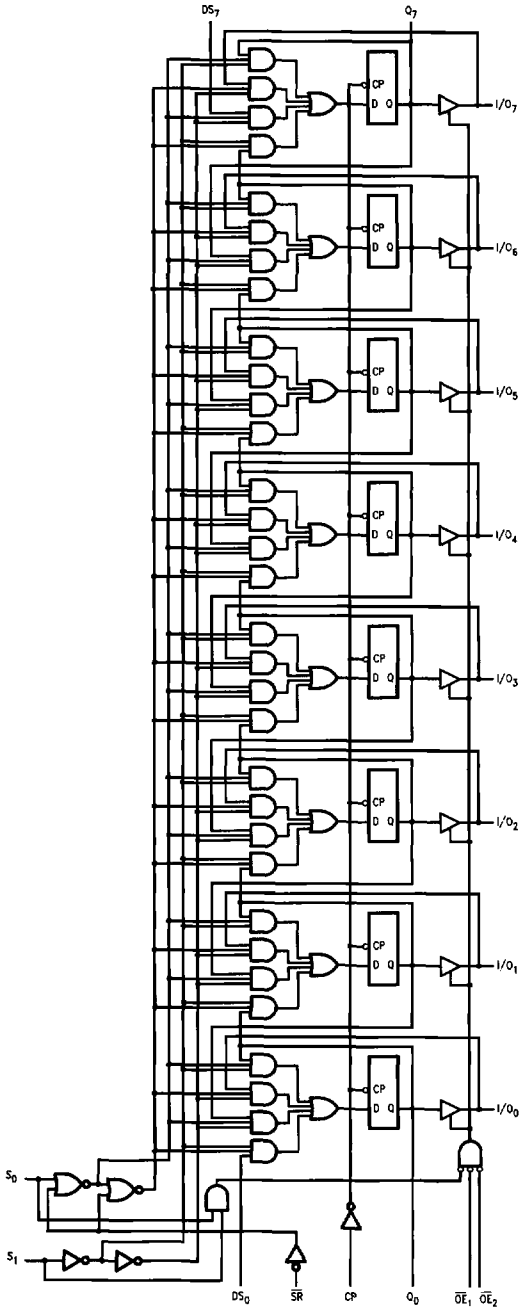
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
$\overline{SR}$	S_1	S_0	CP	
L	X	X	⌐	Synchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (Q_0, Q_7)
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA (I/O_n)
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA (Q_0, Q_7)
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA (I/O_n)
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA (Q_0, Q_7)
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA (I/O_n)
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA (I/O_n, Q_0, Q_7)
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA (Q_0, Q_7)
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA (I/O_n)
I_{IH}	Input HIGH Current				20	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				100	μA	Max	V_{IN} = 7.0V
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				1.0	μA	Max	V_{IN} = 5.5V
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (CP, DS_0, DS_7, $\overline{SR}$, $\overline{OE_1}$, $\overline{OE_2}$)
					−1.2	mA	Max	V_{IN} = 0.5V (S_0, S_1)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current				250	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = V_{CC}
I_{CCH}	Power Supply Current			68	95	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			68	95	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			68	95	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			54F $T_A, V_{CC} = Mil$ $C_L = 50$ pF		74F $T_A, V_{CC} = Com$ $C_L = 50$ pF		Units	Fig No
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	70	100				70		MHz	2-1
t_{PLH}	Propagation Delay	4.0	7.0	9.0			4.0	10.0	ns	2-3
t_{PHL}	CP to Q_0 or Q_7	3.5	6.5	8.5			3.5	9.5		
t_{PLH}	Propagation Delay	4.0	7.0	9.0			4.0	10.0		
t_{PHL}	CP to I/O_n	5.0	8.5	11.0			5.0	12.0		
t_{PZH}	Output Enable Time	3.5	6.0	8.0			3.5	9.0	ns	2-5
t_{PZL}		4.0	7.0	10.0			4.0	11.0		
t_{PHZ}	Output Disable Time	2.5	4.5	6.0			2.5	7.0		
t_{PLZ}		2.0	4.0	5.5			2.0	6.5		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = Mil$		74F $T_A, V_{CC} = Com$		Units	Fig No
		Min	Max	Min	Max	Min	Max		
$t_s(H)$	Setup Time, HIGH or LOW	8.5				8.5		ns	2-6
$t_s(L)$	S_0 or S_1 to CP	8.5				8.5			
$t_h(H)$	Hold Time, HIGH or LOW	0				0			
$t_h(L)$	S_0 or S_1 to CP	0				0			
$t_s(H)$	Setup Time, HIGH or LOW	5.0				5.0		ns	2-6
$t_s(L)$	I/O_n, DS_0, DS_7 to CP	5.0				5.0			
$t_h(H)$	Hold Time, HIGH or LOW	2.0				2.0			
$t_h(L)$	I/O_n, DS_0, DS_7 to CP	2.0				2.0			
$t_s(H)$	Setup Time, HIGH or LOW	10.0				10.0		ns	2-6
$t_s(L)$	$\overline{SR}$ to CP	10.0				10.0			
$t_h(H)$	Hold Time, HIGH or LOW	0				0			
$t_h(L)$	$\overline{SR}$ to CP	0				0			
$t_w(H)$	CP Pulse Width	7.0				7.0		ns	2-4
$t_w(L)$	HIGH or LOW	7.0				7.0			