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# 54F/74F827 • 74F828
# 10-Bit Buffers/Line Drivers

## General Description

The 'F827 and 'F828 10-bit bus buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility.

The 'F827 and 'F828 are functionally- and pin-compatible to AMD's Am29827 and Am29828. The 'F828 is an inverting version of the 'F827.

## Features

- TRI-STATE® output
- 'F828 is inverting
- Direct replacement for AMD's Am29827 and Am29828

## Ordering Code: See Section 11

| Commercial | Military | Package Number | Package Description |
|---|---|---|---|
| 74F827SPC | | N24C | 24-Lead (0.300″ Wide) Molded Dual-In-Line |
| | 54F827SDM (Note 2) | J24F | 24-Lead (0.300″ Wide) Ceramic Dual-In-Line |
| 74F827SC (Note 1) | | M24B | 24-Lead (0.300″ Wide) Molded Small Outline, JEDEC |
| | 54F827FM (Note 2) | W24C | 24-Lead Cerpack |
| | 54F827LM (Note 2) | E28A | 24-Lead Ceramic Leadless Chip Carrier, Type C |
| 74F828SPC | | N24C | 24-Lead (0.300″ Wide) Molded Dual-In-Line |
| 74F828SC (Note 1) | | M24B | 24-Lead (0.300″ Wide) Molded Small Outline, JEDEC |

Note 1: Devices also available in 13″ reel. Use suffix = SCX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = SDMQB, FMQB and LMQB.

## Connection Diagrams

**Pin Assignment for DIP, Flatpak and SOIC**

'F827

| | | | |
|---|---|---|---|
| $\overline{OE}_1$ | 1 | 24 | $V_{CC}$ |
| $D_0$ | 2 | 23 | $O_0$ |
| $D_1$ | 3 | 22 | $O_1$ |
| $D_2$ | 4 | 21 | $O_2$ |
| $D_3$ | 5 | 20 | $O_3$ |
| $D_4$ | 6 | 19 | $O_4$ |
| $D_5$ | 7 | 18 | $O_5$ |
| $D_6$ | 8 | 17 | $O_6$ |
| $D_7$ | 9 | 16 | $O_7$ |
| $D_8$ | 10 | 15 | $O_8$ |
| $D_9$ | 11 | 14 | $O_9$ |
| GND | 12 | 13 | $\overline{OE}_2$ |

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'F828

| | | | |
|---|---|---|---|
| $\overline{OE}_1$ | 1 | 24 | $V_{CC}$ |
| $D_0$ | 2 | 23 | $\overline{O}_0$ |
| $D_1$ | 3 | 22 | $\overline{O}_1$ |
| $D_2$ | 4 | 21 | $\overline{O}_2$ |
| $D_3$ | 5 | 20 | $\overline{O}_3$ |
| $D_4$ | 6 | 19 | $\overline{O}_4$ |
| $D_5$ | 7 | 18 | $\overline{O}_5$ |
| $D_6$ | 8 | 17 | $\overline{O}_6$ |
| $D_7$ | 9 | 16 | $\overline{O}_7$ |
| $D_8$ | 10 | 15 | $\overline{O}_8$ |
| $D_9$ | 11 | 14 | $\overline{O}_9$ |
| GND | 12 | 13 | $\overline{OE}_2$ |
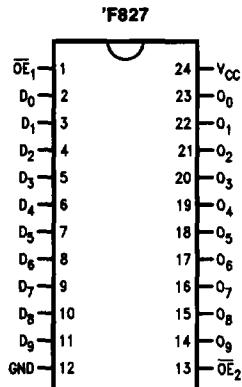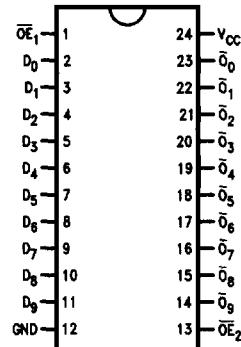
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**Pin Assignment for LCC**
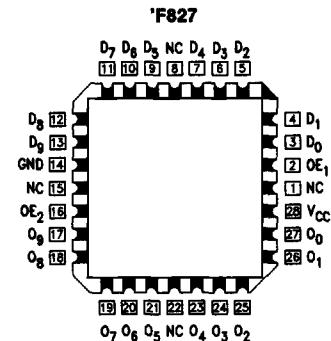
'F827

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# Logic Symbols

### IEEE/IEC
### 'F827

$\overline{OE}_1$  
$\overline{OE}_2$  
& EN1

| $D_0$ | | $O_0$ |
| $D_1$ | | $O_1$ |
| $D_2$ | | $O_2$ |
| $D_3$ | | $O_3$ |
| $D_4$ | | $O_4$ |
| $D_5$ | | $O_5$ |
| $D_6$ | | $O_6$ |
| $D_7$ | | $O_7$ |
| $D_8$ | | $O_8$ |
| $D_9$ | | $O_9$ |

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### IEEE/IEC
### 'F828

$\overline{OE}_1$  
$\overline{OE}_2$  
& EN1

| $D_0$ | | $\overline{O}_0$ |
| $D_1$ | | $\overline{O}_1$ |
| $D_2$ | | $\overline{O}_2$ |
| $D_3$ | | $\overline{O}_3$ |
| $D_4$ | | $\overline{O}_4$ |
| $D_5$ | | $\overline{O}_5$ |
| $D_6$ | | $\overline{O}_6$ |
| $D_7$ | | $\overline{O}_7$ |
| $D_8$ | | $\overline{O}_8$ |
| $D_9$ | | $\overline{O}_9$ |

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### 'F827

$D_0$ $D_1$ $D_2$ $D_3$ $D_4$ $D_5$ $D_6$ $D_7$ $D_8$ $D_9$

$OE_1$  
$OE_2$

$O_0$ $O_1$ $O_2$ $O_3$ $O_4$ $O_5$ $O_6$ $O_7$ $O_8$ $O_9$

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### 'F828

$D_0$ $D_1$ $D_2$ $D_3$ $D_4$ $D_5$ $D_6$ $D_7$ $D_8$ $D_9$

$OE_1$  
$OE_2$

$O_0$ $O_1$ $O_2$ $O_3$ $O_4$ $O_5$ $O_6$ $O_7$ $O_8$ $O_9$

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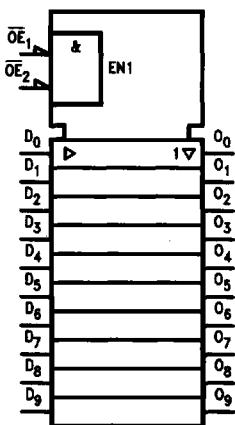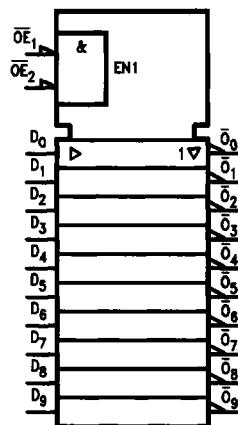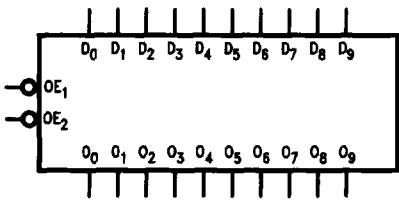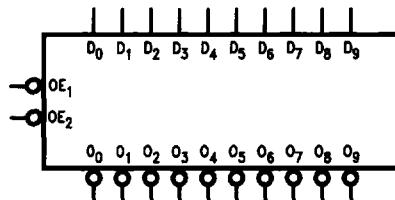
## Unit Loading/Fan Out: See Section 2 for U.L. definitions

| Pin Names | Description | 54F/74F | |
|-----------|-------------|---------|---|
| | | U.L. HIGH/LOW | Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$ |
| $\overline{OE}_1$, $\overline{OE}_2$ | Output Enable Input | 1.0/1.0 | 20 μA/ −0.6 mA |
| $D_0$–$D_7$ | Data Inputs | 1.0/1.0 | 20 μA/ −0.6 mA |
| $O_0$–$O_7$ | Data Outputs, TRI-STATE | 600/106.6 (80) | −12 mA/64 mA (48 mA) |

## Functional Description

The 'F827 and 'F828 are line drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density. The devices have TRI-STATE outputs controlled by the Output Enable ($\overline{OE}$) pins. The outputs can sink 64 mA (48 mA mil) and source 15 mA. Input clamp diodes limit high-speed termination effects.

### Function Table

| Inputs | | Outputs | | |
|--------|---|---------|---|----------|
| | | $O_n$ | | Function |
| $\overline{OE}$ | $D_n$ | 'F827 | 'F828 | |
| L | H | H | L | Transparent |
| L | L | L | H | Transparent |
| H | X | Z | Z | High Z |

H = HIGH Voltage level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

## Logic Diagrams

'F827
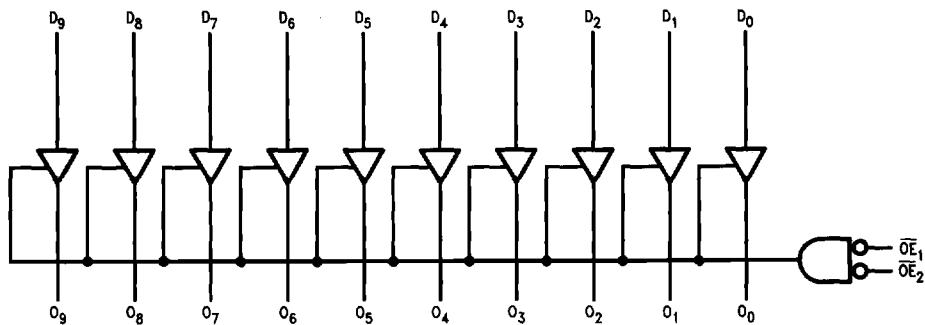


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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'F828
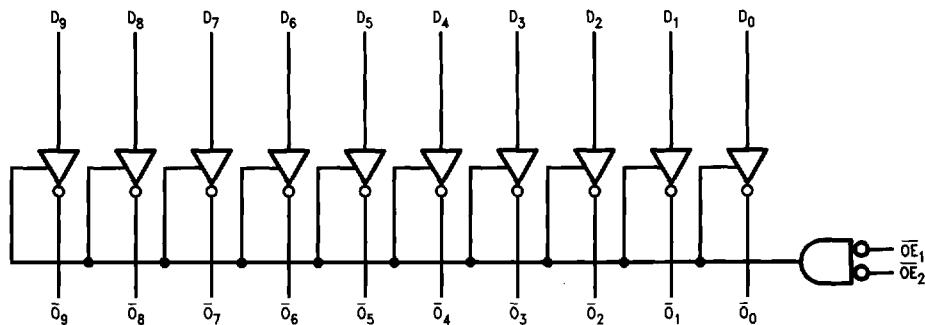


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Storage Temperature | $-65°C$ to $+150°C$ |
| Ambient Temperature under Bias | $-55°C$ to $+125°C$ |
| Junction Temperature under Bias | $-55°C$ to $+175°C$ |
| Plastic | $-55°C$ to $+150°C$ |
| $V_{CC}$ Pin Potential to Ground Pin | $-0.5V$ to $+7.0V$ |
| Input Voltage (Note 2) | $-0.5V$ to $+7.0V$ |
| Input Current (Note 2) | $-30$ mA to $+5.0$ mA |
| Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$) | |
| Standard Output | $-0.5V$ to $V_{CC}$ |
| TRI-STATE Output | $-0.5V$ to $+5.5V$ |
| Current Applied to Output in LOW State (Max) | twice the rated $I_{OL}$ (mA) |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | |
| Military | $-55°C$ to $+125°C$ |
| Commercial | $0°C$ to $+70°C$ |
| Supply Voltage | |
| Military | $+4.5V$ to $+5.5V$ |
| Commercial | $+4.5V$ to $+5.5V$ |

## DC Electrical Characteristics

| Symbol | Parameter | | 54F/74F Min | 54F/74F Typ | 54F/74F Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | | Recognized as a HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V | | Recognized as a LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | | $-1.2$ | V | Min | $I_{IN} = -18$ mA |
| $V_{OH}$ | Output HIGH Voltage | 54F 10% $V_{CC}$ | 2.4 | | | | | $I_{OH} = -3$ mA |
| | | 54F 10% $V_{CC}$ | 2.0 | | | | | $I_{OH} = -12$ mA |
| | | 74F 10% $V_{CC}$ | 2.4 | | | V | Min | $I_{OH} = -3$ mA |
| | | 74F 10% $V_{CC}$ | 2.0 | | | | | $I_{OH} = -15$ mA |
| | | 74F 5% $V_{CC}$ | 2.7 | | | | | $I_{OH} = -3$ mA |
| $V_{OL}$ | Output LOW Voltage | 54F 10% $V_{CC}$ | | | 0.55 | V | Min | $I_{OL} = 48$ mA |
| | | 74F 10% $V_{CC}$ | | | 0.55 | | | $I_{OL} = 64$ mA |
| $I_{IH}$ | Input HIGH Current | 54F | | | 20.0 | $\mu$A | Max | $V_{IN} = 2.7V$ |
| | | 74F | | | 5.0 | | | |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | 54F | | | 100 | $\mu$A | Max | $V_{IN} = 7.0V$ |
| | | 74F | | | 7.0 | | | |
| $I_{CEX}$ | Output HIGH Leakage Current | 54F | | | 250 | $\mu$A | Max | $V_{OUT} = V_{CC}$ |
| | | 74F | | | 50 | | | |
| $V_{ID}$ | Input Leakage Test | 74F | 4.75 | | | V | 0.0 | $I_{ID} = 1.9 \mu$A All Other Pins Grounded |
| $I_{OD}$ | Output Leakage Circuit Current | 74F | | | 3.75 | $\mu$A | 0.0 | $V_{IOD} = 150$ mV All Other Pins Grounded |
| $I_{IL}$ | Input LOW Current | | | | $-0.6$ | mA | Max | $V_{IN} = 0.5V$ |
| $I_{OZH}$ | Output Leakage Current | | | | 50 | $\mu$A | Max | $V_{OUT} = 2.7V$ |
| $I_{OZL}$ | Output Leakage Current | | | | $-50$ | $\mu$A | Max | $V_{OUT} = 0.5V$ |
| $I_{OS}$ | Output Short-Circuit Current | | $-100$ | | $-225$ | mA | Max | $V_{OUT} = 0V$ |

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## DC Electrical Characteristics (Continued)

| Symbol | Parameter | 54F/74F | | | Units | $V_{CC}$ | Conditions |
|--------|-----------|---------|---|---|-------|----------|------------|
| | | Min | Typ | Max | | | |
| $I_{ZZ}$ | Bus Drainage Test | | | 500 | $\mu A$ | 0.0V | $V_{OUT} = 5.25V$ |
| $I_{CCH}$ | Power Supply Current ('F827) | | 30 | 45 | mA | Max | $V_O = HIGH$ |
| $I_{CCL}$ | Power Supply Current ('F827) | | 60 | 90 | mA | Max | $V_O = LOW$ |
| $I_{CCZ}$ | Power Supply Current ('F827) | | 40 | 60 | mA | Max | $V_O = HIGH\ Z$ |
| $I_{CCH}$ | Power Supply Current ('F828) | | 14 | 20 | mA | Max | $V_O = HIGH$ |
| $I_{CCL}$ | Power Supply Current ('F828) | | 56 | 85 | mA | Max | $V_O = LOW$ |
| $I_{CCZ}$ | Power Supply Current ('F828) | | 35 | 50 | mA | Max | $V_O = HIGH\ Z$ |

## AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

| Symbol | Parameter | 74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$ | | | 54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$ | | 74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$ | | Units | Fig. No. |
|--------|-----------|------|------|------|------|------|------|------|-------|------|
| | | Min | Typ | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation Delay | 1.0 | 3.0 | 5.5 | 1.0 | 7.5 | 1.0 | 6.5 | ns | 2–3 |
| $t_{PHL}$ | Data to Output ('F827) | 1.5 | 3.3 | 5.5 | 1.5 | 7.0 | 1.5 | 6.0 | | |
| $t_{PLH}$ | Propagation Delay | 1.0 | 3.0 | 5.0 | | | 1.0 | 5.5 | ns | 2–3 |
| $t_{PHL}$ | Data to Output ('F828) | 1.0 | 2.0 | 4.0 | | | 1.0 | 4.0 | | |
| $t_{PZH}$ | Output Enable Time | 3.0 | 5.7 | 9.0 | 2.5 | 10.0 | 2.5 | 9.5 | ns | 2–5 |
| $t_{PZL}$ | $\overline{OE}$ to $O_n$ | 3.5 | 6.8 | 11.5 | 3.0 | 12.5 | 3.0 | 12.0 | | |
| $t_{PHZ}$ | Output Disable Time | 1.5 | 3.3 | 8.0 | 1.5 | 9.0 | 1.5 | 8.5 | ns | 2–5 |
| $t_{PLZ}$ | $\overline{OE}$ to $O_n$ | 1.0 | 3.5 | 8.0 | 1.0 | 9.0 | 1.0 | 8.5 | | |