

54AC/74AC378 Parallel D Register with Enable

General Description

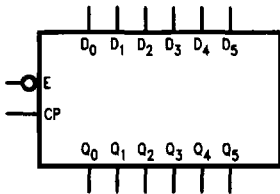
The 'AC378 is a 6-bit register with a buffered common Enable. This device is similar to the 'AC174, but with common Enable rather than common Master Reset.

Features

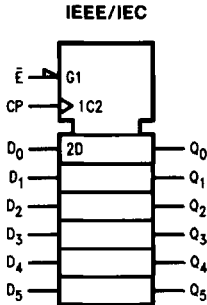
- 6-bit high-speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common clock and enable inputs
- Input clamp diodes limit high-speed termination effects

Ordering Code: See Section 8

Logic Symbols



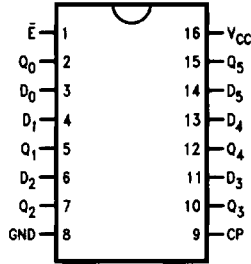
TL/F/10231-1



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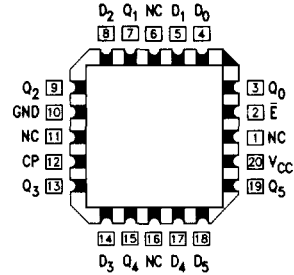
Connection Diagrams

Pin Assignment for
DIP, SOIC and Flatpak



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Pin Assignment
for LCC



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Pin Names	Description
E	Enable Input (Active LOW)
D ₀ -D ₅	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q ₀ -Q ₅	Outputs

Functional Description

The 'AC378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable (E) inputs are common to all flip-flops.

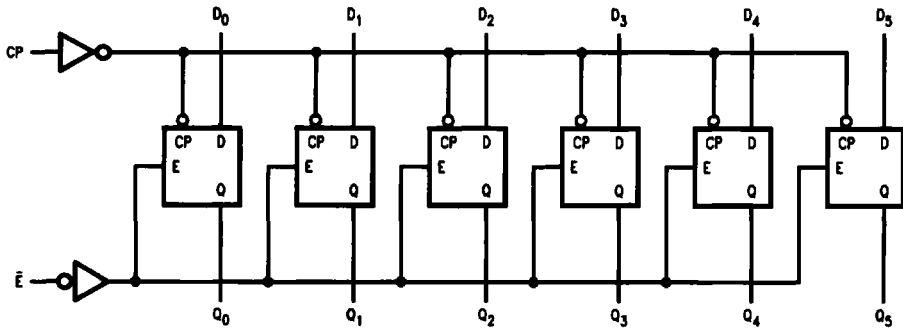
When the \bar{E} input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the \bar{E} input is HIGH the register will retain the present data independent of the CP input.

Truth Table

Inputs			Output
E	CP	D _n	Q _n
H	↗	X	No Change
L	↗	H	H
L	↗	L	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↗ = LOW-to-HIGH Clock Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTM™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	-40°C to +85°C
54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC		54AC	74AC	Units	Conditions	
			$T_A = +25^\circ\text{C}$		$T_A =$ -55°C to +125°C	$T_A =$ -40°C to +85°C			
			Typ	Guaranteed Limits					
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15	3.15			
		5.5	2.75	3.85	3.85	3.85			
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35	1.35			
		5.5	2.75	1.65	1.65	1.65			
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$	
		4.5	4.49	4.4	4.4	4.4			
		5.5	5.49	5.4	5.4	5.4			
			3.0		2.56	2.4	2.46	V	* $V_{IN} = V_{IL}$ or V_{IH} -12 mA I_{OH} -24 mA -24 mA
			4.5		3.86	3.7	3.76		
			5.5		4.86	4.7	4.76		
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		4.5	0.001	0.1	0.1	0.1			
		5.5	0.001	0.1	0.1	0.1			
			3.0		0.36	0.5	0.44	V	* $V_{IN} = V_{IL}$ or V_{IH} 12 mA I_{OL} 24 mA 24 mA
			4.5		0.36	0.5	0.44		
			5.5		0.36	0.5	0.44		
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	± 1.0	μA	$V_I = V_{CC}, \text{GND}$	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74AC		54AC		74AC		Units	Conditions
			T _A = +25°C		T _A = -55°C to +125°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits						
I _{OLD}	†Minimum Dynamic Output Current	5.5			50		75		mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			-50		-75		mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0		40.0		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	125 160	160 200		95 95		110 145		MHz	
t _{PLH}	Propagation Delay CP to Q _n	3.3 5.0	2.5 1.5	8.5 6.0	11.0 8.0	1.5 1.5	12.0 9.0	2.5 1.5	12.5 9.0	ns	2-3, 4
t _{PHL}	Propagation Delay CP to Q _n	3.3 5.0	2.5 1.5	8.0 5.5	10.5 7.5	1.5 1.5	12.0 7.5	2.5 1.5	11.0 8.0	ns	2-3, 4

*Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74AC		54AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum						
t _s	Setup Time, HIGH or LOW D _n to CP	3.3 5.0	1.5 1.0	3.0 2.0		4.0 4.0		3.5 2.5	ns	2-7
t _h	Hold Time, HIGH or LOW D _n to CP	3.3 5.0	1.0 1.0	2.0 2.0		4.0 4.0		2.0 2.0	ns	2-7
t _s	Setup Time, HIGH or LOW, \bar{E} to CP	3.3 5.0	0 0	2.0 2.0		2.5 2.5		2.0 2.0	ns	2-7
t _h	Hold Time, HIGH or LOW, \bar{E} to CP	3.3 5.0	1.0 1.0	2.0 2.0		4.0 4.0		2.0 2.0	ns	2-7
t _w	CP Pulse Width HIGH or LOW	3.3 5.0	3.0 2.0	4.5 3.5		6.5 6.5		5.5 4.0	ns	2-3

*Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	28	pF	V _{CC} = 5.0V