National Semiconductor

F100341
Low Power 8-Bit Shift Register

General Description

The F100341 contains eight edge-triggered, D-type flip-flops with individual inputs (P_n) and outputs (Q_n) for parallel operation, and with serial inputs (D_n) and steering logic for bidirectional shifting. The flip-flops accept input data a setup time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

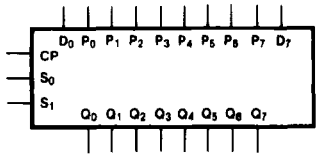
The circuit operating mode is determined by the Select inputs S_0 and S_1, which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as described in the Truth Table. All inputs have 50 kΩ pull-down resistors.

Features

- 35% power reduction of the F100141
- 2000V ESD protection
- Pin/function compatible with F100141
- Voltage compensated operating range = −4.2V to −5.7V

Ordering Code: See Section 8

Logic Symbol



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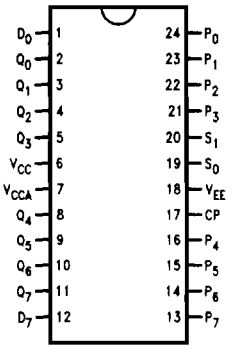
Pin Names	Description
CP	Clock Input
S_0, S_1	Select Inputs
D_0, D_7	Serial Inputs
P_0–P_7	Parallel Inputs
Q_0–Q_7	Data Outputs

Connection Diagrams

24-Pin DIP



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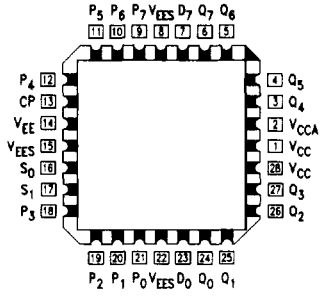
28-Pin PCC



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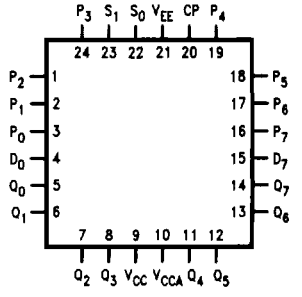
24-Pin Quad Cerpak



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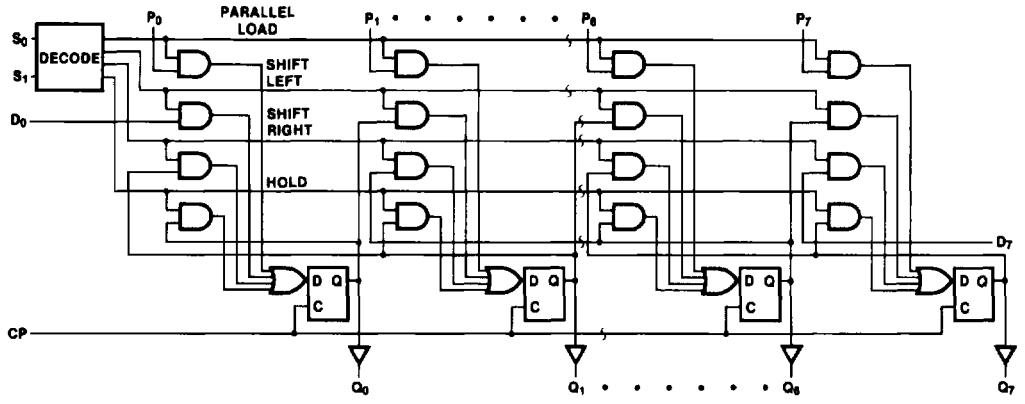
Logic Diagram



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Truth Table

Function	Inputs					Outputs							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Load Register	X	X	L	L	↗	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X	L	L	H	↗	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	H	L	H	↗	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	↗	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	↗	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	No Change							
Hold	X	X	X	X	H								
Hold	X	X	X	X	L								

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↗ = LOW-to-HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	
Commercial	−5.7V to −4.2V
Military	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for all Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for all Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current					Inputs Open	
		−157		−75	mA	V_{EE} = −4.2V to −4.8V	
		−167		−75	mA	V_{EE} = −4.2V to −5.7V	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency	400		400		400		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	1.90	1.00	2.00	1.00	2.10	ns	*Figures 1* and *3* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.30	0.35	1.30	0.35	1.30	ns	*Figures 1* and *3*
t_s	Setup Time D_n, P_n S_n	0.65 1.60		0.65 1.60		0.65 1.60		ns	*Figure 4*
t_h	Hold D_n, P_n S_n	0.80 0.60		0.80 0.60		0.80 0.60		ns	
$t_{pw}(H)$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figure 3*

Note 1: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency	425		425		425		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	1.70	1.00	1.80	1.00	1.90	ns	*Figures 1* and *3* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	*Figures 1* and *3*
t_s	Setup Time D_n, P_n S_n	0.55 1.50		0.55 1.50		0.55 1.50		ns	*Figure 4*
t_h	Hold Time D_n, P_n S_n	0.70 0.50		0.70 0.50		0.70 0.50		ns	
$t_{pw}(H)$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figure 3*
t_s, G–G	Skew, Gate to Gate		TBD		TBD		TBD	ns	PCC Only (Note 2)

Note 1: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

Note 2: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Military Version—Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Current	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input High Current		240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
			340	μA	−55°C			
I_{EE}	Power Supply Current	−168	−55	mA	−55°C to +125°C	Inputs Open V_{EE} = −4.2V to −4.8V		1, 2, 3
		−178	−55	mA		V_{EE} = −4.2V to −5.7V		

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specifications which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version—Preliminary (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Max Clock Frequency	400		400		300		MHz	*Figures 2* and *3*	4
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.50	2.50	0.70	2.30	0.70	2.80	ns	*Figures 1* and *3*	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.90	0.30	1.80	0.30	1.90	ns		
t_s	Setup Time D_n, P_n S_n	0.60 1.70		0.60 1.60		0.60 2.40		ns	*Figure 4*	4
t_h	Hold Time D_n, P_n S_n	0.90 0.50		0.90 0.50		0.90 0.50		ns		
$t_{pw}(H)$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figure 3*	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Max Clock Frequency	425		425		350		MHz	*Figures 2* and *3*	4
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.50	2.50	0.70	2.30	0.70	2.80	ns	*Figures 1* and *3*	1, 2 ,3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.90	0.30	1.80	0.30	1.90	ns		
t_s	Setup Time D_n, P_n S_n	0.60 1.70		0.60 1.60		0.60 2.40		ns	*Figure 4*	4
t_h	Hold Time D_n, P_n S_n	0.90 0.50		0.90 0.50		0.90 0.50		ns		
$t_{pw}(H)$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figure 3*	

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specifications which can be considered a worst case condition at cold temperatures.

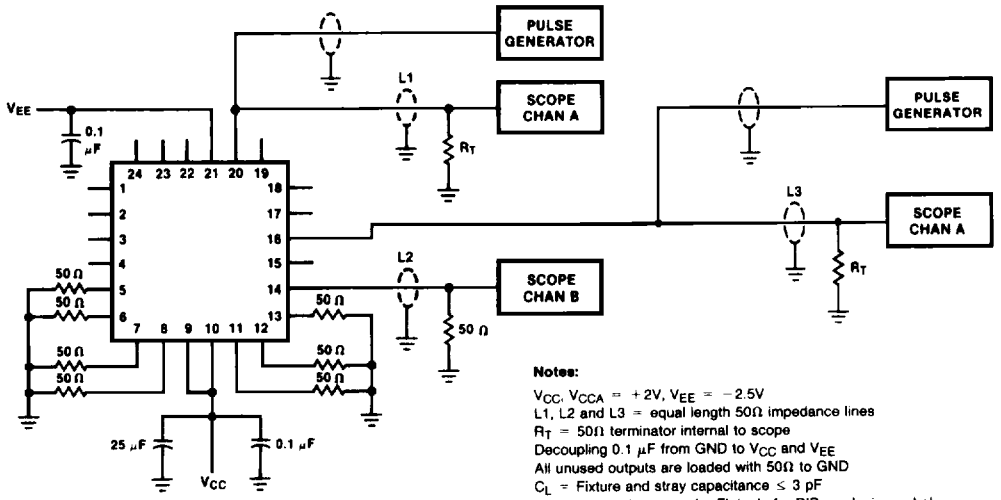
Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

Test Circuitry



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1, L2 and L3 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for Flatpak; for DIP see logic symbol

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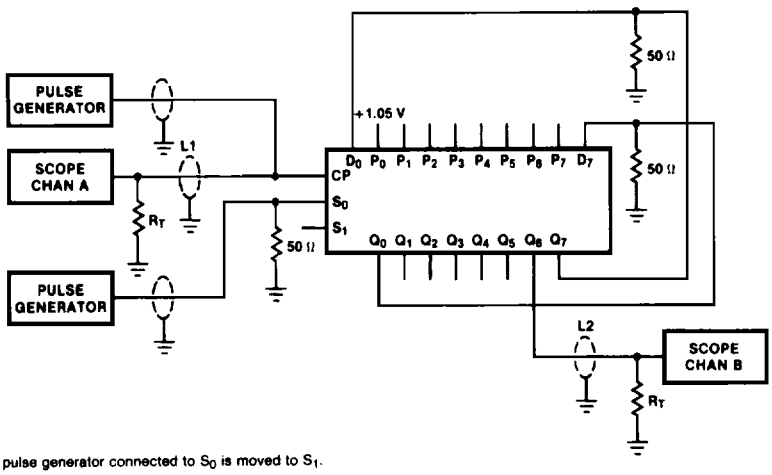
FIGURE 1. AC Test Circuit



Notes:

For shift right mode pulse generator connected to S_0 is moved to S_1.

Pulse generator connected to S_1 has a LOW frequency 99% duty cycle, which allows occasional parallel load.

The feedback path from output to input should be as short as possible.

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FIGURE 2. Shift Frequency Test Circuit (Shift Left)

Switching Waveforms

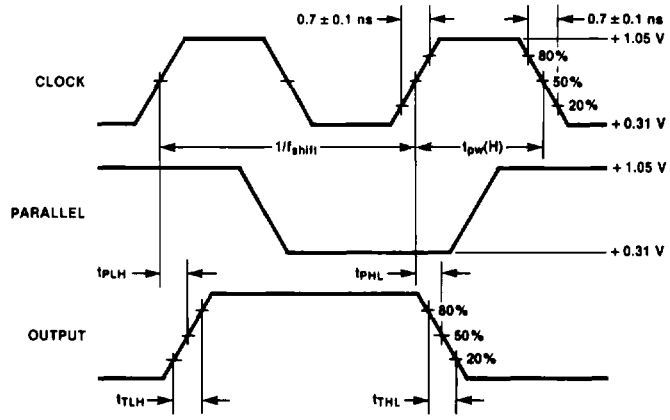

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FIGURE 3. Propagation Delay and Transition Times

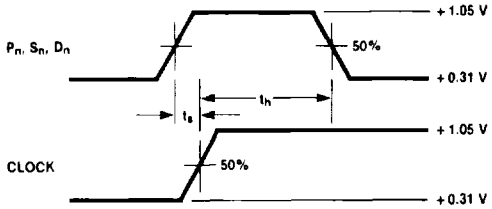

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FIGURE 4. Setup and Hold Times

Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.