National Semiconductor

74ACTQ823
Quiet Series 9-Bit D Flip-Flop with TRI-STATE® Outputs

General Description

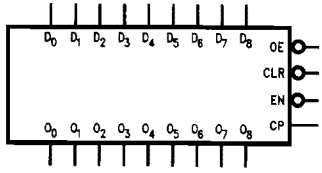
The 'ACTQ823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The ACTQ823 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Improved latch-up immunity
- 'ACTQ823 has TTL-compatible inputs
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

Logic Symbols



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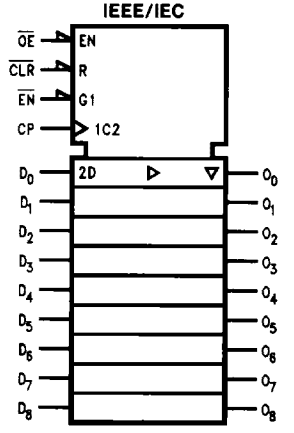

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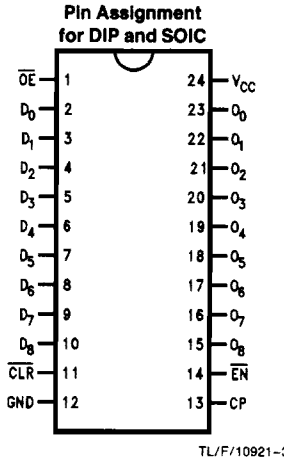
Connection Diagram



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Pin Names	Description
D_0–D_8	Data Inputs
O_0–O_8	Data Outputs
$\overline{OE}$	Output Enable
$\overline{CLR}$	Clear
CP	Clock Input
$\overline{EN}$	Clock Enable

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Functional Description

The 'ACTQ823 consists of nine D-type edge-triggered flip-flops. These have TRI-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}$ LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These devices are ideal for parity bus interfacing in high performance systems.

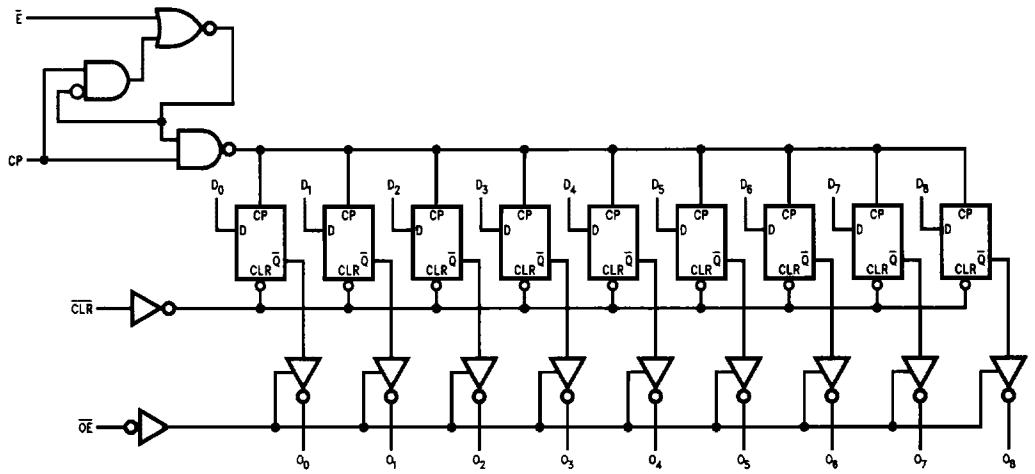
When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	Q	O	
H	X	L	↗	L	L	Z	High Z
H	X	L	↗	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↗	L	L	Z	Load
H	H	L	↗	H	H	Z	Load
L	H	L	↗	L	L	L	Load
L	H	L	↗	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) $-0.5V$ to $+7.0V$

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ -20 mA
- $V_I = V_{CC} + 0.5V$ $+20$ mA

DC Input Voltage (V_I) $-0.5V$ to $V_{CC} + 0.5V$

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ -20 mA
- $V_O = V_{CC} + 0.5V$ $+20$ mA

DC Output Voltage (V_O) $-0.5V$ to $V_{CC} + 0.5V$

DC Output Source or Sink Current (I_O) ± 50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ± 50 mA

Storage Temperature (T_{STG}) $-65°C$ to $+150°C$

DC Latch-Up Source or Sink Current ± 300 mA

Junction Temperature (T_J)
- PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})
- 'ACTQ 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74ACTQ $-40°C$ to $+85°C$

Minimum Input Edge Rate $\Delta V/\Delta t$
- 'ACTQ Devices
- V_{IN} from 0.8V to 2.0V
- V_{CC} @ 4.5V, 5.5V 125 mV/ns

Note 2: All commercial packaging is not recommended for applications requiring greater than 200 temperature cycles from $-65°C$ to $+150°C$.

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4		$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} -24 mA
		5.5		4.86	4.76		I_{OH} -24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		± 0.5	± 5.0	μA	$V_I = V_{IL}$, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			-75	mA	$V_{OHD} = 3.85V$ Min

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

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DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5		V	*Figures 2-12, 13* (Notes 1, 2)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2		V	*Figures 2-12, 13* (Notes 1, 2)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2		V	(Notes 1, 3)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8		V	(Notes 1, 3)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: PDIP package.

Note 2: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 3: Max number of data inputs (n) switching. (n − 1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
t_{PLH}, t_{PHL}	Propagation Delay CP to O_n	5.0	2.0	7.0	9.0	2.0	10.0	ns	2-3, 4
t_{PLH}, t_{PHL}	Propagation Delay CLR to O_n	5.0	2.0	7.0	9.0	2.0	10.0	ns	2-3, 4
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.5	8.0	10.0	2.5	11.0	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.0	6.0	8.0	1.0	9.0	ns	2-5, 6
t_{OSLH}, t_{OSHL}	Output to Output Skew** D_n to O_n	5.0		0.5	1.0		1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$ $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D to CP	5.0	0.5	3.0	3.0	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.5	1.5	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	5.0	0	3.0	3.0	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	5.0	0	1.5	1.5	ns	2-7
t_w	CP Pulse Width HIGH or LOW	5.0	2.5	4.0	4.0	ns	2-4
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	3.0	4.0		ns	2-4
t_{rec}	$\overline{CLR}$ to CP Recovery Time	5.0	1.5	3.5	4.0	ns	2-4, 7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	54	pF	V_{CC} = 5.0V