MX66L1G45J

3V, 1G-BIT [x 1/x 2/x 4]
CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY

Key Features

- *Protocol Support - Single I/O, Dual I/O and Quad I/O*
- *Supports DTR (Double Transfer Rate) Mode*
- *Supports clock frequencies up to 133MHz*

Contents

3V 1G-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- Single Power Supply Operation
  - 2.7 to 3.6 volts for read, erase, and program operations
- 1,073,741,824 x 1 bit structure
  or 536,870,912 x 2 bits (two I/O mode) structure
  or 268,435,456 x 4 bits (four I/O mode) structure
- Protocol Support
  - Single I/O, Dual I/O and Quad I/O
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.5V to 2.5V
- Fast read for SPI mode
  - Supports clock frequencies up to 166MHz for all protocols
  - Supports Fast Read, 2READ, DREAD, 4READ, QREAD instructions
  - Supports DTR (Double Transfer Rate) Mode
  - Configurable dummy cycle number for fast read operation
- Supports Performance Enhance Mode - XIP (execute-in-place)
- Quad Peripheral Interface (QPI) available
- Equal 4K byte Sectors, or Equal Blocks with 32K byte or 64K byte each
  - Any Block can be erased individually
- Programming :
  - 256byte page buffer
  - Quad Input/Output page program(4PP) to enhance program performance
- ECC (Error Checking and Correcting): to prevent the data storage errors
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
  The BP0-BP3 and T/B status bits define the size of the area to be protected against program and erase instructions
  - Advanced sector protection function (Solid Protect)
- Additional 4K bit secure OTP
  - Features unique identifier
  - Factory locked identifiable, and customer lockable
- Command Reset
- Program/Erase Suspend and Resume operation
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Supports Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware Write Protection or Serial Data Input/Output for 4 x I/O read mode
- RESET#/SIO3
  - Hardware Reset pin or Serial Data Input/Output for 4 x I/O read mode
- RESET#
  - Hardware Reset pin
- NC/SIO3
  - No Connection or Serial Data Input/Output for 4 x I/O read mode
- PACKAGE
  - 16-pin SOP (300mil)
  - 8-land WSON (8x6mm 3.4 x 4.3EP)
  - 24-Ball BGA (5x5 ball array)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX66L1G45J is 1Gb bits Serial NOR Flash memory, which is configured as 134,217,728 x 8 internally. When it is in two or four I/O mode, the structure becomes 536,870,912 bits x 2 or 268,435,456 bits x 4. MX66L1G45J features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# and RESET# pin (of the 8-pin package) become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX66L1G45J MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for erase command is executed on 4K-byte sector, 32K-byte block, or 64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please refer to the security features section for more details.

When the device is not in operation and CS# is high, it will remain in standby mode.

The MX66L1G45J utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

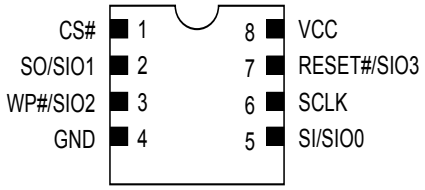
Table 1. Read performance Comparison

Numbers of Dummy Cycles	Fast Read (MHz)	Dual Output Fast Read (MHz)	Quad Output Fast Read (MHz)	Dual IO Fast Read (MHz)	Quad IO Fast Read (MHz)	Quad I/O DT Read (MHz)
4	-	-	-	80*	54	-
6	-	-	-	-	70*	54*
8	120*/133R	120*/133R	104/114R	104/114R	84/95R	70/80R
10	-	-	-	-	104/114R	84/100R

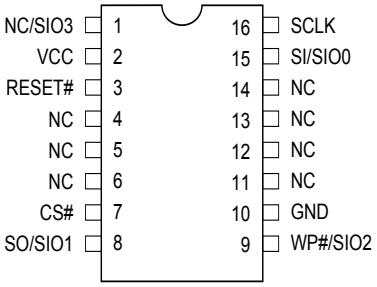
Notes:
1. * Default Status.
2. R mean VCC range = 3.0V-3.6V.

3. PIN CONFIGURATIONS

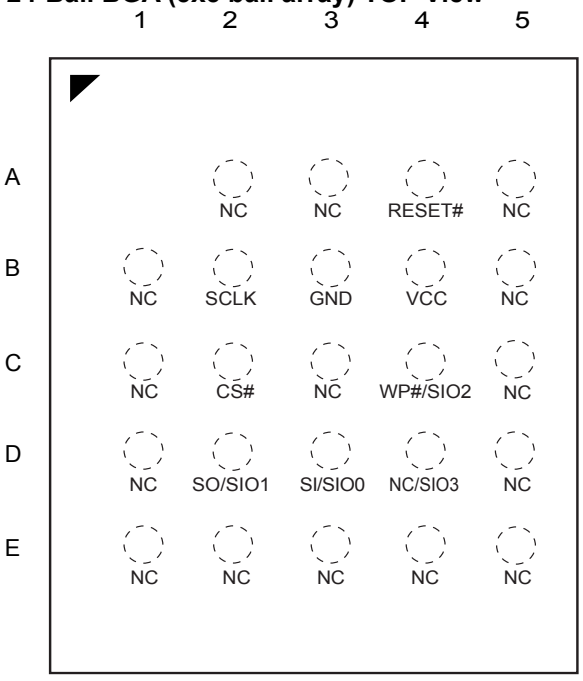
8-WSON (8x6mm 3.4 x 4.3EP)



16-PIN SOP (300mil)



24-Ball BGA (5x5 ball array) TOP View



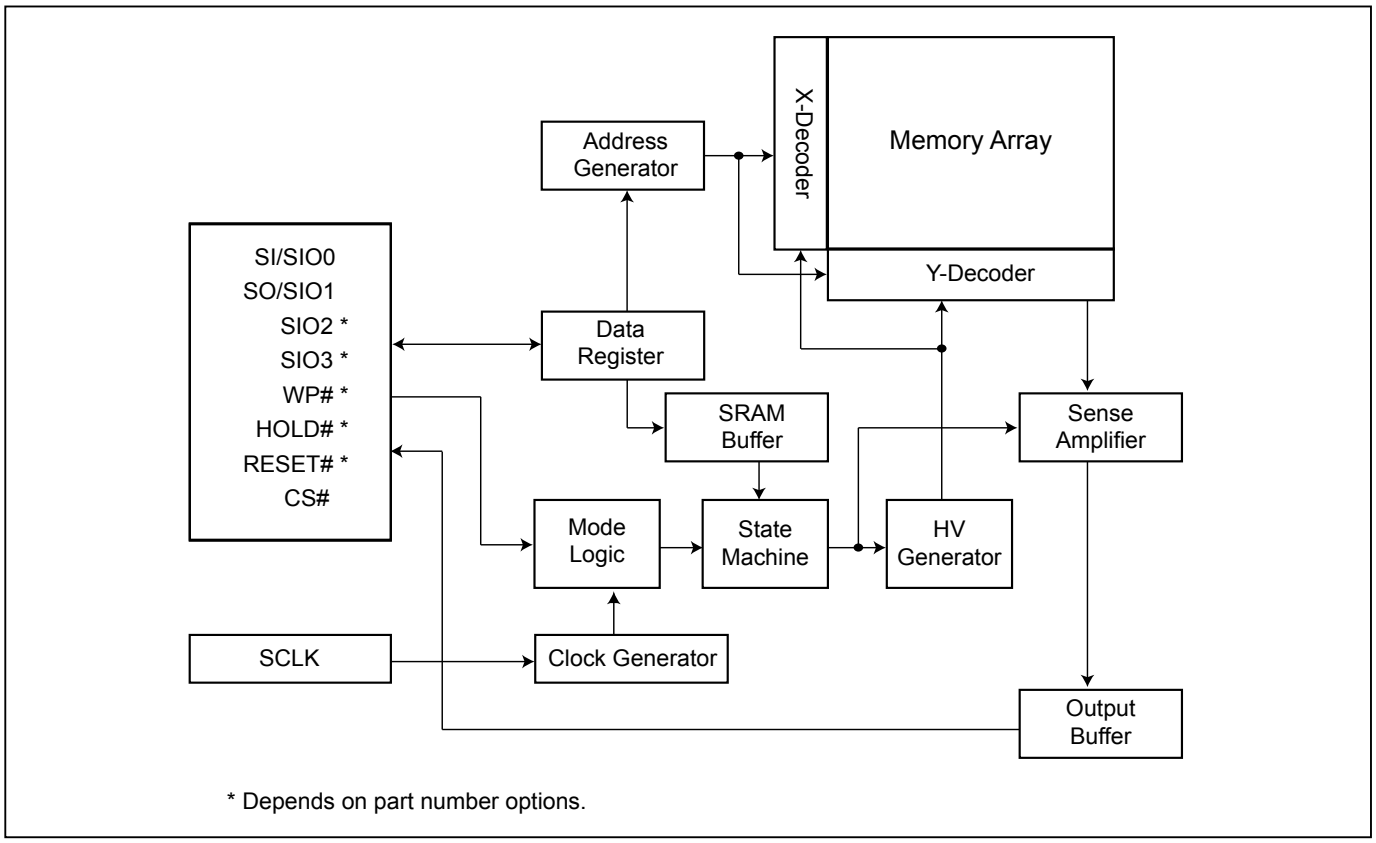
4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
WP#*/SIO2	Write Protection Active Low or Serial Data Input & Output (for 4xI/O read mode)
RESET#*/SIO3	Hardware Reset Pin Active low or Serial Data Input & Output (for 4xI/O read mode)
NC/SIO3	NC or Serial Data Input & Output (for 4xI/O read mode)
RESET#*	Hardware Reset Pin Active low
VCC	+ 3V Power Supply
GND	Ground
NC	No Connection

Notes:

1. The pin of RESET# or WP#/SIO2 will remain internal pull up function while this pin is not physically connected in system configuration. However, the internal pull up function will be disabled if the system has physical connection to RESET# or WP#/SIO2 pin.
2. RESET#/SIO3 pin must be controlled by the system, while it functions as hardware RESET pin.
3. RESET#/SIO3 pin must be connected to VCC (Floating is not allowed), if the system is not using the functions of either 4 x IO or hardware RESET.

5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other commands to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES), and softreset command.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0 and T/B) bits to allow part of memory to be protected as read only. The protected area definition is shown as *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit.
- In four I/O and QPI mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Protected Area Sizes (T/B bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	1Gb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 2047th)
0	0	1	0	2 (2 blocks, protected block 2046th-2047th)
0	0	1	1	3 (4 blocks, protected block 2044th-2047th)
0	1	0	0	4 (8 blocks, protected block 2040th-2047th)
0	1	0	1	5 (16 blocks, protected block 2032nd-2047th)
0	1	1	0	6 (32 blocks, protected block 2016th-2047th)
0	1	1	1	7 (64 blocks, protected block 1984th-2047th)
1	0	0	0	8 (128 blocks, protected block 1920th-2047th)
1	0	0	1	9 (256 blocks, protected block 1792nd-2047th)
1	0	1	0	10 (512 blocks, protected block 1536th-2047th)
1	0	1	1	11 (1024 blocks, protected block 1024th-2047th)
1	1	0	0	12 (2048 blocks, protected all)
1	1	0	1	13 (2048 blocks, protected all)
1	1	1	0	14 (2048 blocks, protected all)
1	1	1	1	15 (2048 blocks, protected all)

Protected Area Sizes (T/B bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	1Gb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 0th)
0	0	1	0	2 (2 blocks, protected block 0th-1st)
0	0	1	1	3 (4 blocks, protected block 0th-3rd)
0	1	0	0	4 (8 blocks, protected block 0th-7th)
0	1	0	1	5 (16 blocks, protected block 0th-15th)
0	1	1	0	6 (32 blocks, protected block 0th-31st)
0	1	1	1	7 (64 blocks, protected block 0th-63rd)
1	0	0	0	8 (128 blocks, protected block 0th-127th)
1	0	0	1	9 (256 blocks, protected block 0th-255th)
1	0	1	0	10 (512 blocks, protected block 0th-511th)
1	0	1	1	11 (1024 blocks, protected block 0th-1023rd)
1	1	0	0	12 (2048 blocks, protected all)
1	1	0	1	13 (2048 blocks, protected all)
1	1	1	0	14 (2048 blocks, protected all)
1	1	1	1	15 (2048 blocks, protected all)

II. Additional 8K-bit secured OTP for an unique identifier to provide an 8K-bit one-time program area for setting a device unique serial number. This may be accomplished in the factory or by an end systems customer.

- Security register bit 0 indicates whether the secured OTP area is locked by factory or not.

- The 8K-bit secured OTP area is programmed by entering secured OTP mode (with the Enter Security OTP command), and going through a normal program procedure. Exiting secured OTP mode is done by issuing the Exit Security OTP command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 12. Security Register Definition"* for security register bit definition and *"Table 3. 8K-bit Secured OTP Definition"* for address range definition.

- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 8K-bit secured OTP mode, array access is not allowed.

Table 3. 8K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000-xxx1FF	4096-bit	Determined by customer	N/A
xxx200-xxx3FF	4096-bit	N/A	Determined by factory

7. Memory Organization

Table 4. Memory Organization

Block(64K-byte)	Block(32K-byte)	Sector	Address Range	
2047	4095	32767	7FFF000h	7FFFFFFh
		⋮	⋮	⋮
		32760	7FF8000h	7FF8FFFh
	4094	32759	7FF7000h	7FF7FFFh
		⋮	⋮	⋮
		32752	7FF0000h	7FF0FFFh
2046	4093	32751	7FEF000h	7FEFFFFh
		⋮	⋮	⋮
		32744	7FE8000h	7FE8FFFh
	4092	32743	7FE7000h	7FE7FFFh
		⋮	⋮	⋮
		32736	7FE0000h	7FE0FFFh
2045	4091	32735	7FDF000h	7FDFFFFh
		⋮	⋮	⋮
		32728	7FD8000h	7FD8FFFh
	4090	32727	7FD7000h	7FD7FFFh
		⋮	⋮	⋮
		32720	7FD0000h	7FD0FFFh
2	5	47	002F000h	002FFFFh
		⋮	⋮	⋮
		40	0028000h	0028FFFh
	4	39	027000h	0027FFFh
		⋮	⋮	⋮
		32	0020000h	0020FFFh
1	3	31	001F000h	001FFFFh
		⋮	⋮	⋮
		24	0018000h	0018FFFh
	2	23	0017000h	0017FFFh
		⋮	⋮	⋮
		16	0010000h	0010FFFh
0	1	15	000F000h	000FFFFh
		⋮	⋮	⋮
		8	0008000h	0008FFFh
	0	7	0007000h	0007FFFh
		⋮	⋮	⋮
		0	0000000h	0000FFFh

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte

individual block lock/unlock unit:64K-byte

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When an incorrect command is written to this device, it enters standby mode and stays in standby mode until the next CS# falling edge. In standby mode, This device's SO pin should be High-Z.

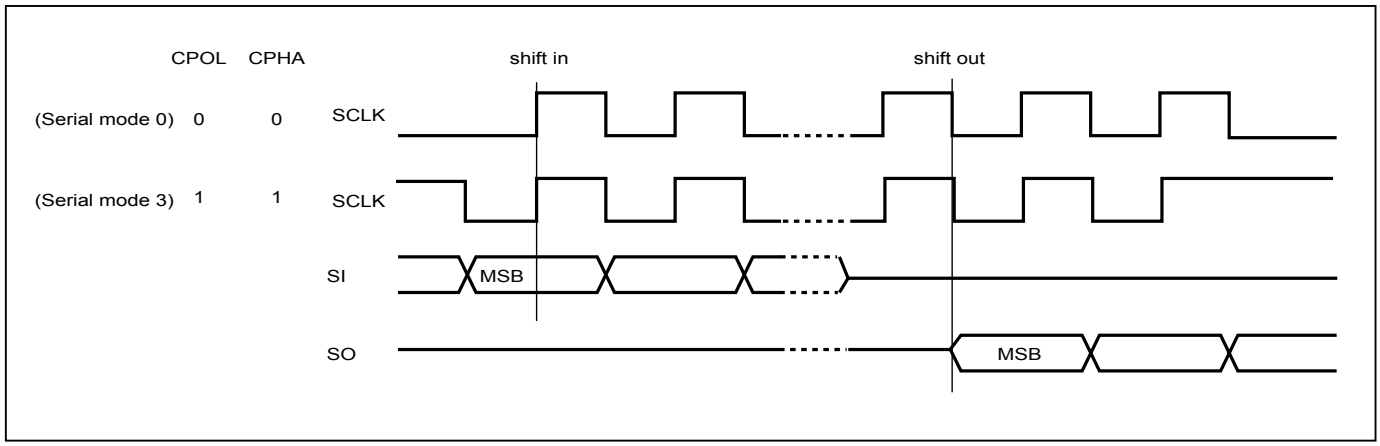
3. When a correct command is written to this device, it enters active mode and stays in active mode until the next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ/READ4B, FAST_READ/FAST_READ4B, 2READ/2READ4B, DREAD/DREAD4B, 4READ/4READ4B, QREAD/QREAD4B, RDSFDP, RES, REMS, QPIID, RDDPB, RDSPB, RDLR, RDEAR, RDCR, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE/SE4B, BE32K/BE32K4B, BE/BE4B, CE, PP/PP4B, 4PP/4PP4B, DP, ENSO, EXSO, WRSCUR, EN4B, EX4B, WPSEL, GBLK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program, or Erase operation is in progress, access to the memory array is ignored and will not affect the current operation of Write Status Register, Program, or Erase.

Figure 1. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing

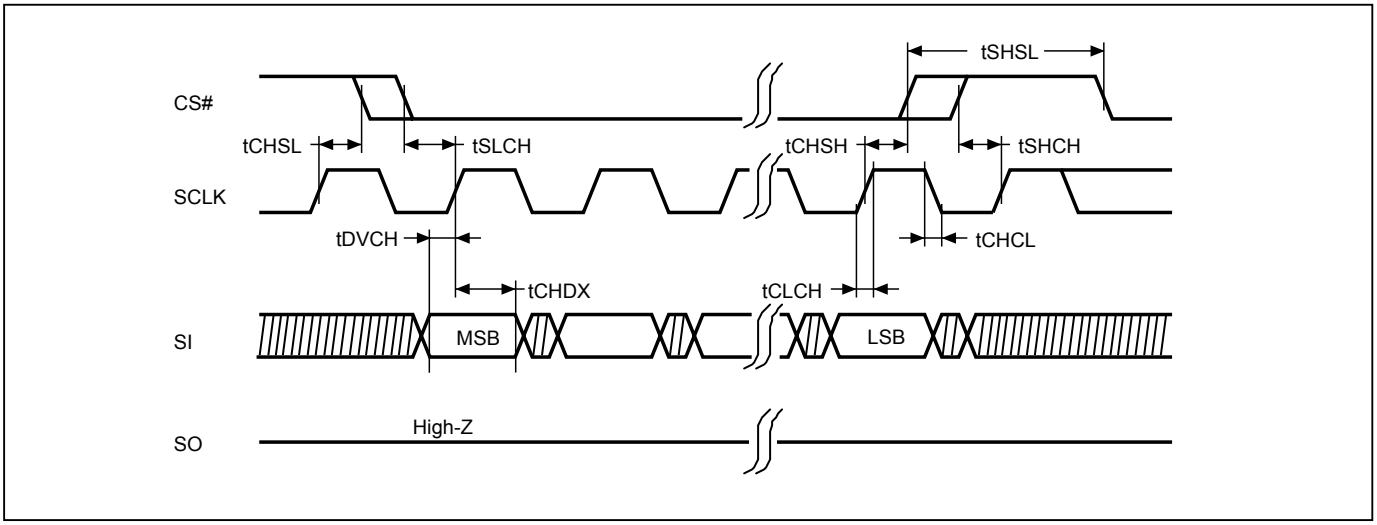


Figure 3. Serial Input Timing (DTR mode)

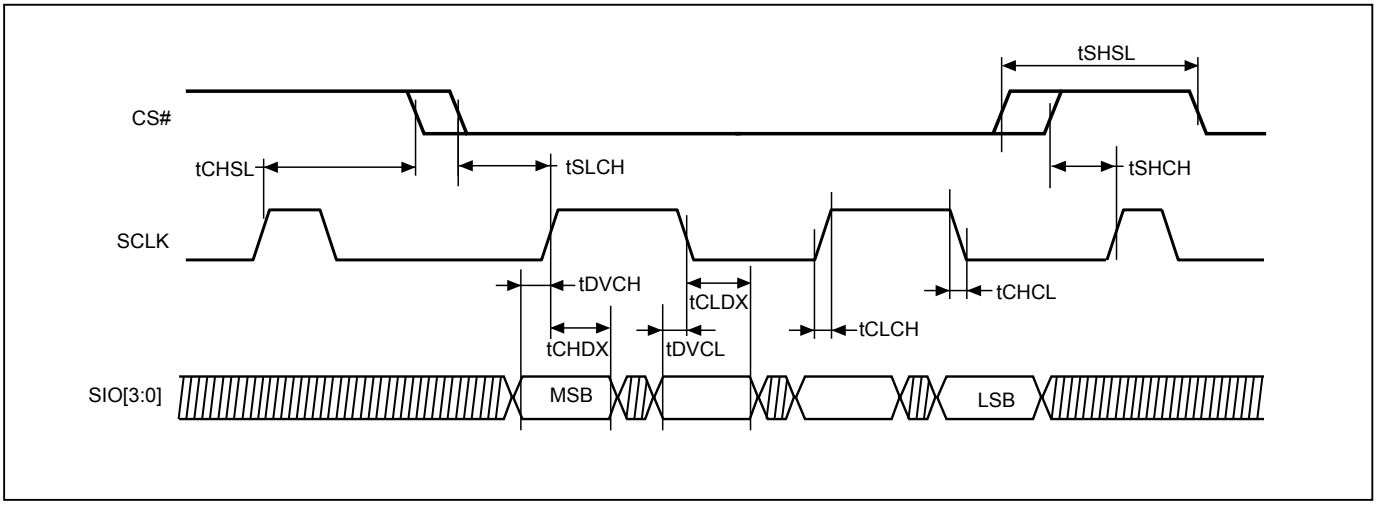


Figure 4. Output Timing (STR mode)

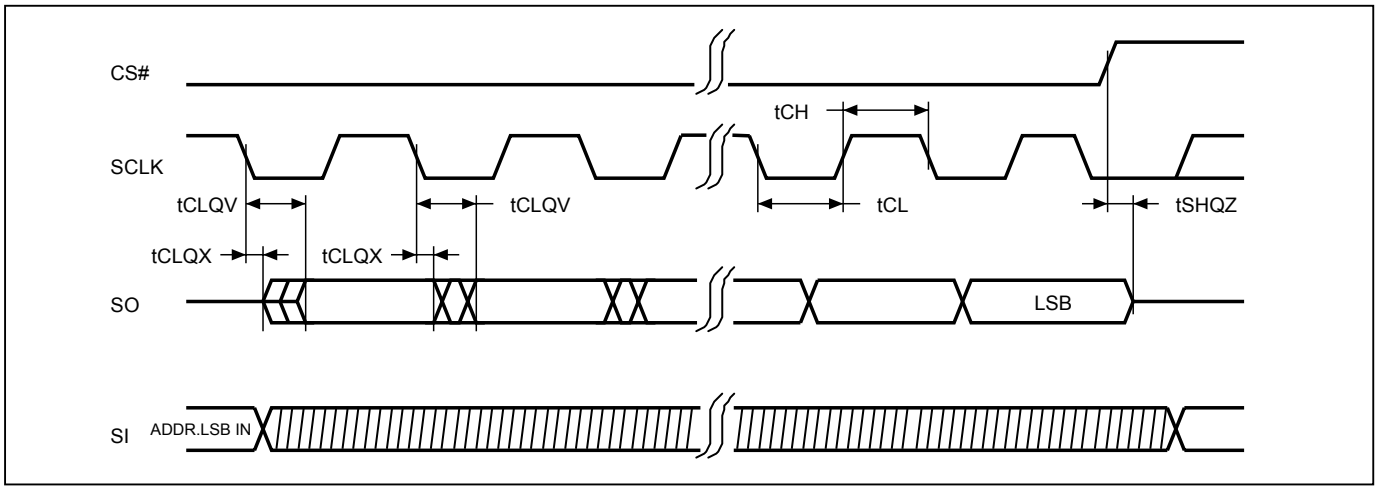
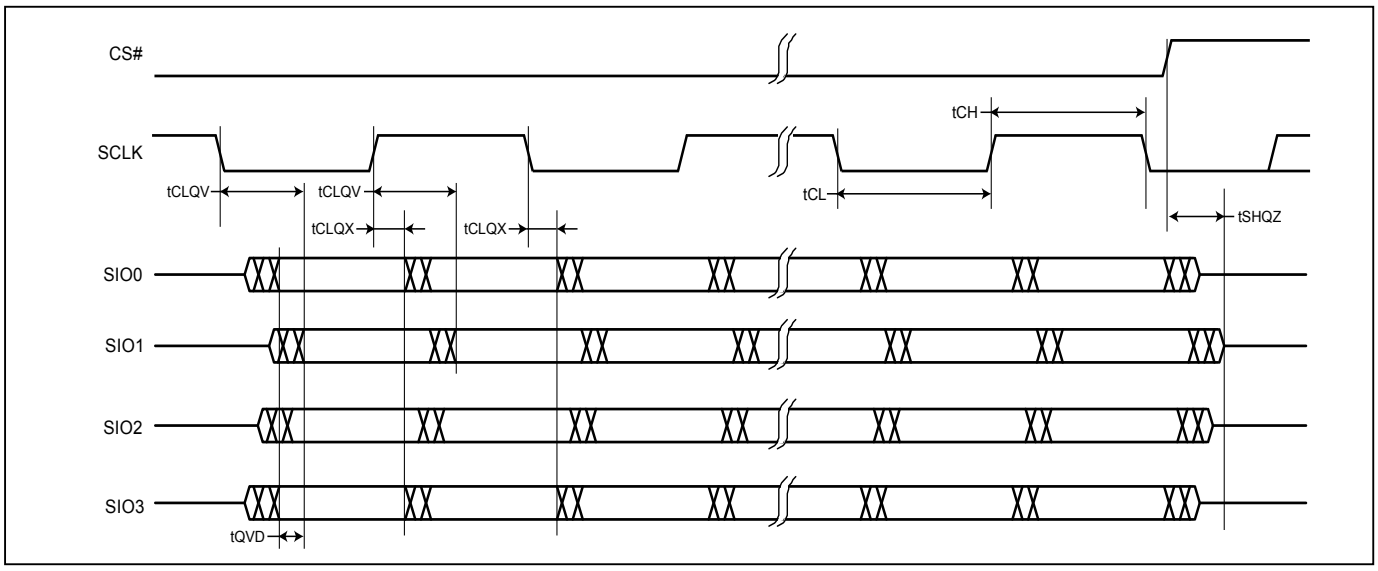


Figure 5. Output Timing (DTR mode)



8-1. 256Mb Address Protocol

The original 24 bit address protocol of Serial NOR Flash can only access density size below 128Mb. For the memory device of 256Mb and above, the 32bit address is requested for access higher memory size. The MX66L1G45J provides three different methods to access the whole density:

(1)Command entry 4-byte address mode: Issue Enter 4-Byte mode command to set up the 4BYTE bit in Configuration Register bit. After 4BYTE bit has been set, the number of address cycle become 32-bit.

(2)Extended Address Register (EAR): configure the memory device into eight 128Mb segments to select which one is active through the EAR<0-2>.

(3)4-byte Address Command Set: When issuing 4-byte address command set, 4-byte address (A31-A0) is requested after the instruction code. Please note that it is not necessary to issue EN4B command before issuing any of 4-byte command set.

Enter 4-Byte Address Mode

In 4-byte Address mode, all instructions are 32-bits address clock cycles. By using EN4B and EX4B to enable and disable the 4-byte address mode.

When 4-byte address mode is enabled, the EAR<0-2> becomes "don't care" for all instructions requiring 4-byte address. The EAR function will be disabled when 4-byte mode is enabled.

Extended Address Register (Configurable)

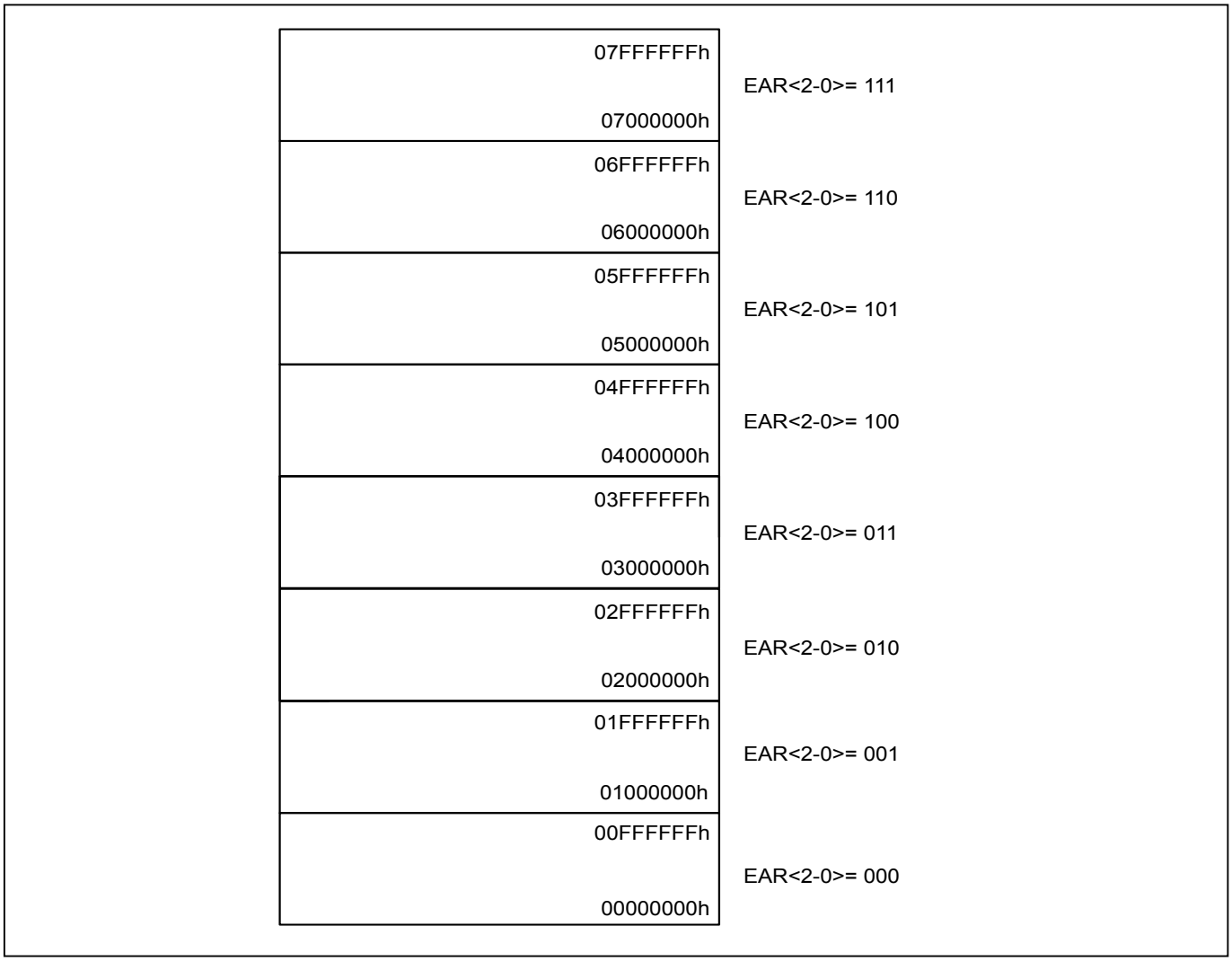
The device provides an 8-bit volatile register for extended Address Register: it identifies the extended address (A31-A24) above 128Mb density by using original 3-byte address.

Extended Address Register (EAR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A31	A30	A29	A28	A27	A26	A25	A24

For the MX66L1G45J the A31 to A27 are Don't Care. During EAR, reading these bits will read as 0. The bit 0 is default as "0".

Figure 6. EAR Operation Segments



When under EAR mode, Read, Program, Erase operates in the selected segment by using 3-byte address mode.

For the read operation, the whole array data can be continually read out with one command. Data output starts from the selected top or bottom 128Mb, but it can cross the boundary. When the last byte of the segment is reached, the next byte (in a continuous reading) is the first byte of the next segment. However, the EAR (Extended Address Register) value does not change. The random access reading can only be operated in the selected segment.

The Chip erase command will erase the whole chip and is not limited by EAR selected segment. However, the sector erase, block erase, program operation are limited in selected segment and will not cross the boundary.

Figure 7. Write EAR Register (WREAR) Sequence (SPI Mode)

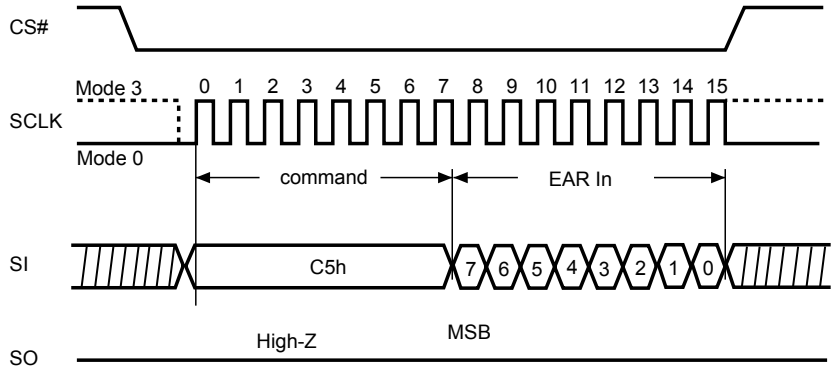


Figure 8. Write EAR Register (WREAR) Sequence (QPI Mode)

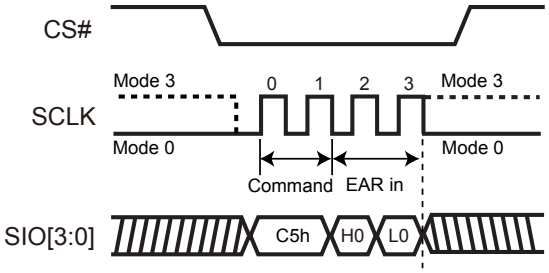


Figure 9. Read EAR (RDEAR) Sequence (SPI Mode)

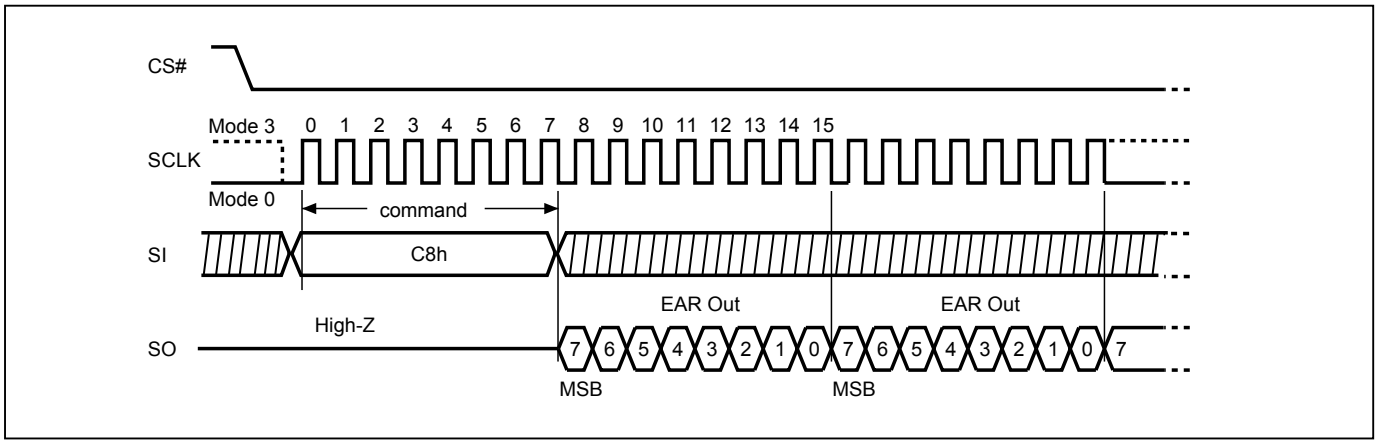
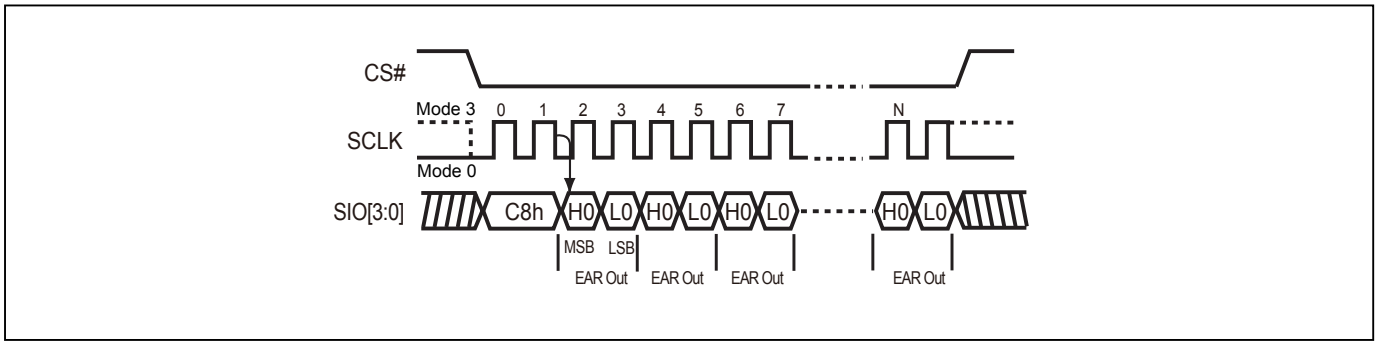


Figure 10. Read EAR (RDEAR) Sequence (QPI Mode)



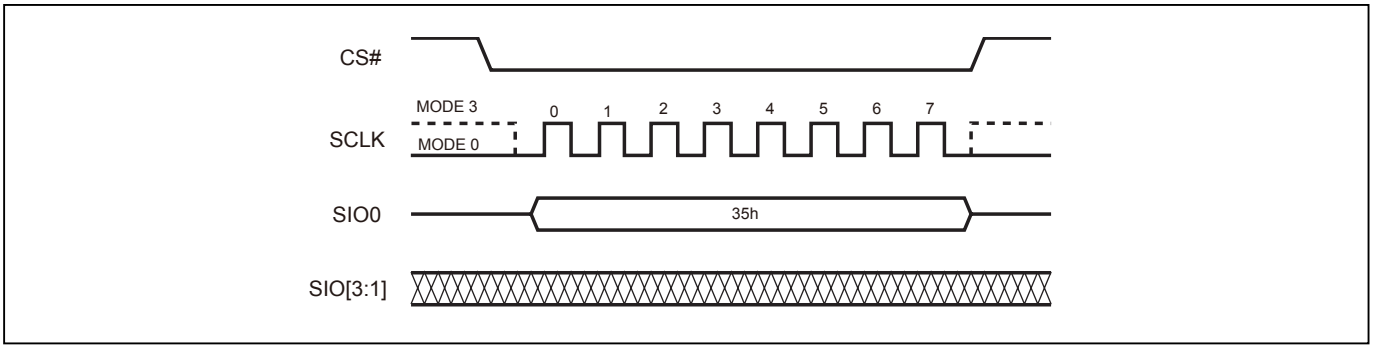
8-2. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial NOR Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing EQIO (35h) command, the QPI mode is enabled. After QPI mode is enabled, the device enters quad mode (4-4-4) without QE bit status changed.

Figure 11. Enable QPI Sequence

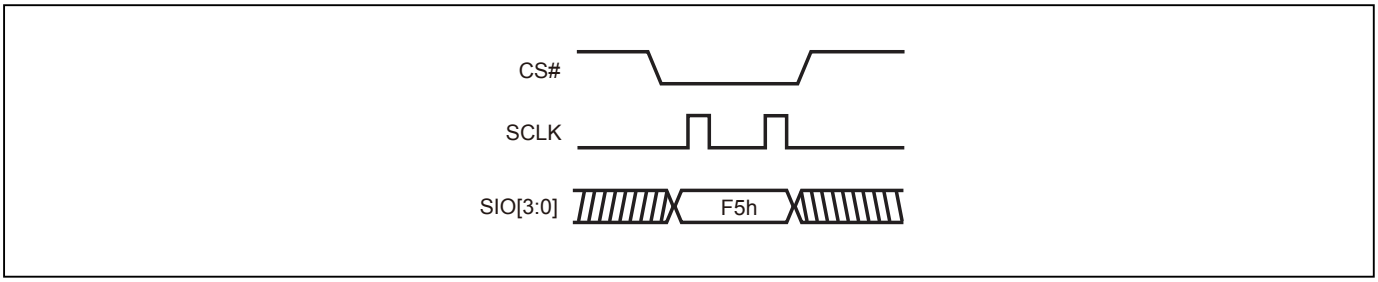


Reset QPI (RSTQIO)

To reset the QPI mode, the RSTQIO (F5h) command is required. After the RSTQIO command is issued, the device returns from QPI mode (4 I/O interface in command cycles) to SPI mode (1 I/O interface in command cycles).

Note:
For EQIO and RSTQIO commands, CS# high width has to follow "From Write/Erase/Program to Read Status Register" tSHSL specification for next instruction, as defined in *"Table 26. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 2.7V - 3.6V)"*.

Figure 12. Reset QPI Mode



9. COMMAND DESCRIPTION

Table 5. Command Set

	Command Code	SPI	QPI	Address Byte					Dummy Cycle	Data Byte
				Total ADD Byte	Byte 1	Byte 2	Byte 3	Byte 4		
Array access										
READ (normal read)	03 (hex)	V		3/4	A[23:16]	A[15:8]	A[7:0]		0	1- ∞
FAST READ (fast read data)	0B (hex)	V		3/4	A[23:16]	A[15:8]	A[7:0]		8 *	1- ∞
2READ (2 x I/O read command)	BB (hex)	V		3/4	A[23:16]	A[15:8]	A[7:0]		4 *	1- ∞
DREAD (1I 2O read)	3B (hex)	V		3/4	A[23:16]	A[15:8]	A[7:0]		8 *	1- ∞
4READ (4 I/O read)	EB (hex)	V	V	3/4	A[23:16]	A[15:8]	A[7:0]		6 *	1- ∞
QREAD (1I 4O read)	6B (hex)	V		3/4	A[23:16]	A[15:8]	A[7:0]		8 *	1- ∞
4DTRD (Quad I/O DT Read)	ED (hex)	V	V	3/4	A[23:16]	A[15:8]	A[7:0]		6 *	1- ∞
PP (page program)	02 (hex)	V	V	3/4	A[23:16]	A[15:8]	A[7:0]		0	1-256
4PP (quad page program)	38 (hex)	V		3/4	A[23:16]	A[15:8]	A[7:0]		0	1-256
SE (sector erase)	20 (hex)	V	V	3/4	A[23:16]	A[15:8]	A[7:0]		0	0
BE 32K (block erase 32KB)	52 (hex)	V	V	3/4	A[23:16]	A[15:8]	A[7:0]		0	0
BE (block erase 64KB)	D8 (hex)	V	V	3/4	A[23:16]	A[15:8]	A[7:0]		0	0
CE (chip erase)	60 or C7 (hex)	V	V	0					0	0
Read/Write Array Commands (4 Byte Address Command Set)										
READ4B (read data byte by 4 byte address)	13 (hex)	V		4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	1- ∞
FAST READ4B (read data byte by 4 byte address)	0C (hex)	V		4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	8 *	1- ∞
2READ4B (read data byte by 2 x I/O with 4 byte address)	BC (hex)	V		4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	4 *	1- ∞
DREAD4B (Read data byte by Dual Output with 4 byte address)	3C (hex)	V		4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	8 *	1- ∞
4READ4B (read data byte by 4 x I/O with 4 byte address)	EC (hex)	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	6 *	1- ∞
QREAD4B (Read data byte by Quad Output with 4 byte address)	6C (hex)	V		4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	8 *	1- ∞
4DTRD4B (Quad I/O DT Read)	EE (hex)	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	6 *	1- ∞

* Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

	Command Code	SPI	QPI	Address Byte					Dummy Cycle	Data Byte
				Total ADD Byte	Byte 1	Byte 2	Byte 3	Byte 4		
PP4B (to program the selected page with 4byte address)	12 (hex)	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	1-256
4PP4B (Quad input to program the selected page with 4byte address)	3E (hex)	V		4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	1-256
SE4B (Sector erase 4KB)	21 (hex)	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	0
BE32K4B (block erase 32KB)	5C (hex)	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	0
BE4B (block erase 64KB)	DC (hex)	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	0
Device operation										
WREN (write enable)	06 (hex)	V	V	0					0	0
WRDI (write disable)	04 (hex)	V	V	0					0	0
WPSEL (Write Protect Selection)	68 (hex)	V		0					0	0
EQIO (Enable QPI)	35 (hex)	V		0					0	0
RSTQIO (Reset QPI)	F5 (hex)		V	0					0	0
EN4B (enter 4-byte mode)	B7 (hex)	V	V	0					0	0
EX4B (exit 4-byte mode)	E9 (hex)	V	V	0					0	0
PGM/ERS Suspend (Suspends Program/ Erase)	B0 (hex)	V	V	0					0	0
PGM/ERS Resume (Resumes Program/ Erase)	30 (hex)	V	V	0					0	0
DP (Deep power down)	B9 (hex)	V	V	0					0	0
RDP (Release from deep power down)	AB (hex)	V	V	0					0	0
NOP (No Operation)	00 (hex)	V	V	0					0	0
RSTEN (Reset Enable)	66 (hex) *(Note2)*	V	V	0					0	0
RST (Reset Memory)	99 (hex) *(Note2)*	V	V	0					0	0
GBLK (gang block lock)	7E (hex)	V		0					0	0
GBULK (gang block unlock)	98 (hex)	V		0					0	0
FMEN (factory mode enable)	41 (hex)	V	V	0					0	0

	Command Code	SPI	QPI	Address Byte					Dummy Cycle	Data Byte
				Total ADD Byte	Byte 1	Byte 2	Byte 3	Byte 4		
Register Access										
RDID (read identification)	9F (hex)	V		0					0	3
RES (read electronic ID)	AB (hex)	V	V	0					24	1
REMS (read electronic manufacturer & device ID)	90 (hex)	V		1			ADD		16	1
QPIID (QPI ID Read)	AF (hex)		V	0					0	3
RDSFDP (Read SFDP Table)	5A (hex)	V		3	A[23:16]	A[15:8]	A[7:0]		8	1- ∞
RDSR (read status register)	05 (hex)	V	V	0					0	1
RDCR (read configuration register)	15 (hex)	V	V	0					0	1
WRSR (write status/configuration register)	01 (hex)	V	V	0					0	1-2
RDEAR (read extended address register)	C8 (hex)	V	V	0					0	0
WREAR (write extended address register)	C5 (hex)	V	V	0					0	1
RDSCUR (read security register)	2B (hex)	V	V	0					0	1
WRSCUR (write security register)	2F (hex)	V	V	0					0	0
SBL (Set Burst Length)	C0 (hex)	V	V	0					0	1
ENSO (enter secured OTP)	B1 (hex)	V	V	0					0	0
EXSO (exit secured OTP)	C1 (hex)	V	V	0					0	0
WRLR (write Lock register)	2C (hex)	V		0					0	2
RDLR (read Lock register)	2D (hex)	V		0					0	2
WRSPB (SPB bit program)	E3 (hex)	V		4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	0
ESSPB (all SPB bit erase)	E4 (hex)	V		0					0	0
RDSPB (read SPB status)	E2 (hex)	V		4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	1
WRDPB (write DPB register)	E1 (hex)	V		4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	1
RDDPB (read DPB register)	E0 (hex)	V		4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	1

Note 1: It is not recommended to adopt any other code/address not in the command definition table, which will potentially enter the hidden mode.

Note 2: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.

9-1. Write Enable (WREN)

The Write Enable (WREN) instruction sets the Write Enable Latch (WEL) bit. Instructions like PP/PP4B, 4PP/4PP4B, SE/SE4B, BE32K/BE32K4B, BE/BE4B, CE, and WRSR that are intended to change the device content, should be preceded by the WREN instruction.

The sequence of issuing WREN instruction is: CS# goes low→send WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care in SPI mode.

Figure 13. Write Enable (WREN) Sequence (SPI Mode)

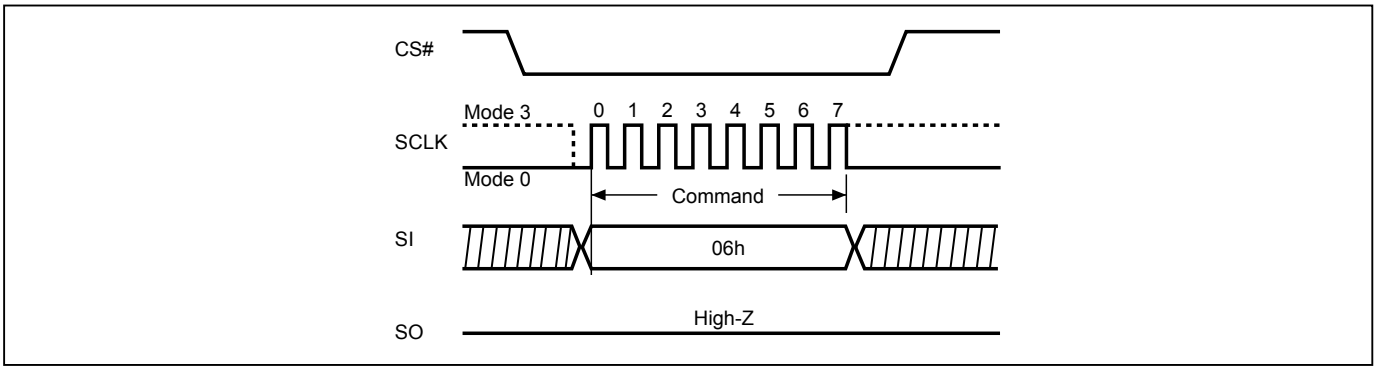
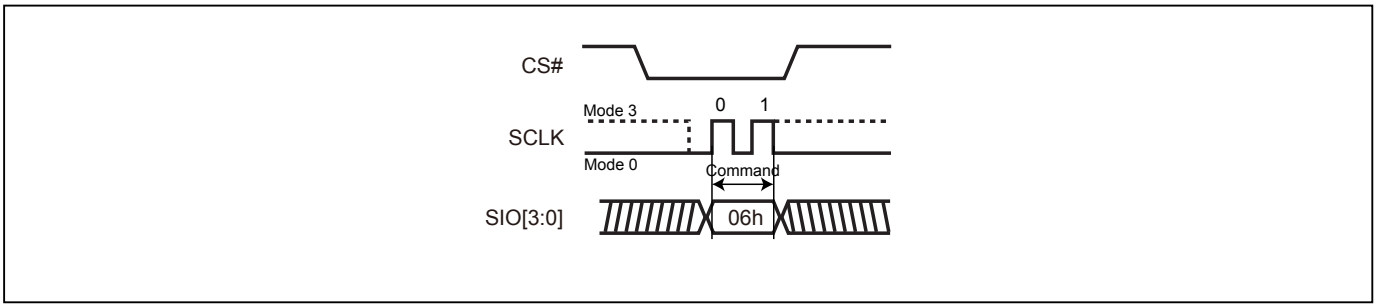


Figure 14. Write Enable (WREN) Sequence (QPI Mode)



9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction resets the Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→send WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care in SPI mode.

The WEL bit is reset in the following situations:

- Power-up
- RESET# pin driven low
- WRDI command completion
- WRSR command completion
- PP/PP4B command completion
- 4PP/4PP4B command completion
- SE/SE4B command completion
- BE32K/BE32K4B command completion
- BE/BE4B command completion
- CE command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion
- WPSEL command completion
- GBLK command completion
- GBULK command completion
- WREAR command completion
- WRLR command completion
- WRSPB command completion
- WRDPB command completion
- ESSPB command completion

Figure 15. Write Disable (WRDI) Sequence (SPI Mode)

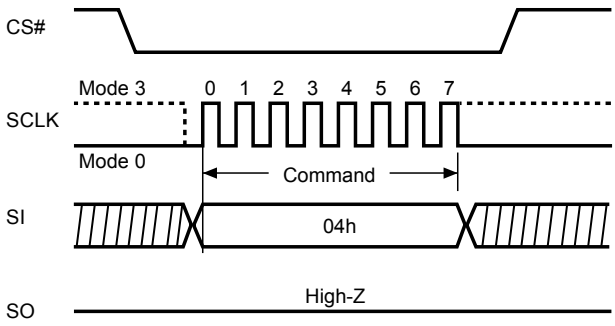
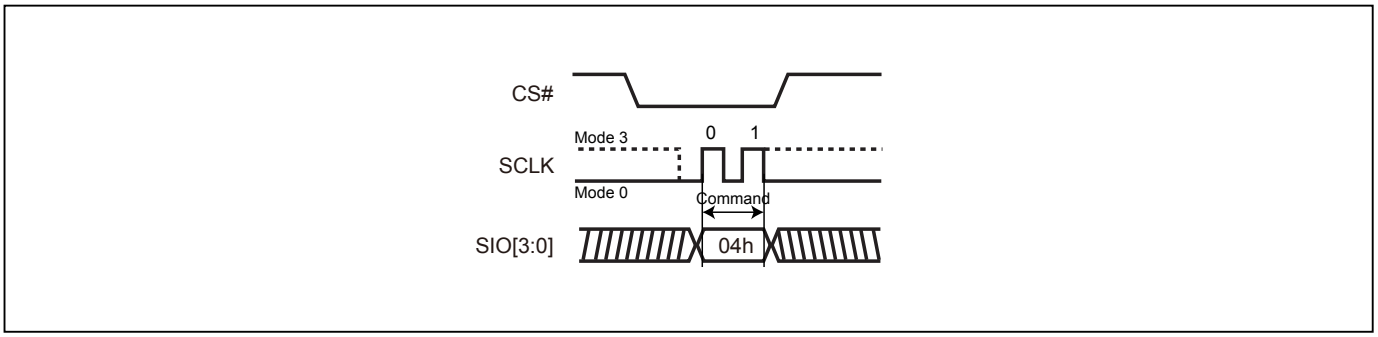


Figure 16. Write Disable (WRDI) Sequence (QPI Mode)



9-3. Factory Mode Enable (FMEN)

The Factory Mode Enable (FMEN) instruction enhances Program and Erase performance for increase factory production throughput. The FMEN instruction needs to combine with the instructions which are intended to change the device content, like PP/PP4B, 4PP/4PP4B, SE/SE4B, BE32K/BE32K4B, BE/BE4B, and CE.

The sequence of issuing FMEN instruction is: CS# goes low→send FMEN instruction code→ CS# goes high. A valid factory mode operation needs to be included three sequences: WREN instruction → FMEN instruction→ Program or Erase instruction.

Suspend command is not acceptable under factory mode.

The FMEN is reset in the following situations

- Power-up
- Reset# pin driven low
- PP/PP4B command completion
- 4PP/4PP4B command completion
- SE/SE4B command completion
- BE32K/BE32K4B command completion
- BE/BE4B command completion
- CE command completion
- Softreset command completion

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care in SPI mode.

Figure 17. Factory Mode Enable (FMEN) Sequence (SPI Mode)

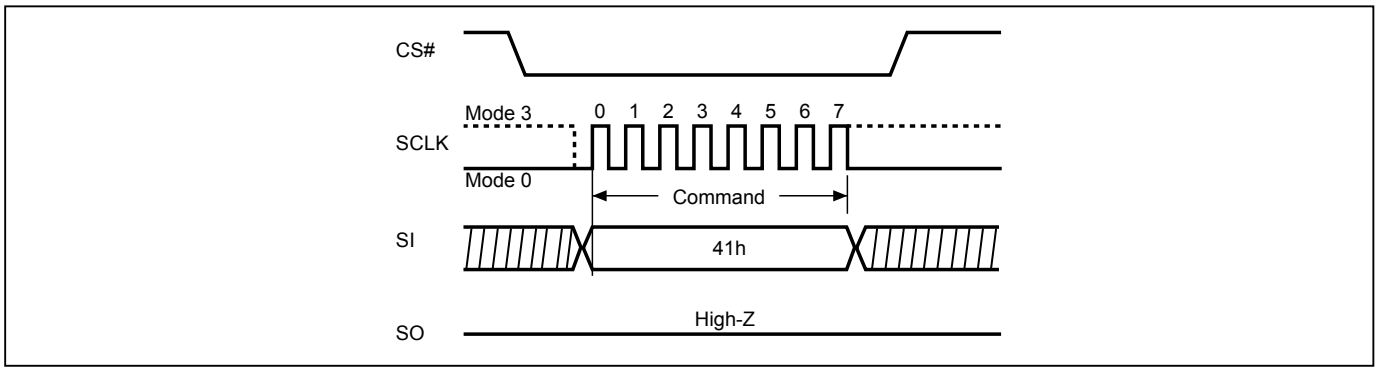
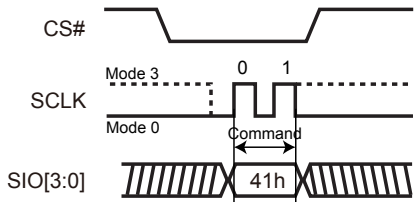


Figure 18. Factory Mode Enable (FMEN) Sequence (QPI Mode)



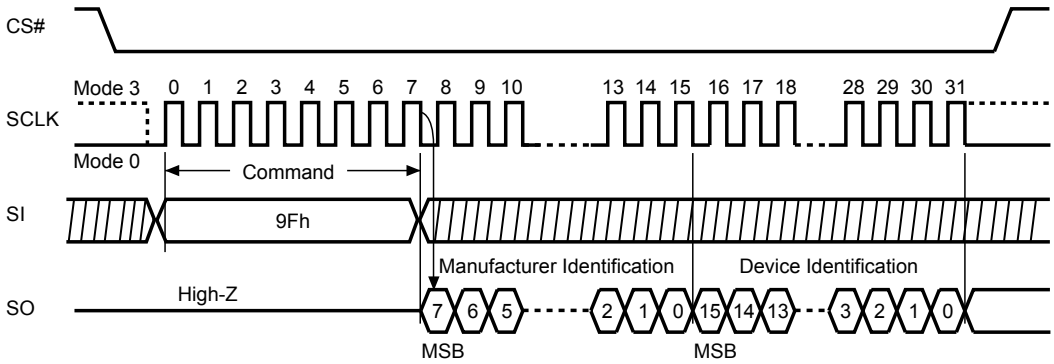
9-4. Read Identification (RDID)

The RDID instruction is for reading the 1-byte manufacturer ID and the 2-byte Device ID that follows. The Macronix Manufacturer ID and Device ID are listed as *Table 6* ID Definitions.

The sequence of issuing RDID instruction is: CS# goes low→ send RDID instruction code→24-bits ID data out on SO→ to end RDID operation, drive CS# high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 19. Read Identification (RDID) Sequence (SPI mode only)



9-5. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max), as specified in *"Table 26. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 2.7V - 3.6V)"*. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode. Reset# pin goes low will release the Flash from deep power down mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature ID, whose values are shown as *"Table 6. ID Definitions"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

The RDP and RES are allowed to execute in Deep power-down mode, except if the device is in progress of program/erase/write cycle; In this case, there is no effect on the current program/erase/write cycle that is in progress.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The RES instruction ends when CS# goes high, after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

Figure 20. Read Electronic Signature (RES) Sequence (SPI Mode)

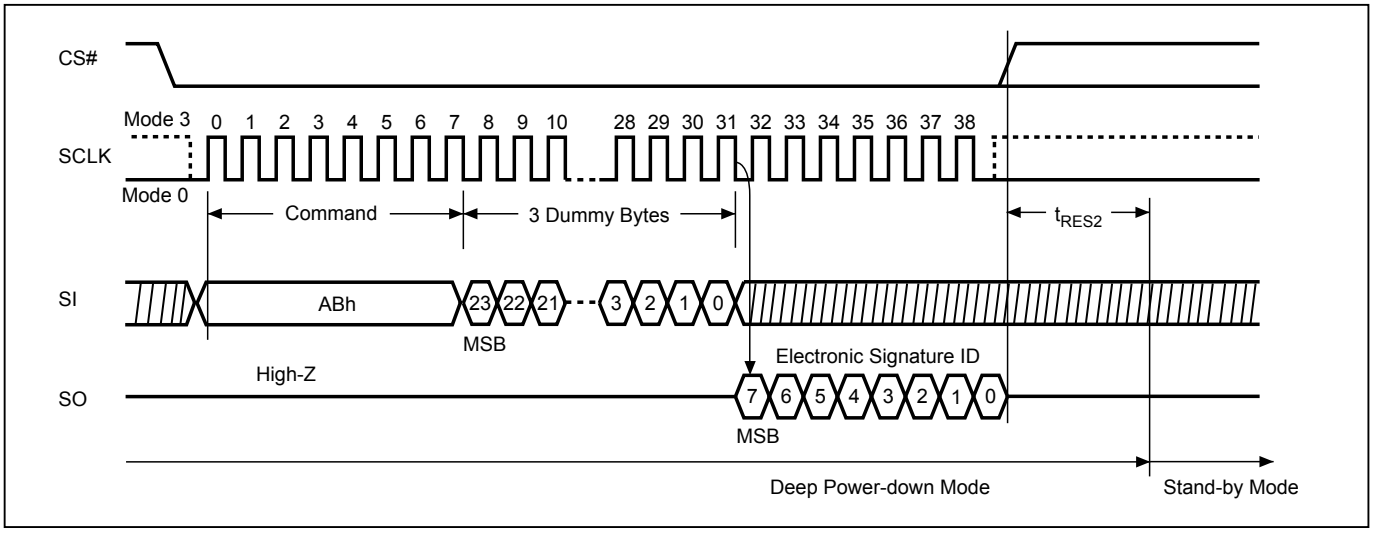


Figure 21. Read Electronic Signature (RES) Sequence (QPI Mode)

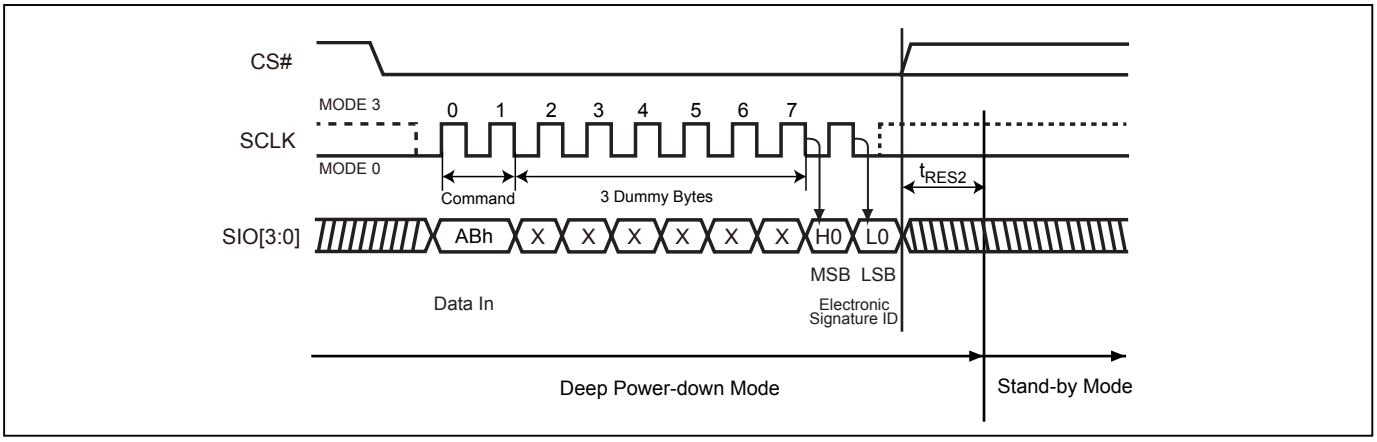


Figure 22. Release from Deep Power-down (RDP) Sequence (SPI Mode)

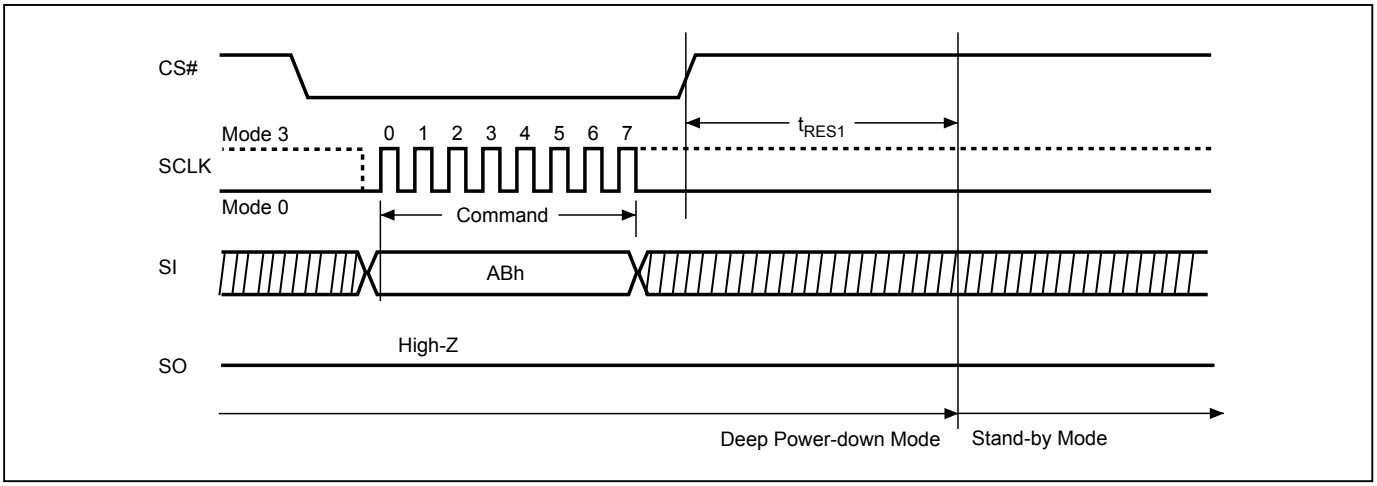
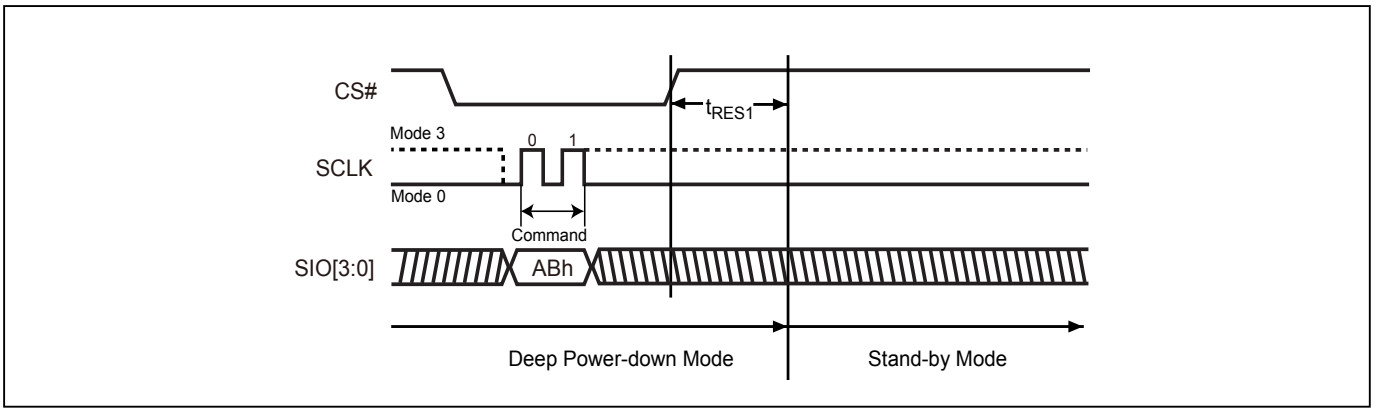


Figure 23. Release from Deep Power-down (RDP) Sequence (QPI Mode)

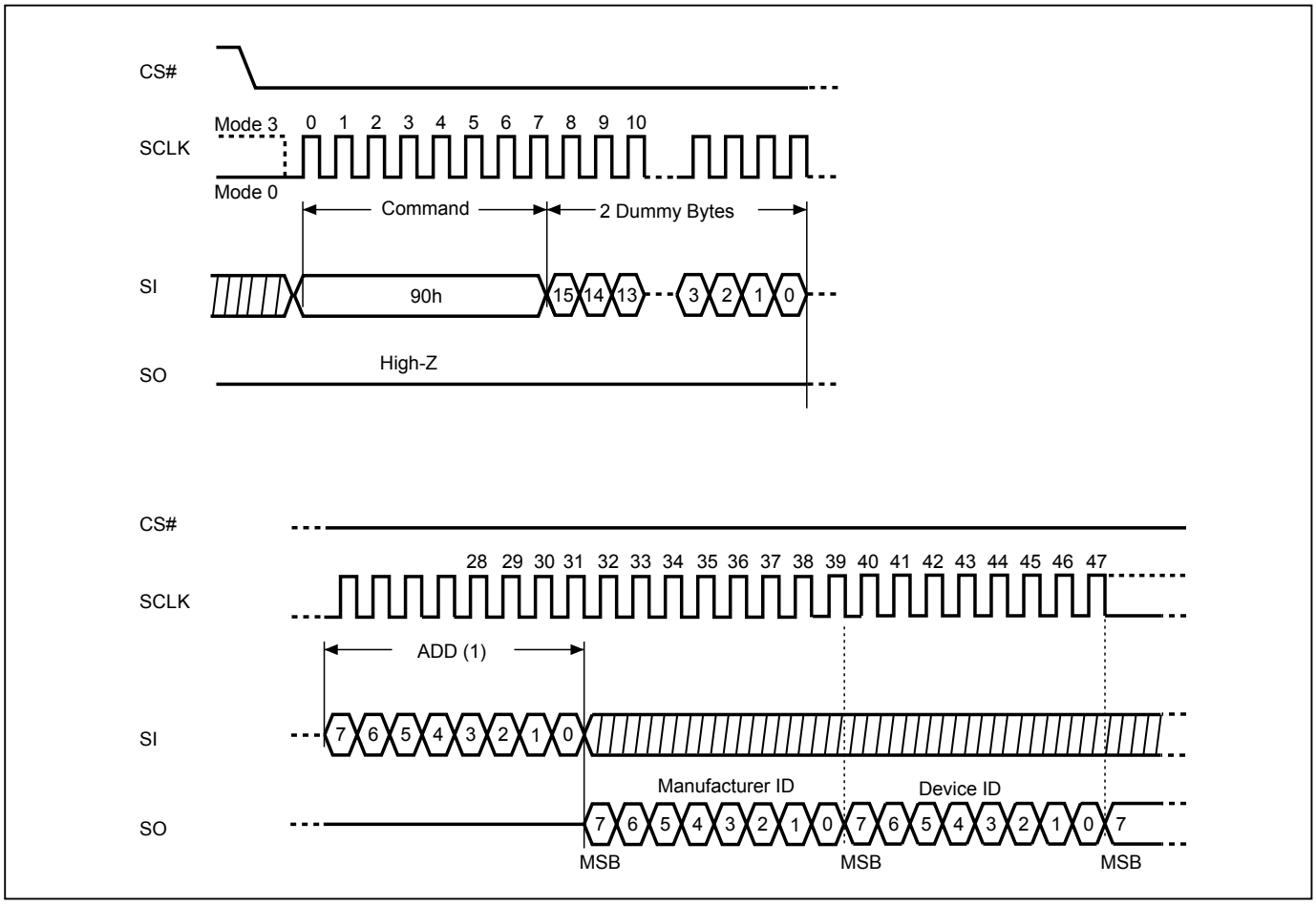


9-6. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in *"Table 6. ID Definitions"*.

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7-A0). After which the manufacturer ID for Macronix (C2h) and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 24. Read Electronic Manufacturer & Device ID (REMS) Sequence (SPI Mode only)



Notes: (1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

9-7. QPI ID Read (QPIID)

The QPIID Read instruction can be used to identify the Device ID and Manufacturer ID. The sequence of issuing the QPIID instruction is as follows: CS# goes low→send QPI ID instruction→Data out on SO→CS# goes high. Most significant bit (MSB) first.

After the command cycle, the device will immediately output data on the falling edge of SCLK. The manufacturer ID, memory type, and memory density data byte will be output continuously, until the CS# goes high.

Table 6. ID Definitions

Command Type		MX66L1G45J		
RDID	9Fh	Manufacturer ID	Memory Type	Memory Density
		C2	20	1B
RES	ABh	Electronic Signature ID		
		1A		
REMS	90h	Manufacturer ID	Device ID	
		C2	1A	
QPIID	AFh	Manufacturer ID	Memory Type	Memory Density
		C2	20	1B

9-8. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ send RDSR instruction code→ Status Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Figure 25. Read Status Register (RDSR) Sequence (SPI Mode)

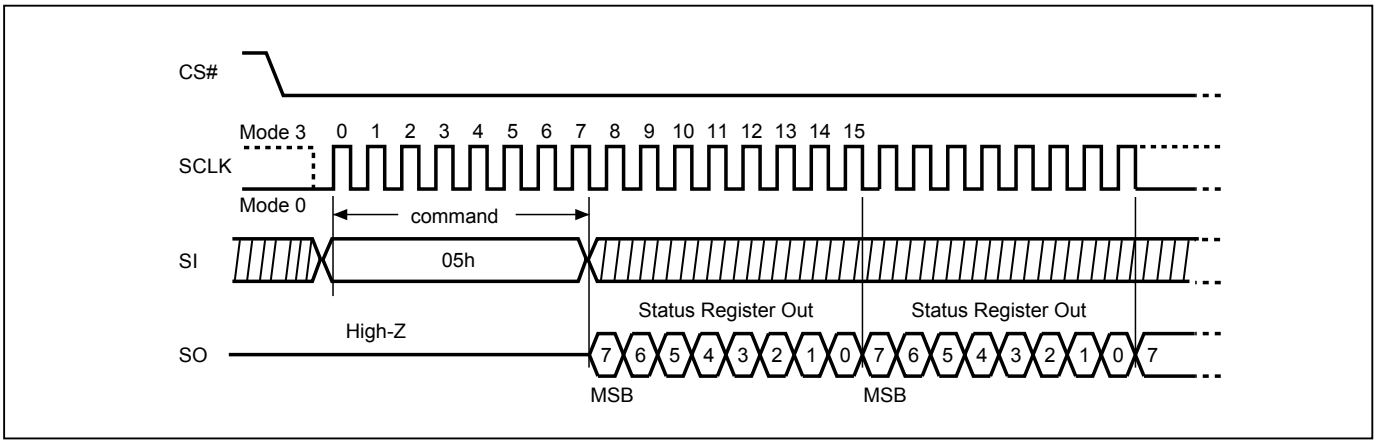
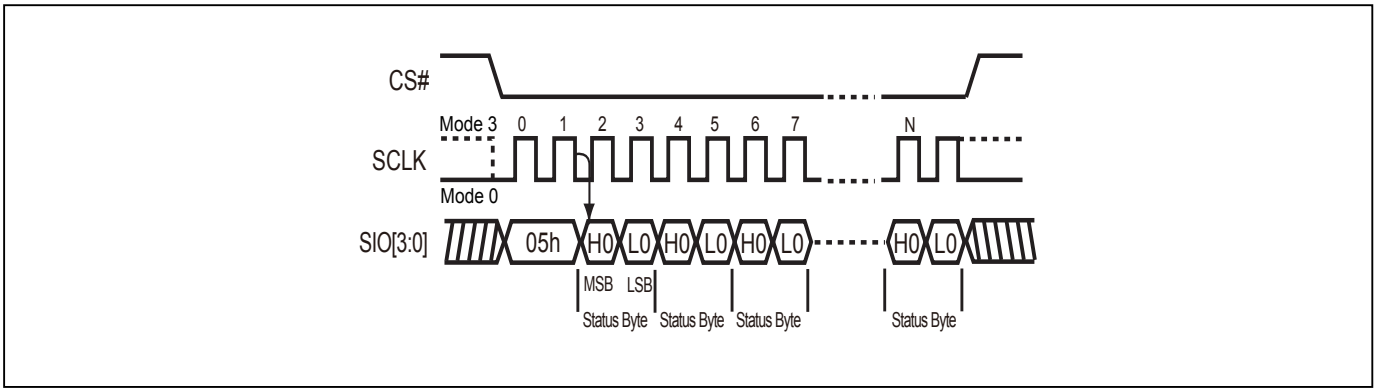


Figure 26. Read Status Register (RDSR) Sequence (QPI Mode)



9-9. Read Configuration Register (RDCR)

The RDCR instruction is for reading Configuration Register Bits. The Read Configuration Register can be read at any time (even in program/erase/write configuration register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write configuration register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ send RDCR instruction code→ Configuration Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Figure 27. Read Configuration Register (RDCR) Sequence (SPI Mode)

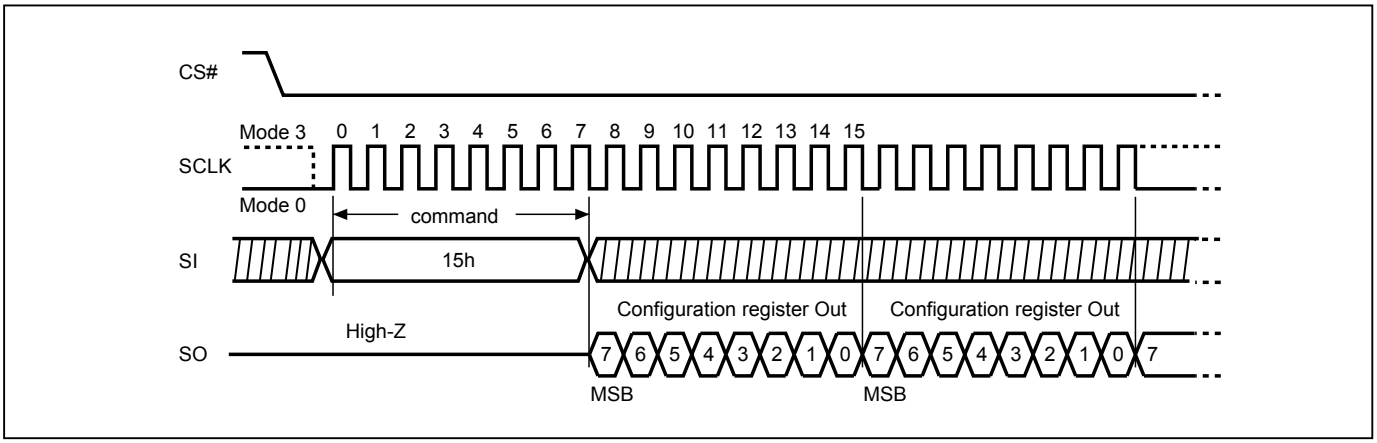
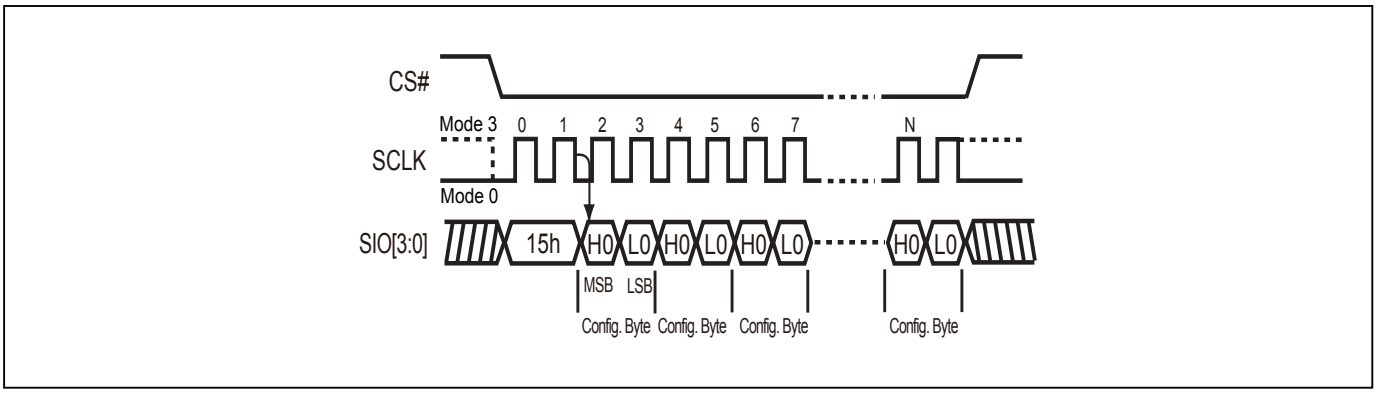


Figure 28. Read Configuration Register (RDCR) Sequence (QPI Mode)



For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 29. Program/Erase flow with read array data

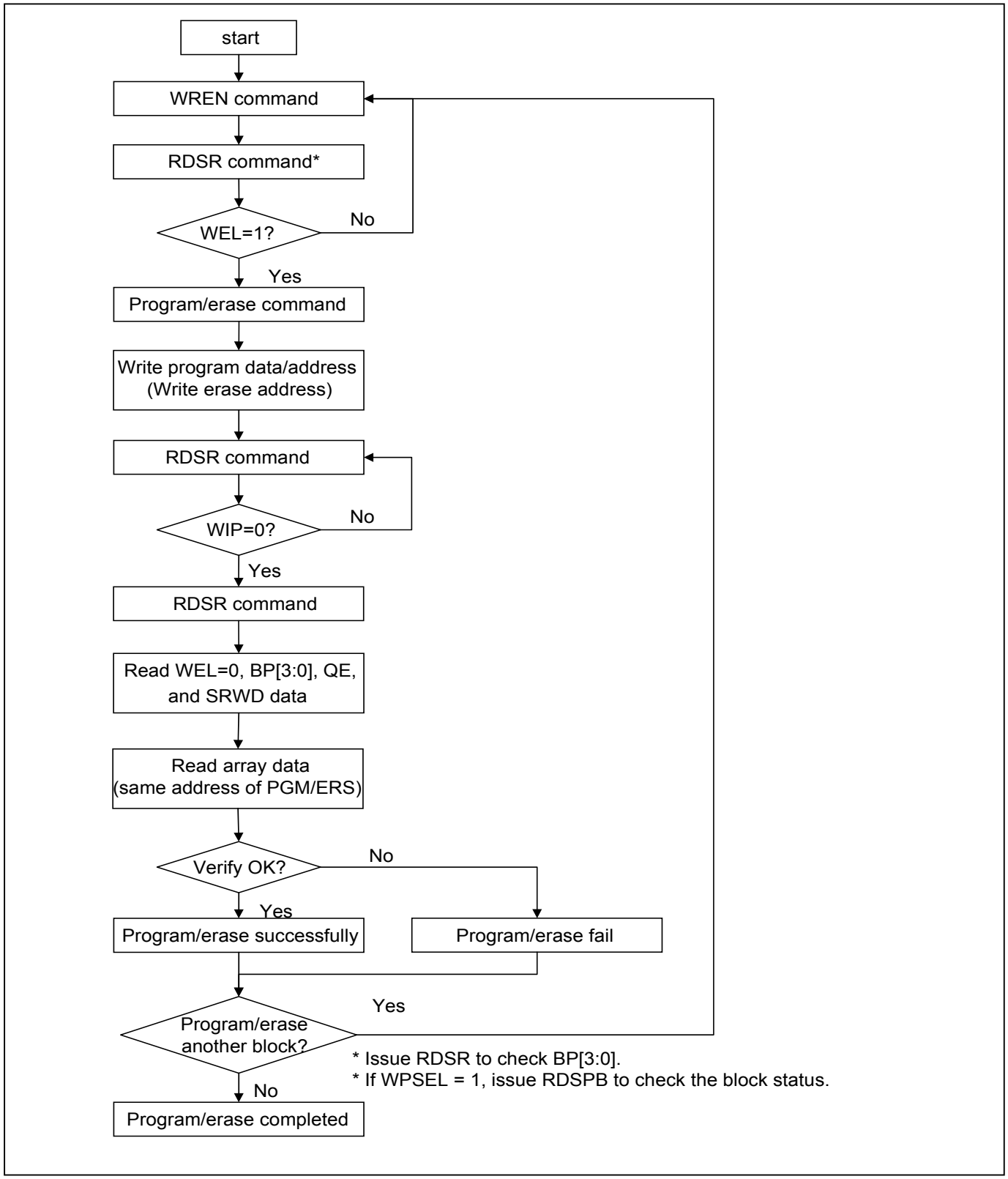
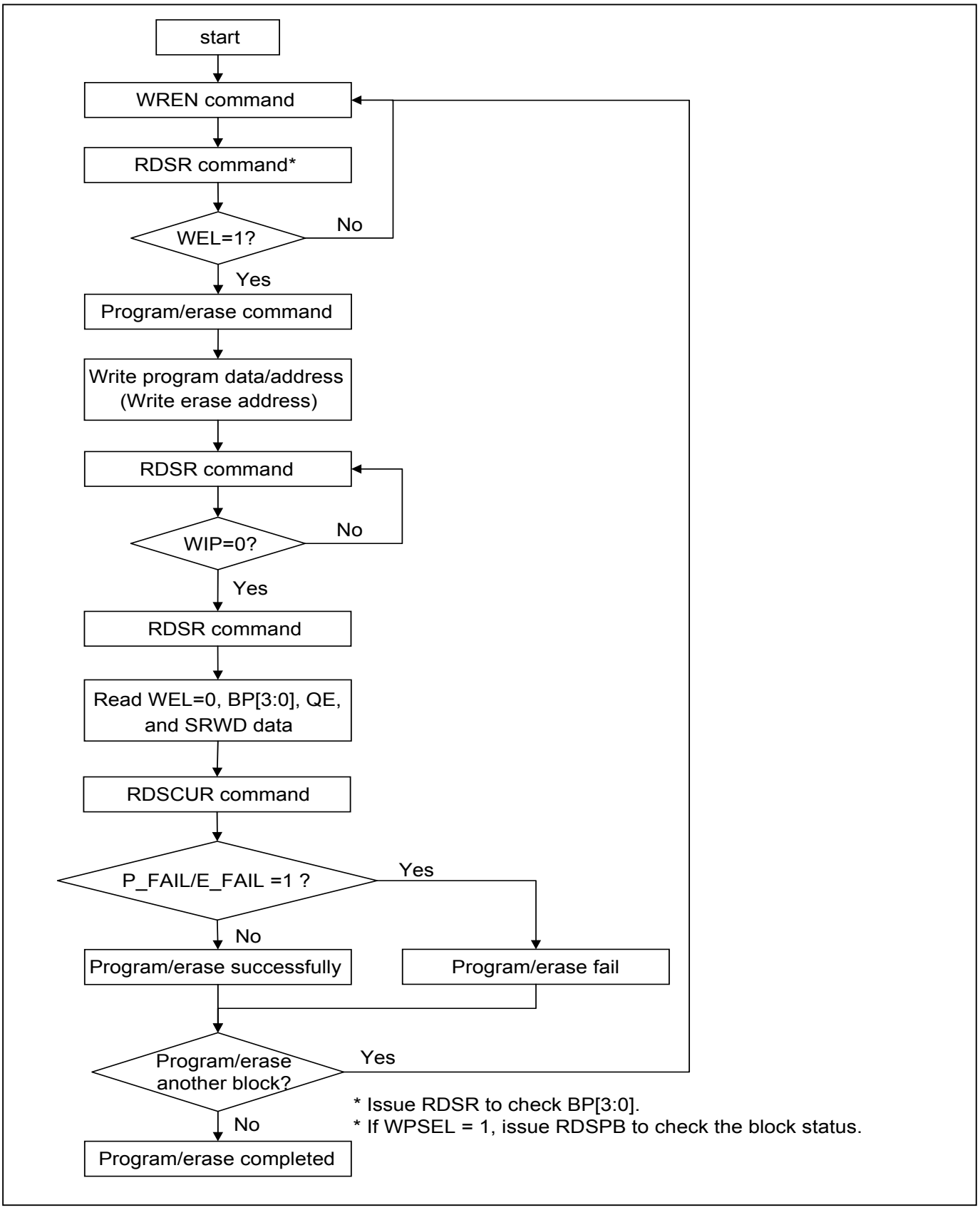


Figure 30. Program/Erase flow without read array data (read P_FAIL/E_FAIL flag)



Status Register

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit is a volatile bit that is set to "1" by the WREN instruction. WEL needs to be set to "1" before the device can accept program and erase instructions, otherwise the program and erase instructions are ignored. WEL automatically clears to "0" when a program or erase operation completes. To ensure that both WIP and WEL are "0" and the device is ready for the next program or erase operation, it is recommended that WIP be confirmed to be "0" before checking that WEL is also "0" (Please refer to *"Figure 33. WRSR flow"*). If a program or erase instruction is applied to a protected memory area, the instruction will be ignored and WEL will clear to "0".

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 2. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

QE bit. The Quad Enable (QE) bit is a non-volatile bit with a factory default of "0". When QE is "0", Quad mode commands are ignored; pins WP#/SIO2, RESET#/SIO3 (of 8-pin package) and NC/SIO3 function as WP#, RESET# and NC, respectively. When QE is "1", Quad mode is enabled and Quad mode commands are supported along with Single and Dual mode commands. Pins WP#/SIO2, RESET#/SIO3 (of 8-pin package) and NC/SIO3 function as SIO2 and SIO3, respectively, and their alternate pin functions are disabled. Enabling Quad mode also disables the HPM and RESET features.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Table 7. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disabled 0=status register write enabled	1=Quad Enabled 0=not Quad Enabled	*(note 1)*	*(note 1)*	*(note 1)*	*(note 1)*	1=write enabled 0=not write enabled	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: Please refer to the *"Table 2. Protected Area Sizes"*.

Configuration Register

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

ODS bit
The output driver strength (ODS2, ODS1, ODS0) bits are volatile bits, which indicate the output driver level (as defined in *"Table 9. Output Driver Strength Table"*) of the device. The Output Driver Strength is defaulted as 75% when delivered from factory. To write the ODS bits requires the Write Status Register (WRSR) instruction to be executed.

TB bit
The Top/Bottom (TB) bit is a non-volatile OTP bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as “0”, which means Top area protect. When it is set as “1”, the protect area will change to Bottom area of the memory device. To write the TB bits requires the Write Status Register (WRSR) instruction to be executed.

PBE bit
The Preamble Bit Enable (PBE) bit is a volatile bit. It is used to enable or disable the preamble bit data pattern output on dummy cycles. The PBE bit is defaulted as “0”, which means preamble bit is disabled. When it is set as “1”, the preamble bit will be enabled, and inputted into dummy cycles. To write the PBE bits requires the Write Status Register (WRSR) instruction to be executed.

4BYTE Indicator bit
By writing EN4B instruction, the 4BYTE bit may be set as "1" to access the address length of 32-bit for memory area of higher density (large than 128Mb). The default state is "0" as the 24-bit address mode. The 4BYTE bit may be cleared by power-off or writing EX4B instruction to reset the state to be "0".

Table 8. Configuration Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DC1 (Dummy cycle 1)	DC0 (Dummy cycle 0)	4 BYTE	PBE (Preamble bit Enable)	TB (top/bottom selected)	ODS 2 (output driver strength)	ODS 1 (output driver strength)	ODS 0 (output driver strength)
(Note 2)	*(Note 2)*	0=3-byte address mode 1=4-byte address mode (Default=0)	0=Disable 1=Enable	0=Top area protect 1=Bottom area protect (Default=0)	*(Note 1)*	*(Note 1)*	*(Note 1)*
volatile bit	volatile bit	volatile bit	volatile bit	OTP	volatile bit	volatile bit	volatile bit

Note 1: Please refer to *"Table 9. Output Driver Strength Table"*
Note 2: Please refer to *"Table 10. Dummy Cycle and Frequency Table (MHz)"*

Table 9. Output Driver Strength Table

ODS2	ODS1	ODS0	Output Driver Strength	Note
0	0	0	-	Impedance at VCC/2
0	0	1	17%	
0	1	0	25%	
0	1	1	58%	
1	0	0	-	
1	0	1	83%	
1	1	0	100%	
1	1	1	75%	

Table 10. Dummy Cycle and Frequency Table (MHz)

(STR Mode)

DC[1:0]	Numbers of Dummy clock cycles	Fast Read	Dual Output Fast Read	Quad Output Fast Read
00 (default)	8	120/133R	120/133R	104/114R
01	8	120/133R	120/133R	104/114R
10	8	120/133R	120/133R	104/114R
11	8	120/133R	120/133R	104/114R

DC[1:0]	Numbers of Dummy clock cycles	Dual IO Fast Read
00 (default)	4	80
01	8	104/114R
10	4	80
11	8	104/114R

DC[1:0]	Numbers of Dummy clock cycles	Quad IO Fast Read
00 (default)	6	70
01	4	54
10	8	84/95R
11	10	104/114R

(DTR Mode)

DC[1:0]	Numbers of Dummy clock cycles	Quad IO DTR Read
00 (default)	6	54
01	6	54
10	8	70/80R
11	10	84/100R

Note: "R" mean VCC range= 3.0V-3.6V.

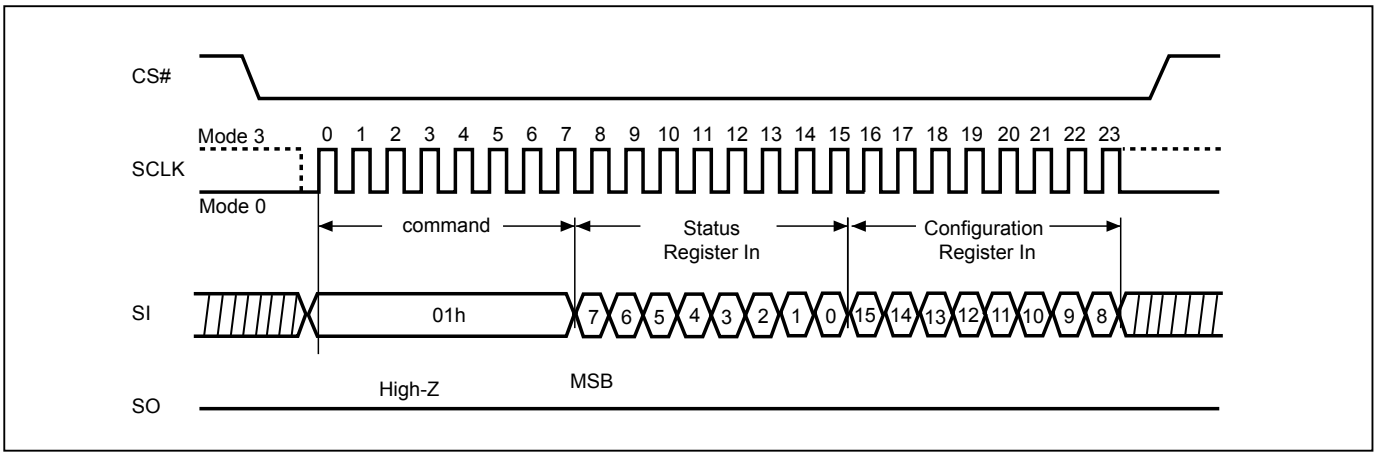
9-10. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits and Configuration Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 2. Protected Area Sizes"*). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ send WRSR instruction code→ Status Register data on SI→Configuration Register data on SI→CS# goes high.

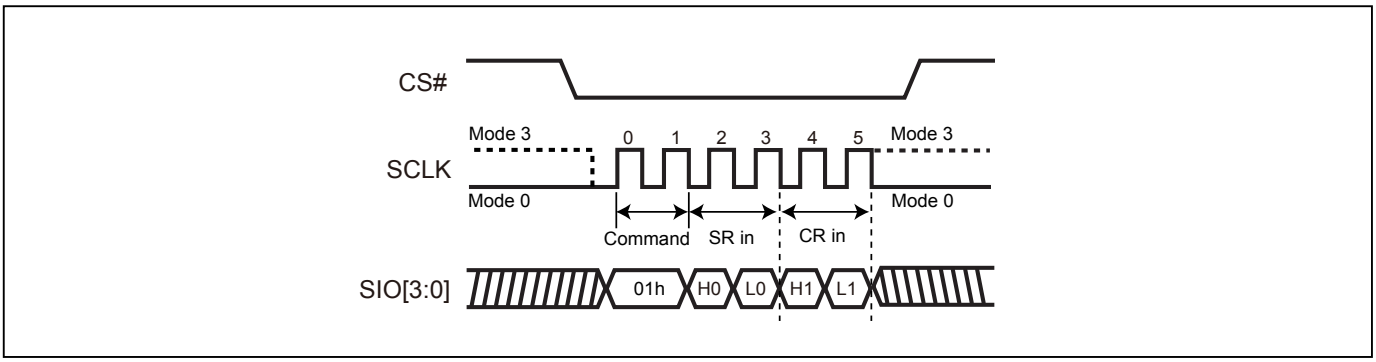
The CS# must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 31. Write Status Register (WRSR) Sequence (SPI Mode)



Note: The CS# must go high exactly at 8 bits or 16 bits data boundary to completed the write register command.

Figure 32. Write Status Register (WRSR) Sequence (QPI Mode)



Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0 and T/B bit, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0 and T/B bit, is at software protected mode (SPM)

Note:

If SRWD bit=1 but WP#/SIO2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and T/B bit and hardware protected mode by the WP#/SIO2 to against data modification.

Note:

To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0 and T/B bit.
If the system enter QPI or set QE=1, the feature of HPM will be disabled.

Table 11. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be programmed or erased.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be programmed or erased.

Note: As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *"Table 2. Protected Area Sizes"*.

Figure 33. WRSR flow

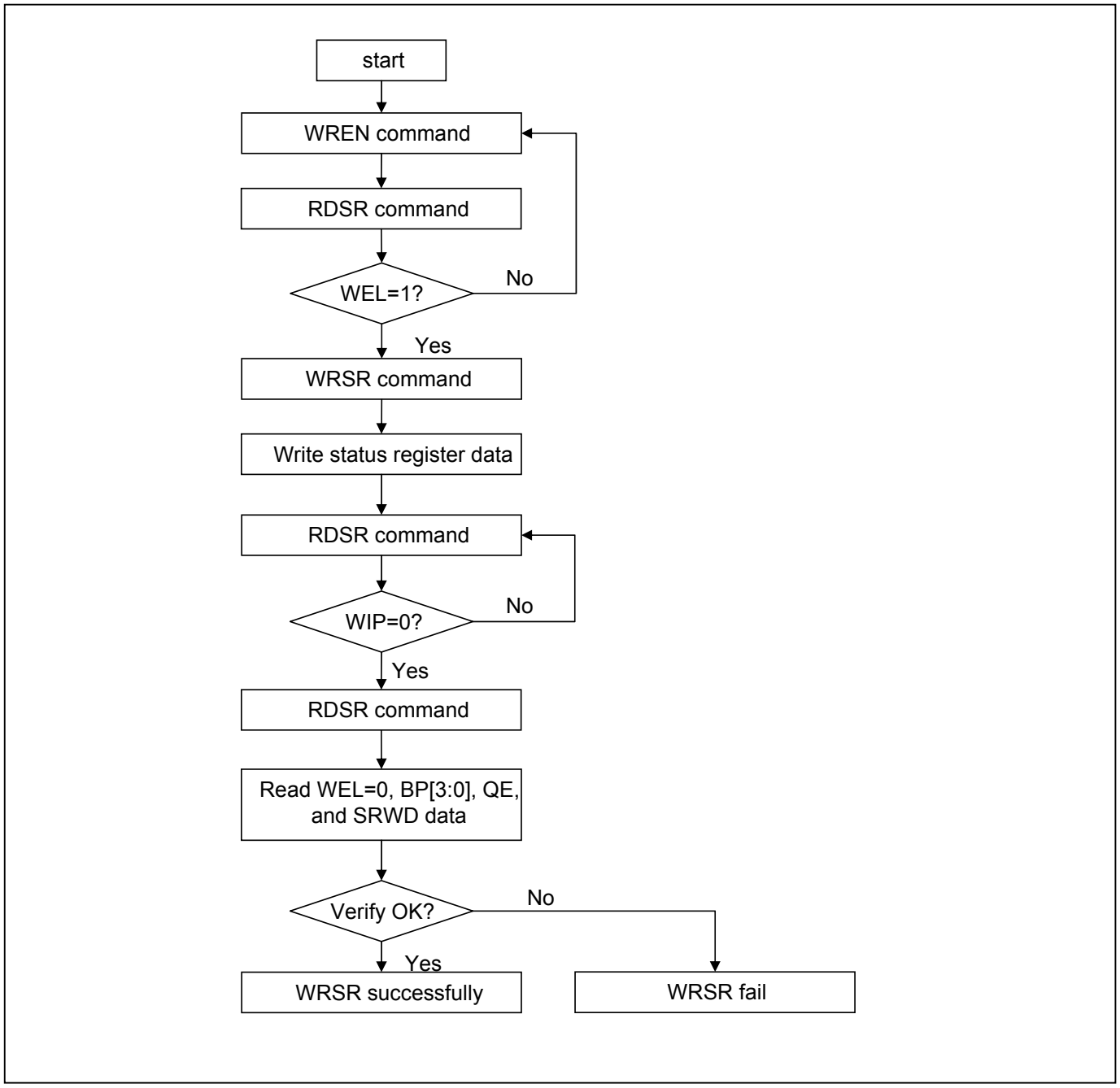
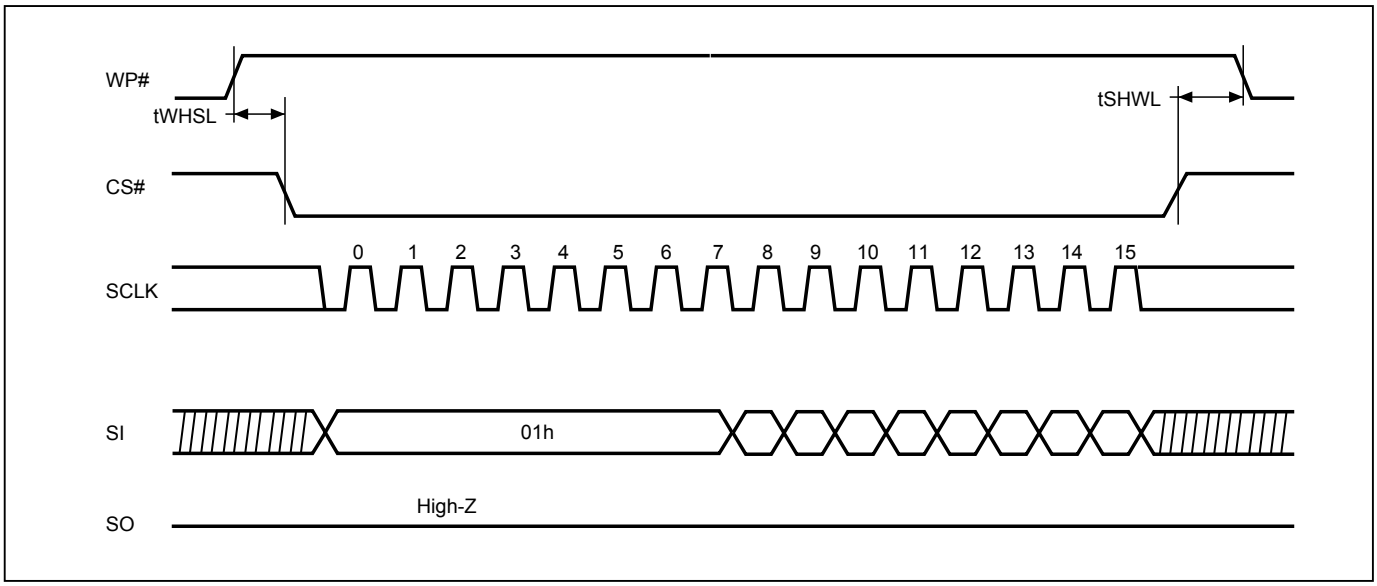


Figure 34. WP# Setup Timing and Hold Timing during WRSR when SRWD=1



Note: WP# must be kept high until the embedded operation finish.

9-11. Enter 4-byte mode (EN4B)

The EN4B instruction enables accessing the address length of 32-bit for the memory area of higher density (larger than 128Mb). The device default is in 24-bit address mode; after sending out the EN4B instruction, the bit5 (4BYTE bit) of Configuration Register will be automatically set to "1" to indicate the 4-byte address mode has been enabled. Once the 4-byte address mode is enabled, the address length becomes 32-bit instead of the default 24-bit. There are three methods to exit the 4-byte mode: writing exit 4-byte mode (EX4B) instruction, Reset or power-off.

All instructions are accepted normally, and just the address bit is changed from 24-bit to 32-bit.

The following commands don't support 4-byte address: RDSFDP, RES and REMS.

The sequence of issuing EN4B instruction is: CS# goes low→send EN4B instruction to enter 4-byte mode (automatically set 4BYTE bit as "1") → CS# goes high.

9-12. Exit 4-byte mode (EX4B)

The EX4B instruction is executed to exit the 4-byte address mode and return to the default 3-bytes address mode. After sending out the EX4B instruction, the bit5 (4BYTE bit) of Configuration Register will be cleared to be "0" to indicate the exit of the 4-byte address mode. Once exiting the 4-byte address mode, the address length will return to 24-bit.

The sequence of issuing EX4B instruction is: CS# goes low → send EX4B instruction to exit 4-byte mode (automatically clear the 4BYTE bit to be "0") → CS# goes high.

9-13. Read Data Bytes (READ)

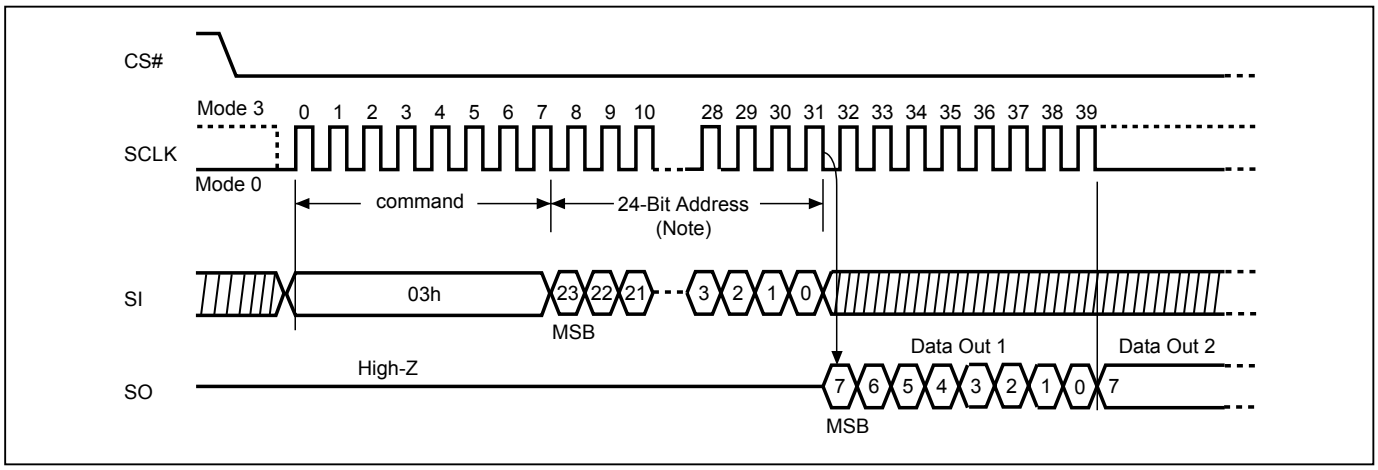
The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the *"9-11. Enter 4-byte mode (EN4B)"* section.

The sequence of issuing READ instruction is: CS# goes low→send READ instruction code→ 3-byte or 4-byte address on SI→ data out on SO→to end READ operation, drive CS# high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 35. Read Data Bytes (READ) Sequence (SPI Mode only)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

9-14. Read Data Bytes at Higher Speed (FAST_READ)

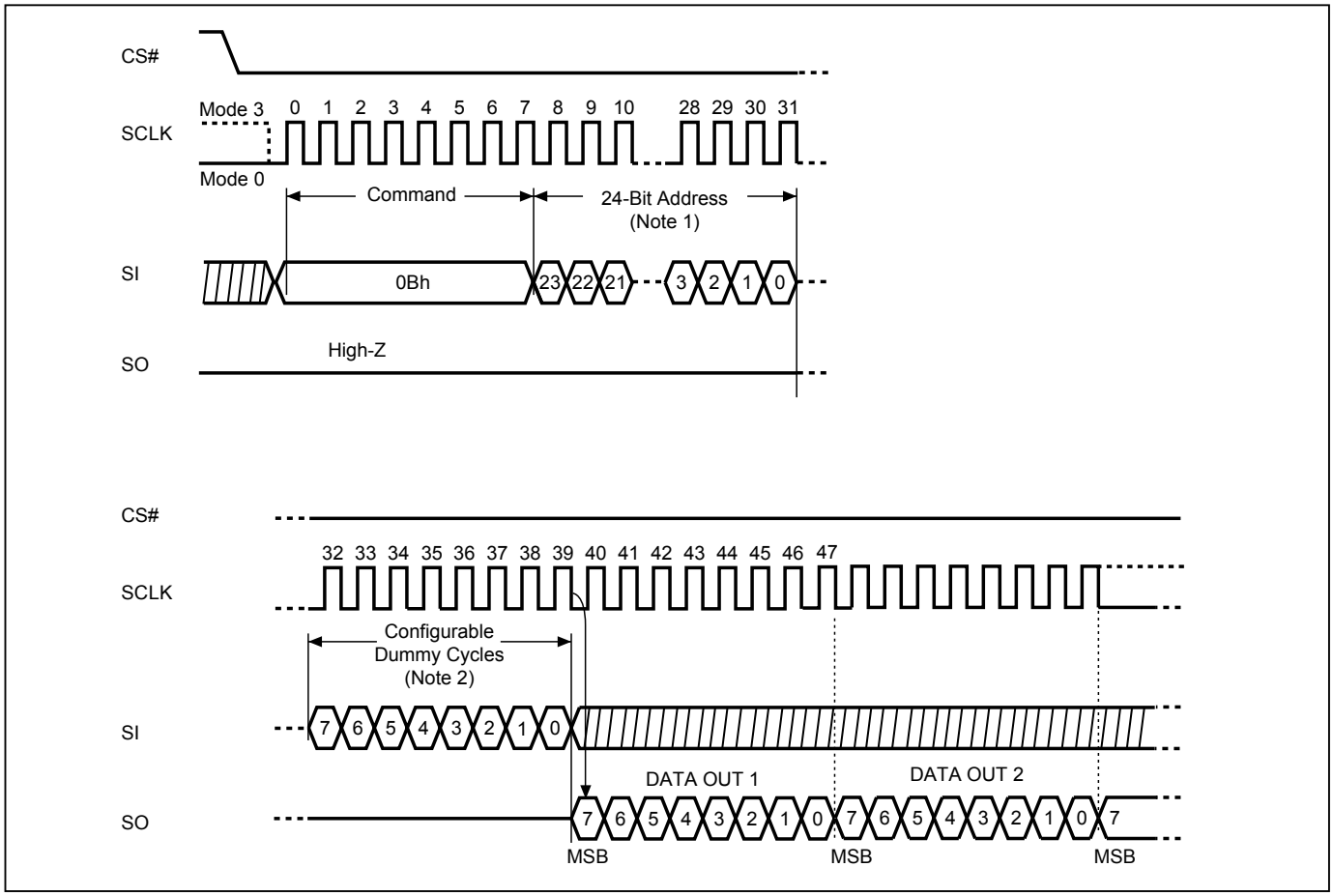
The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the *"9-11. Enter 4-byte mode (EN4B)"* section.

The sequence of issuing FAST_READ instruction is: CS# goes low→ send FAST_READ instruction code→ 3-byte or 4-byte address on SI→ 8 dummy cycles (default)→ data out on SO→ to end FAST_READ operation, drive CS# high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 36. Read at Higher Speed (FAST_READ) Sequence (SPI Mode only)



Notes:

1. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

9-15. Dual Output Read Mode (DREAD)

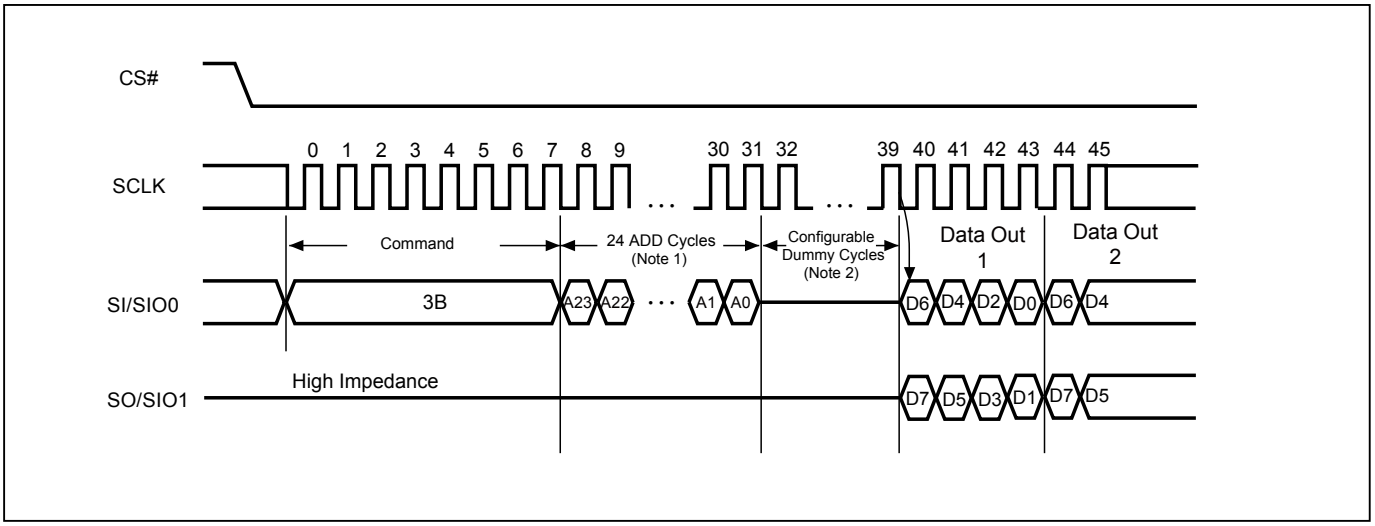
The DREAD instruction enables double throughput of the Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the *"9-11. Enter 4-byte mode (EN4B)"* section.

The sequence of issuing DREAD instruction is: CS# goes low→send DREAD instruction→3-byte or 4-byte address on SIO0→ 8 dummy cycles (default) on SIO0→ data out interleave on SIO1 & SIO0→ to end DREAD operation can, drive CS# high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 37. Dual Read Mode Sequence (SPI Mode only)



Notes:

1. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

9-16. 2 x I/O Read Mode (2READ)

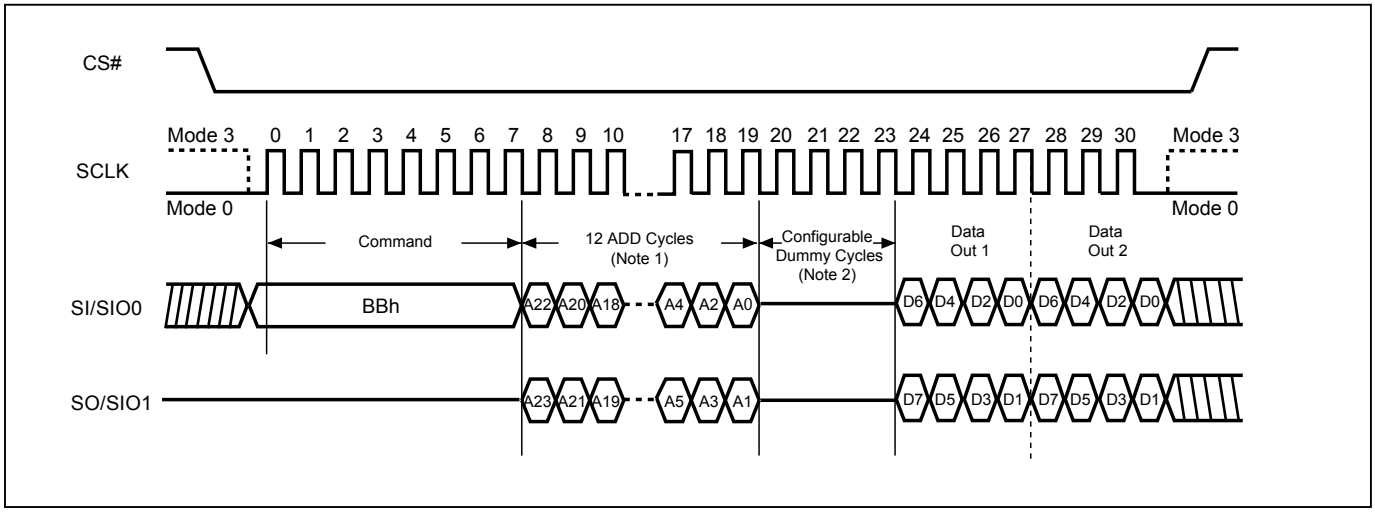
The 2READ instruction enables double throughput of the Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to *"9-11. Enter 4-byte mode (EN4B)"* section.

The sequence of issuing 2READ instruction is: CS# goes low→ send 2READ instruction→ 3-byte or 4-byte address interleave on SIO1 & SIO0→ 4 dummy cycles (default) on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation, drive CS# high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 38. 2 x I/O Read Mode Sequence (SPI Mode only)



Notes:

1. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

9-17. Quad Read Mode (QREAD)

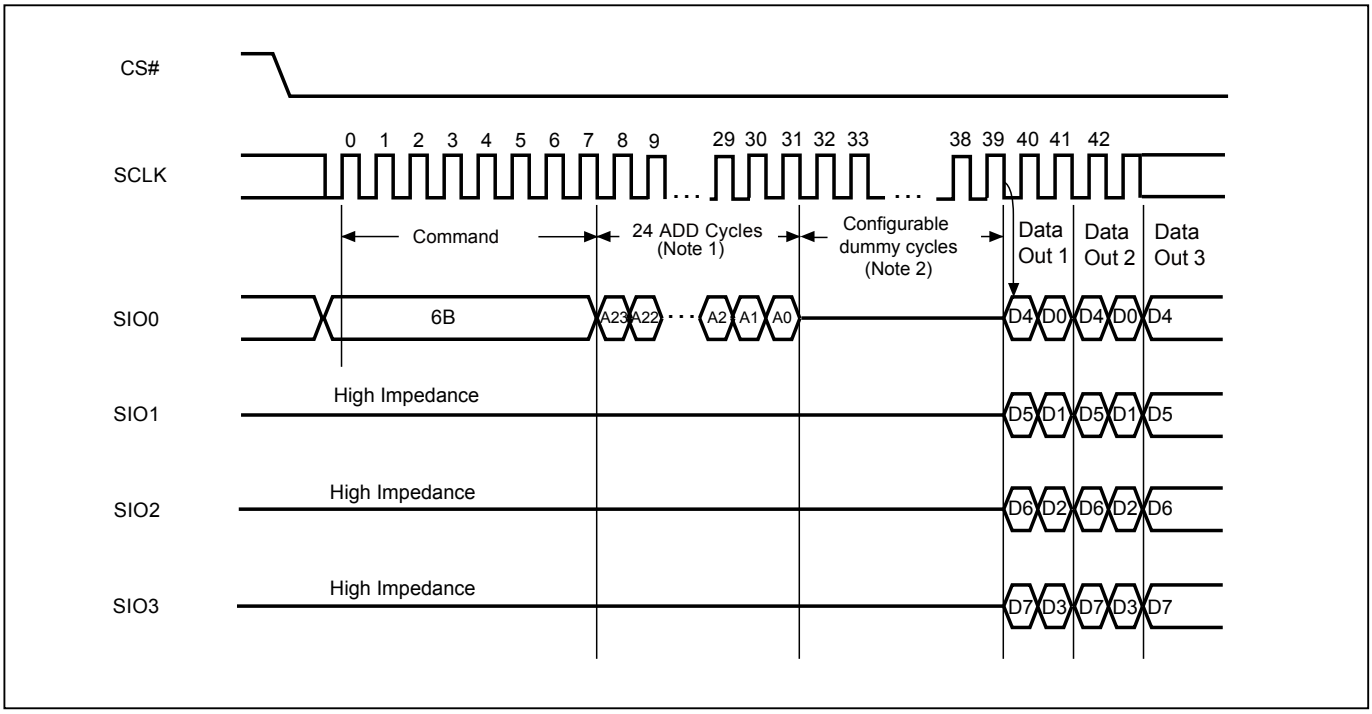
The QREAD instruction enables quad throughput of the Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the QREAD instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to *"9-11. Enter 4-byte mode (EN4B)"* section.

The sequence of issuing QREAD instruction is: CS# goes low→send QREAD instruction → 3-byte or 4-byte address on SI → 8 dummy cycle (Default) → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QREAD operation, drive CS# high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 39. Quad Read Mode Sequence (SPI Mode only)



Notes:
1. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

9-18. 4 x I/O Read Mode (4READ)

The 4READ instruction enables quad throughput of the Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

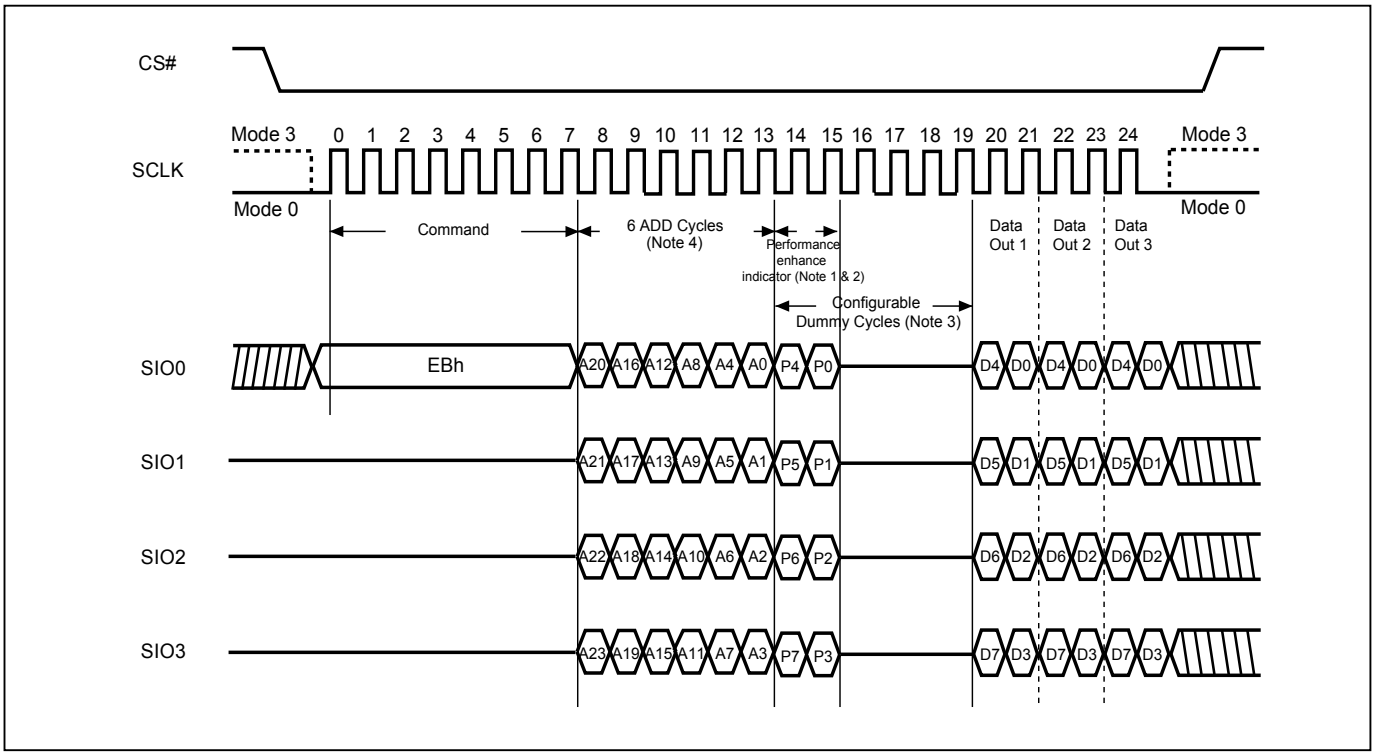
The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to *"9-11. Enter 4-byte mode (EN4B)"* section.

4 x I/O Read on SPI Mode (4READ) The sequence of issuing 4READ instruction is: CS# goes low→ send 4READ instruction→ 3-byte or 4-byte address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles (Default) →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation, drive CS# high at any time during data out.

4 x I/O Read on QPI Mode (4READ) The 4READ instruction also support on QPI command mode. The sequence of issuing 4READ instruction QPI mode is: CS# goes low→ send 4READ instruction→ 3-byte or 4-byte address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles (Default) →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation, drive CS# high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

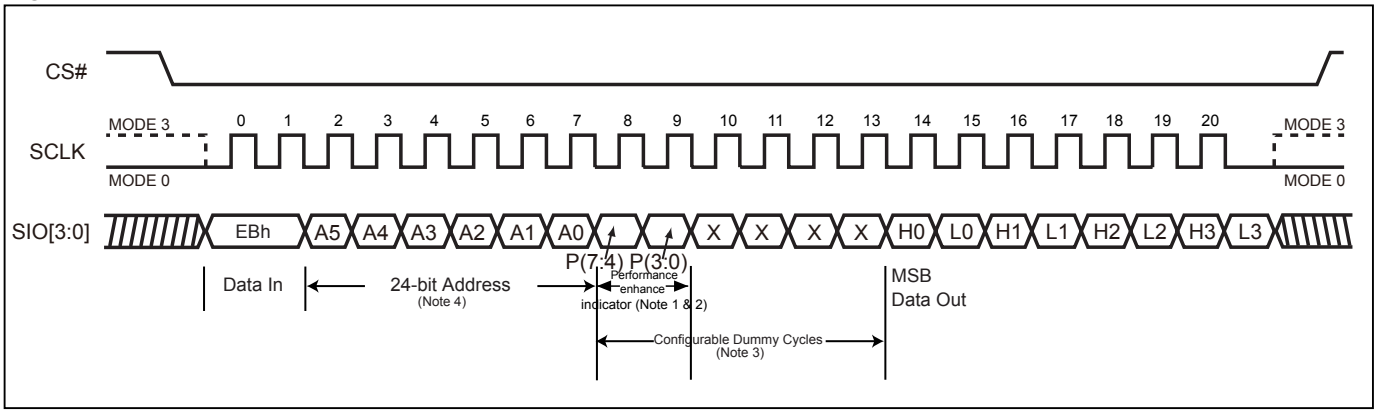
Figure 40. 4 x I/O Read Mode Sequence (SPI Mode)



Notes:

1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will result in entering the performance enhance mode.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.
4. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 41. 4 x I/O Read Mode Sequence (QPI Mode)



Notes:

1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will result in entering the performance enhance mode.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.
4. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

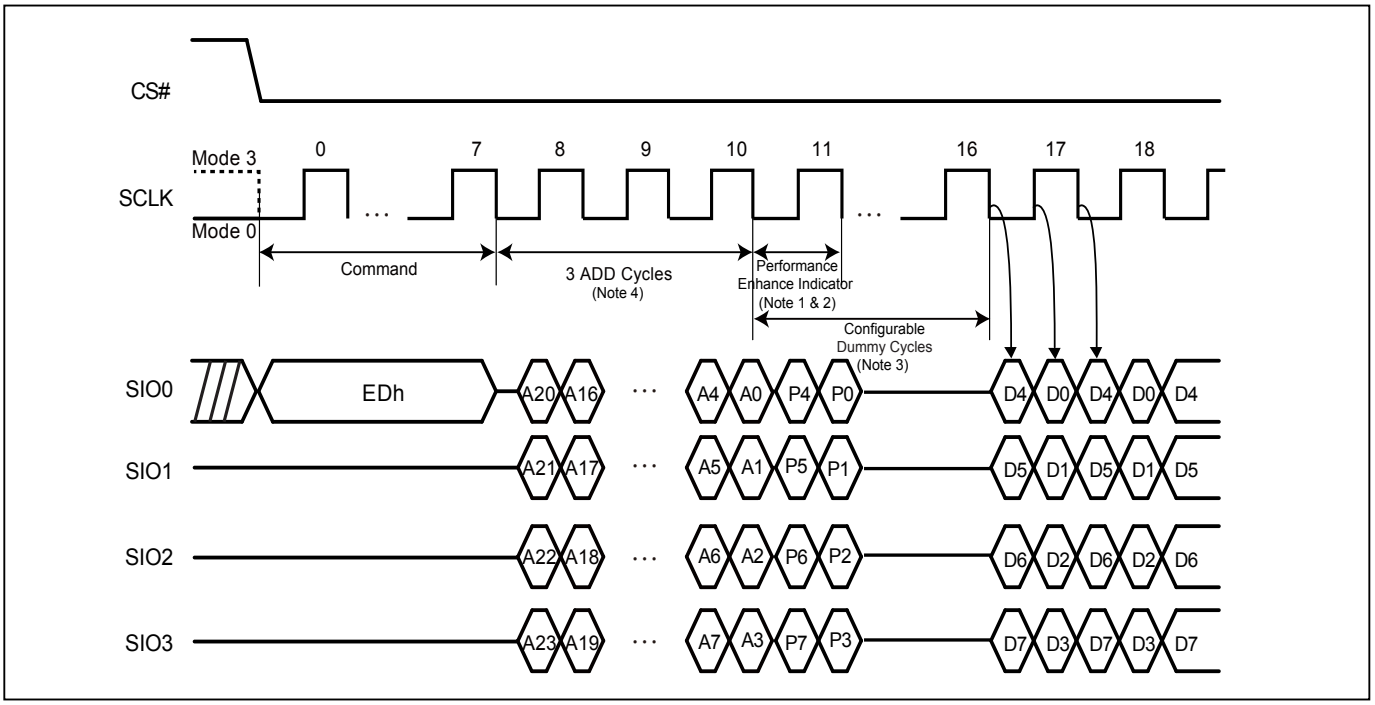
9-19. 4 x I/O Double Transfer Rate Read Mode (4DTRD)

The 4DTRD instruction enables Double Transfer Rate throughput on quad I/O of the Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4DTRD instruction. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of SCLK. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4DTRD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4DTRD instruction, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

While Program/Erase/Write Status Register cycle is in progress, 4DTRD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

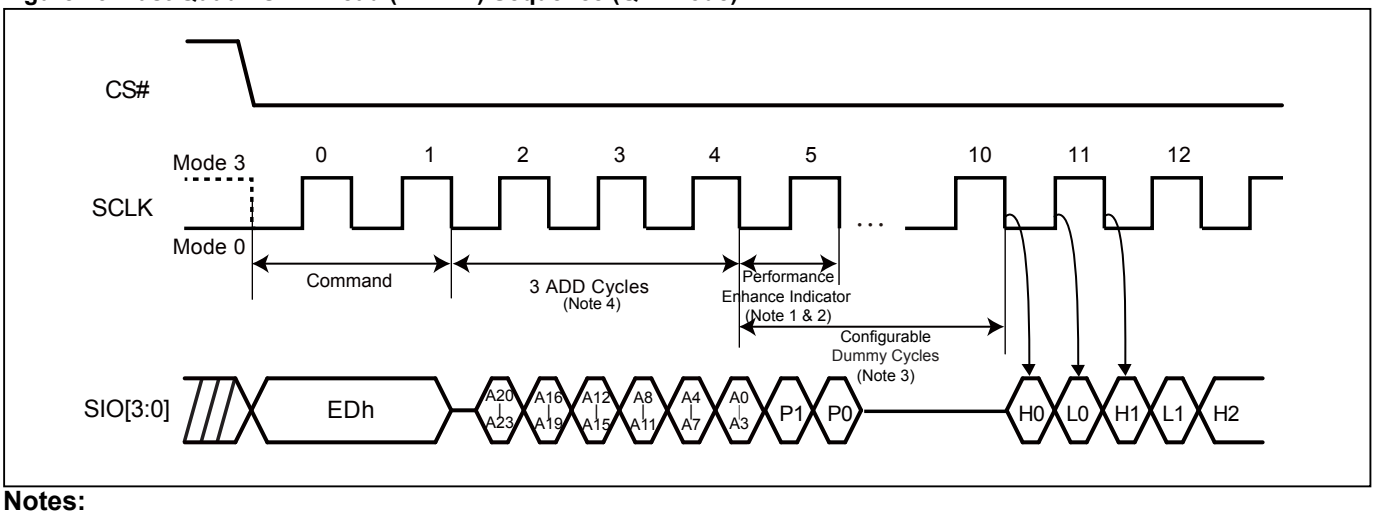
Figure 42. Fast Quad I/O DT Read (4DTRD) Sequence (SPI Mode)



Notes:

1. Hi-impedance is inhibited for this clock cycle.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will result in entering the performance enhance mode.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.
4. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 43. Fast Quad I/O DT Read (4DTRD) Sequence (QPI Mode)



Notes:

1. Hi-impedance is inhibited for this clock cycle.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will result in entering the performance enhance mode.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.
4. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

9-20. Preamble Bit

The Preamble Bit data pattern supports system/memory controller to determine valid window of data output more easily and improve data capture reliability while the flash memory is running in high frequency.

Preamble Bit data pattern can be enabled or disabled by setting the bit4 of Configuration register (Preamble bit Enable bit). Once the CR<4> is set, the preamble bit is inputted into dummy cycles.

Enabling preamble bit will not affect the function of enhance mode bit. In Dummy cycles, performance enhance mode bit still operates with the same function. Preamble bit will output after performance enhance mode bit.

The preamble bit is a fixed 8-bit data pattern (00110100). While dummy cycle number reaches 10, the complete 8 bits will start to output right after the performance enhance mode bit. While dummy cycle is not sufficient of 10 cycles, the rest of the preamble bits will be cut. For example, 8 dummy cycles will cause 6 preamble bits to output, and 6 dummy cycles will cause 4 preamble bits to output.

Figure 44. SDR 1I/O (10DC)

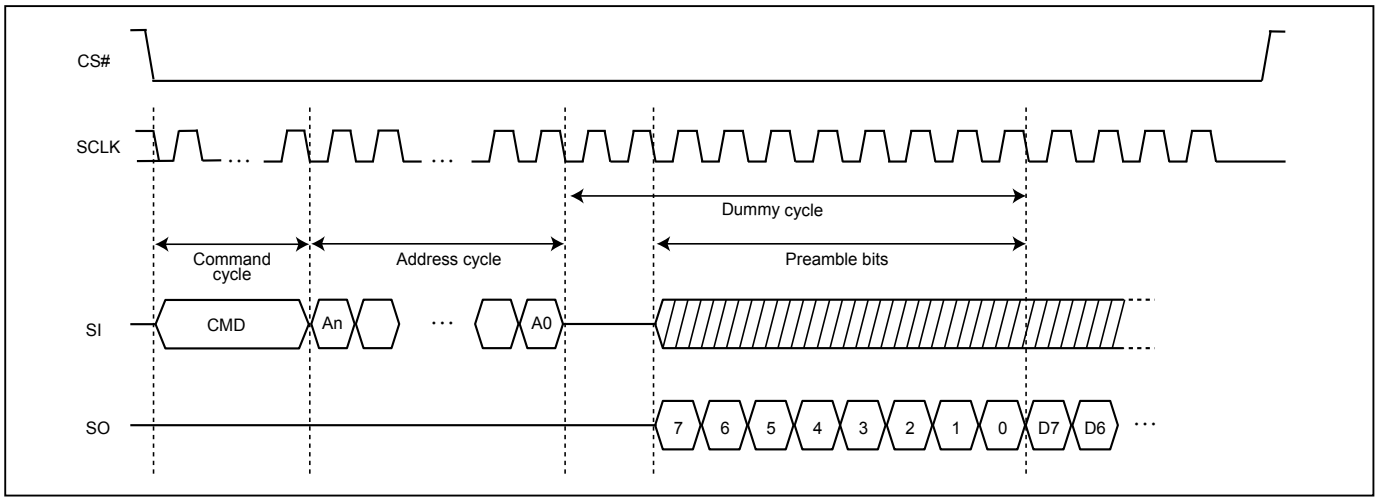


Figure 45. SDR 1I/O (8DC)

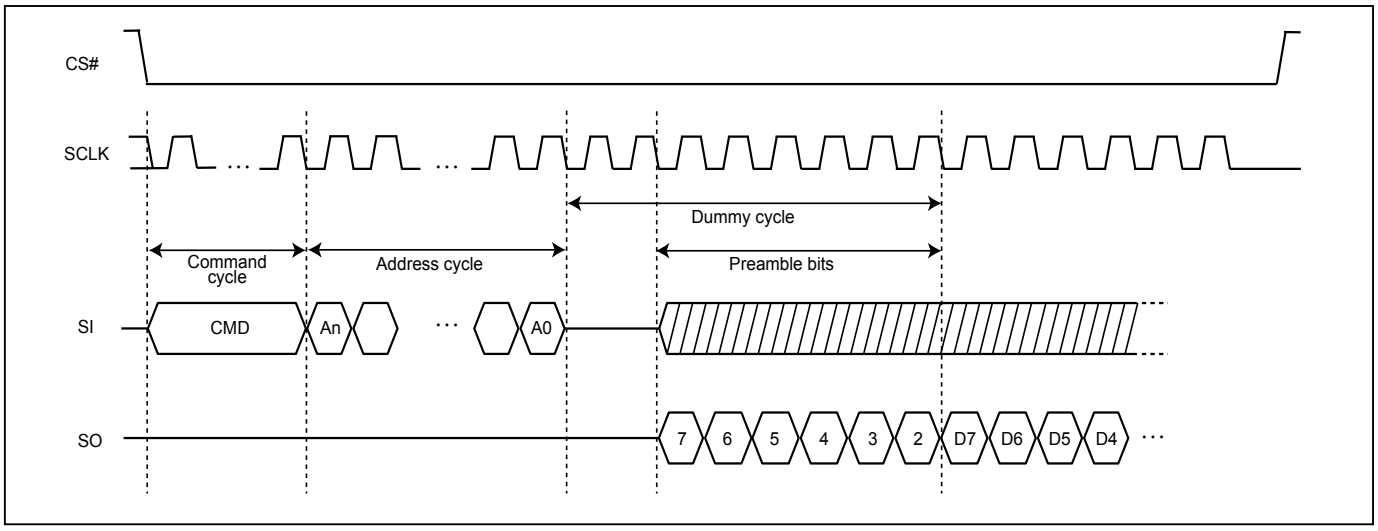


Figure 46. SDR 2I/O (10DC)

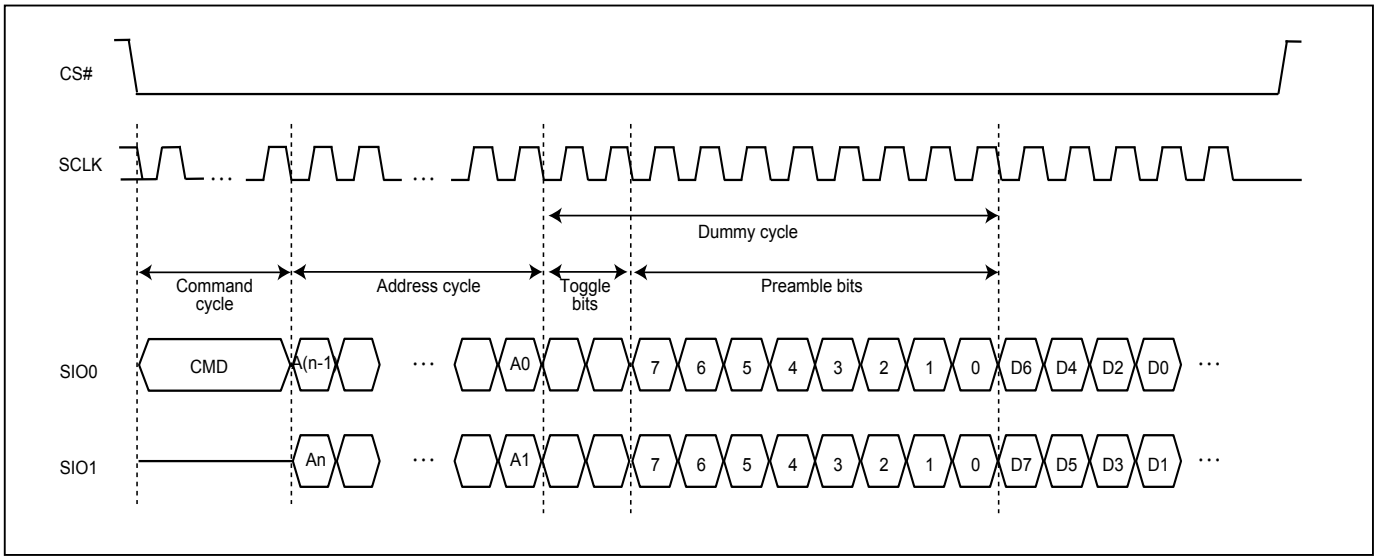


Figure 47. SDR 2I/O (8DC)

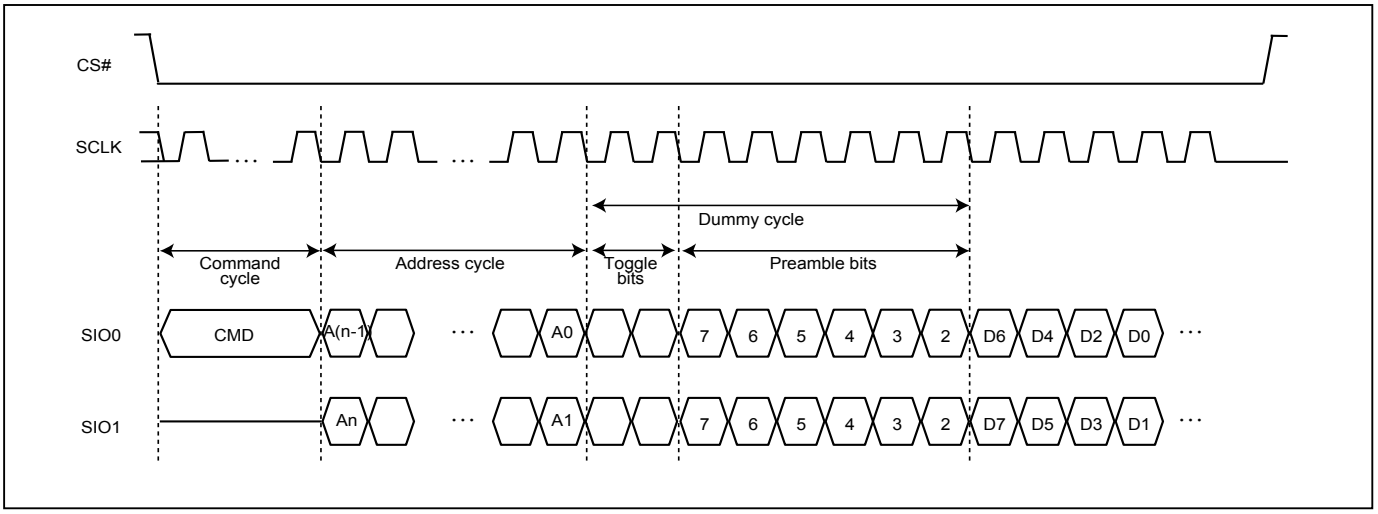


Figure 48. SDR 4I/O (10DC)

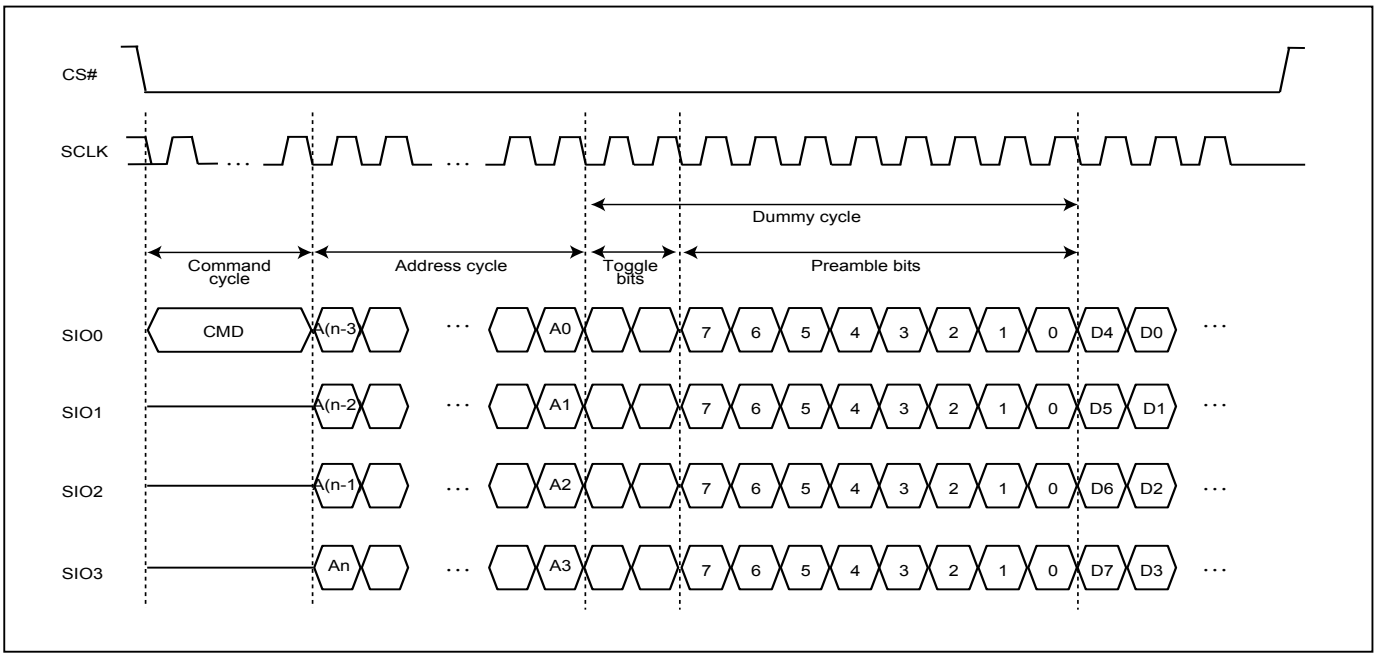


Figure 49. SDR 4I/O (8DC)

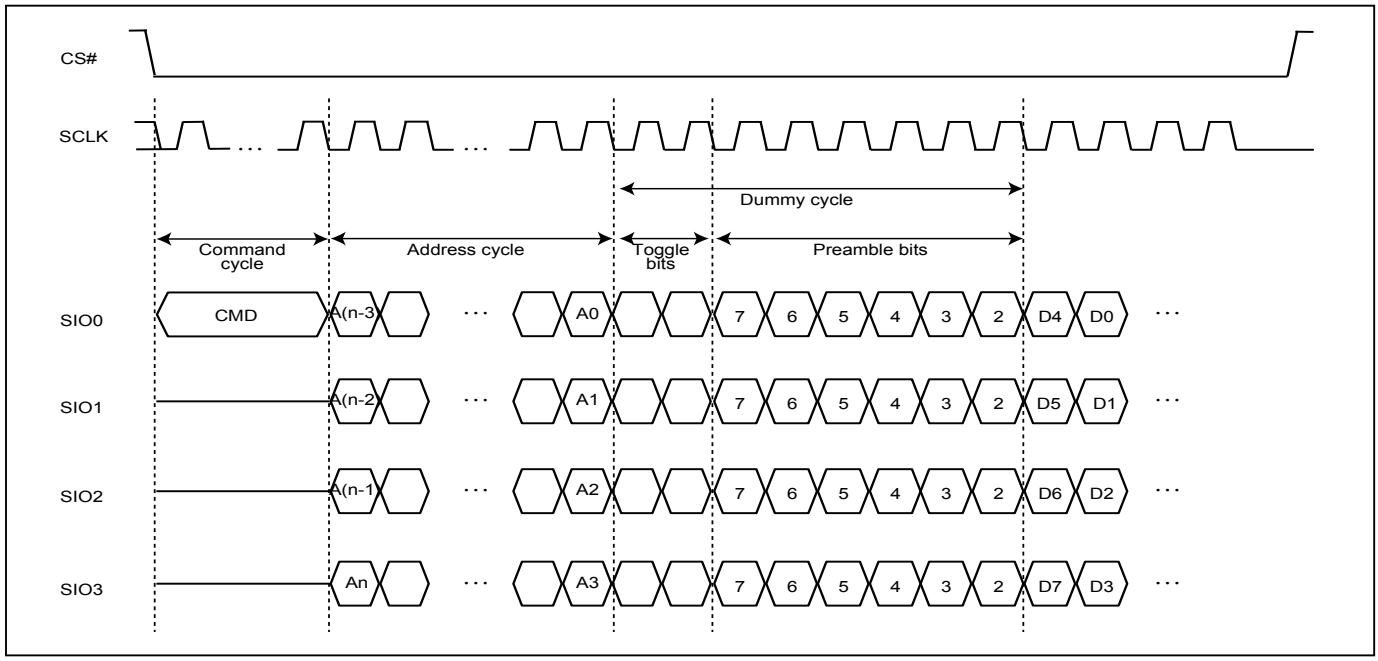
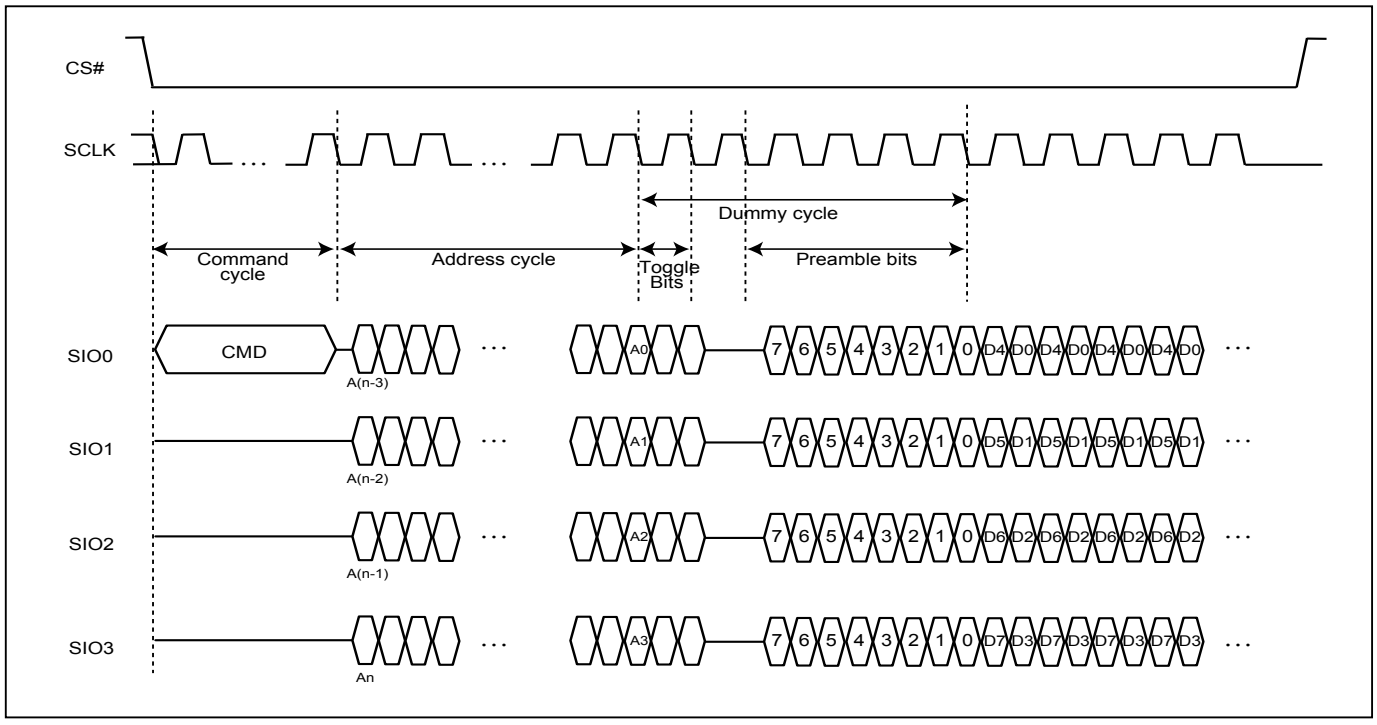


Figure 50. DTR4IO (6DC)



9-21. 4 Byte Address Command Set

The operation of 4-byte address command set was very similar to original 3-byte address command set. The only different is all the 4-byte command set request 4-byte address (A31-A0) followed by instruction code. The command set support 4-byte address including: READ4B, FAST_READ4B, DREAD4B, 2READ4B, QREAD4B, 4READ4B, PP4B, 4PP4B, SE4B, BE32K4B, BE4B. Please note that it is not necessary to issue EN4B command before issuing any of 4-byte command set.

Figure 51. Read Data Bytes using 4-Byte Address Sequence (READ4B) (SPI Mode only)

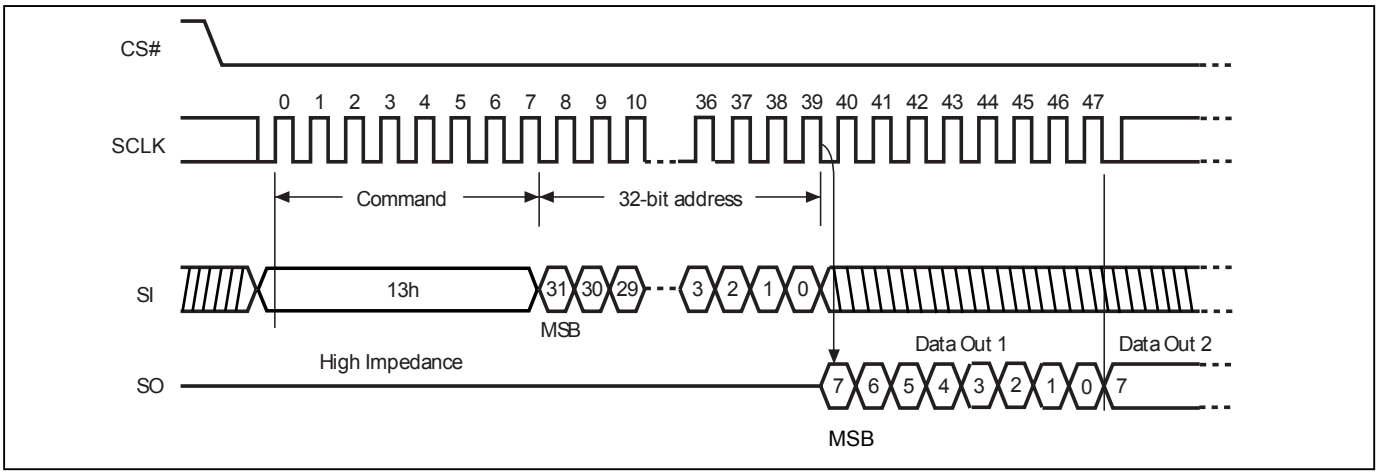
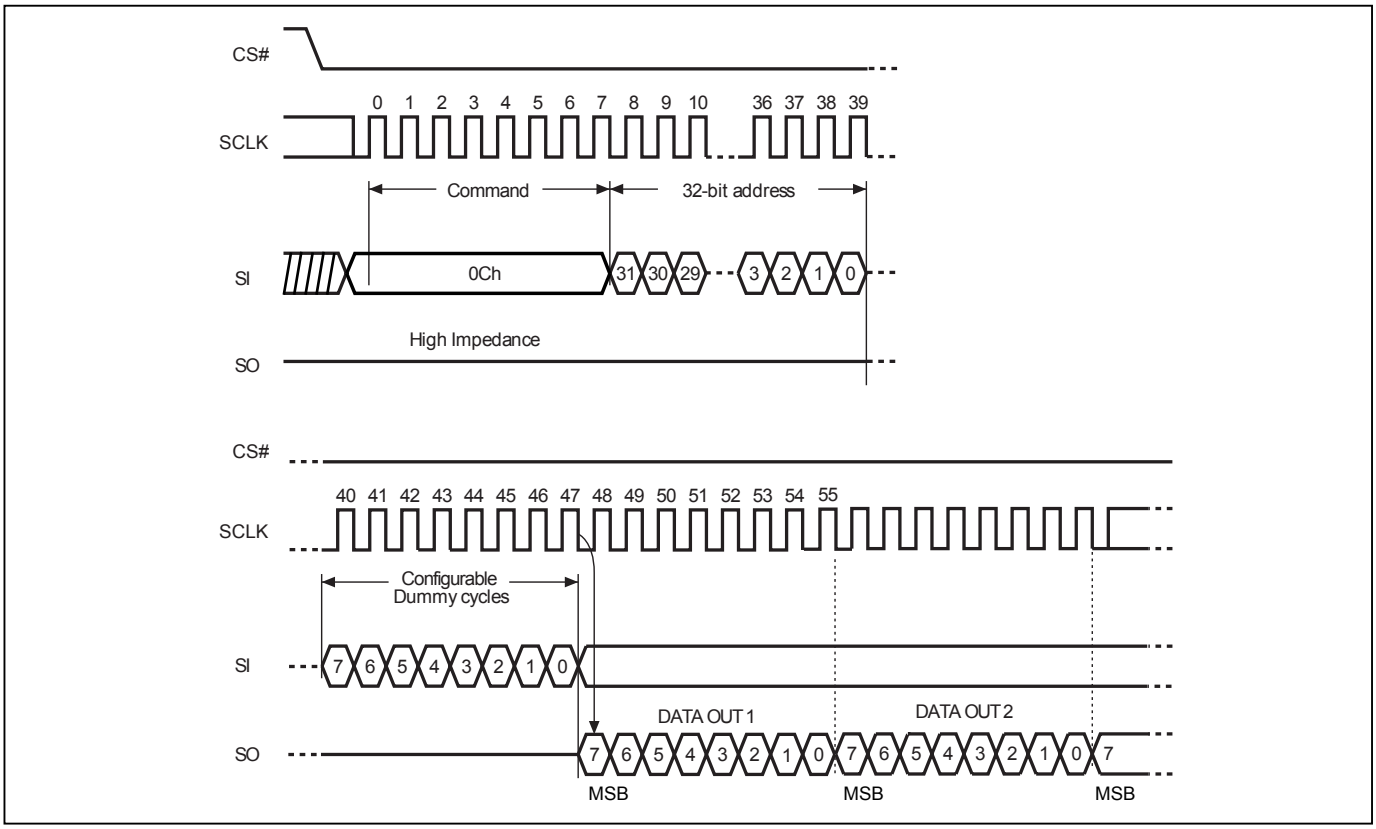
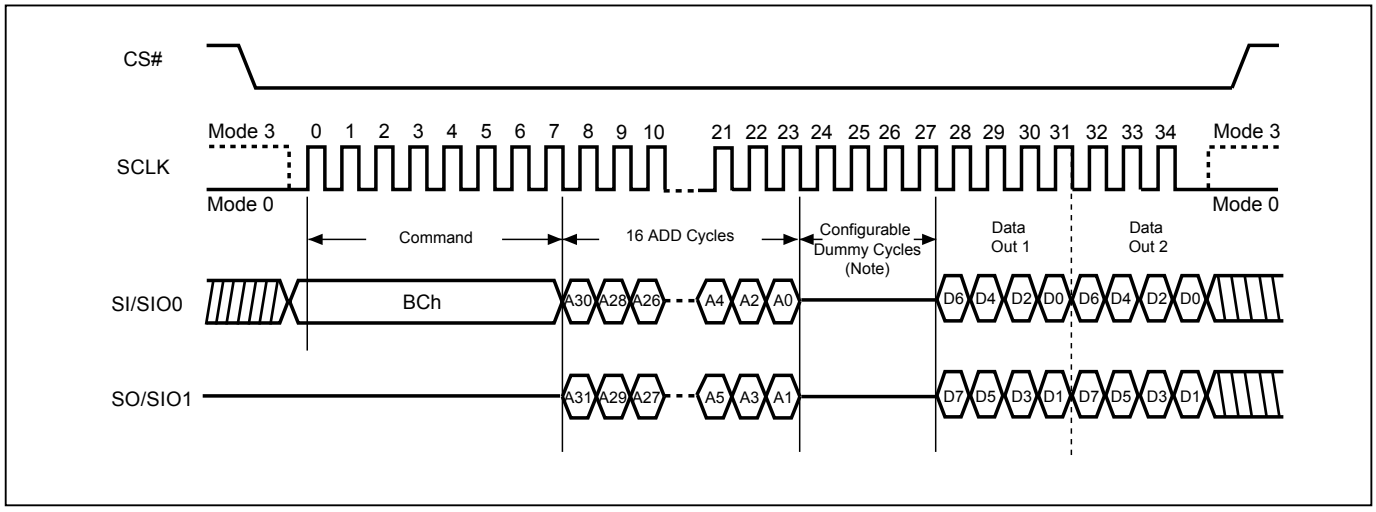


Figure 52. Read Data Bytes at Higher Speed using 4-Byte Address Sequence (FASTREAD4B) (SPI Mode only)



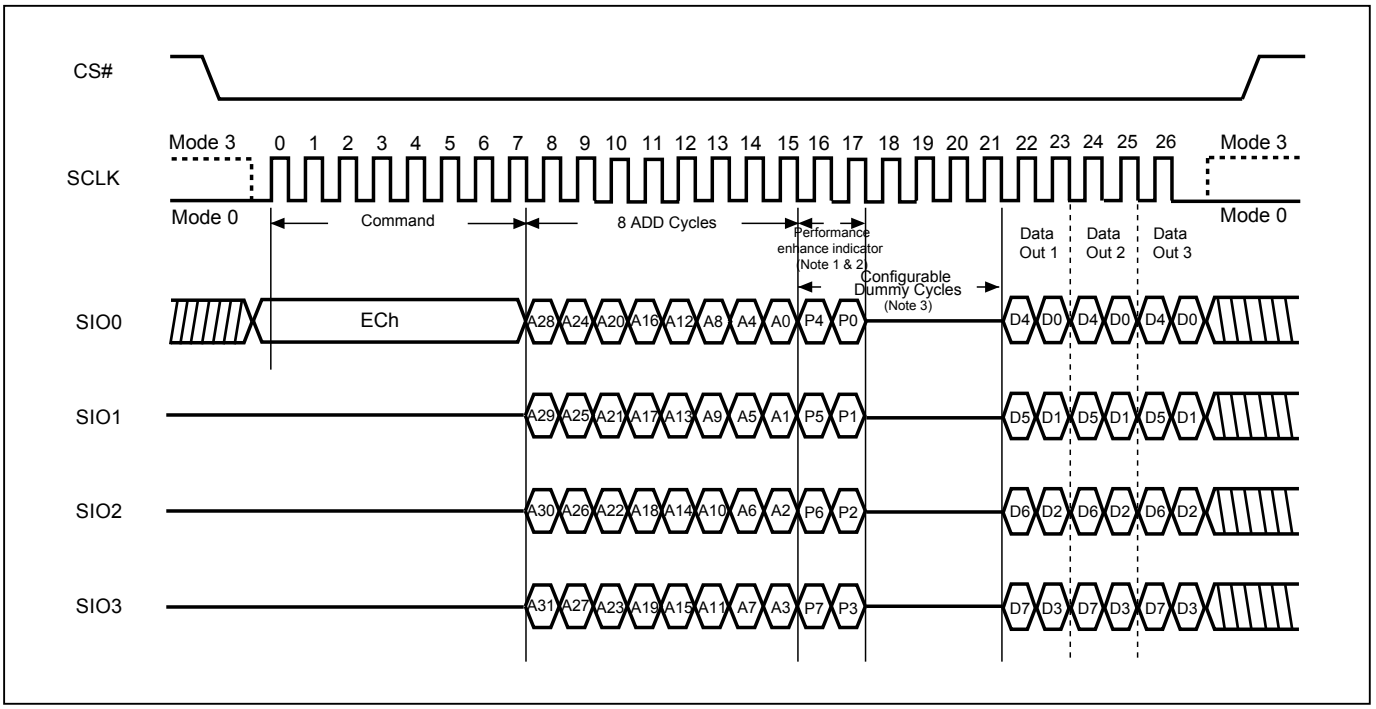
Note: Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

Figure 53. 2 x I/O Fast Read using 4-Byte Address Sequence (2READ4B) (SPI Mode only)



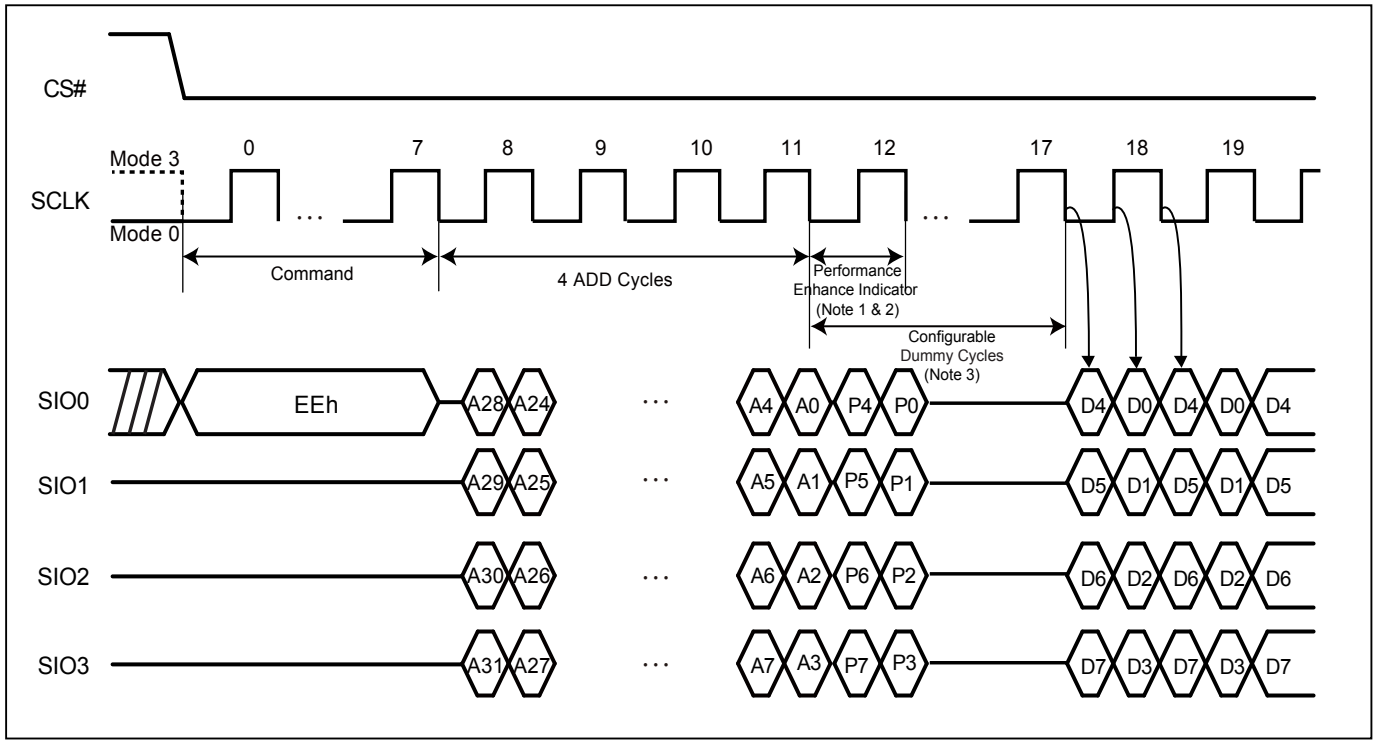
Note: Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

Figure 54. 4 I/O Fast Read using 4-Byte Address sequence (4READ4B) (SPI Mode only)



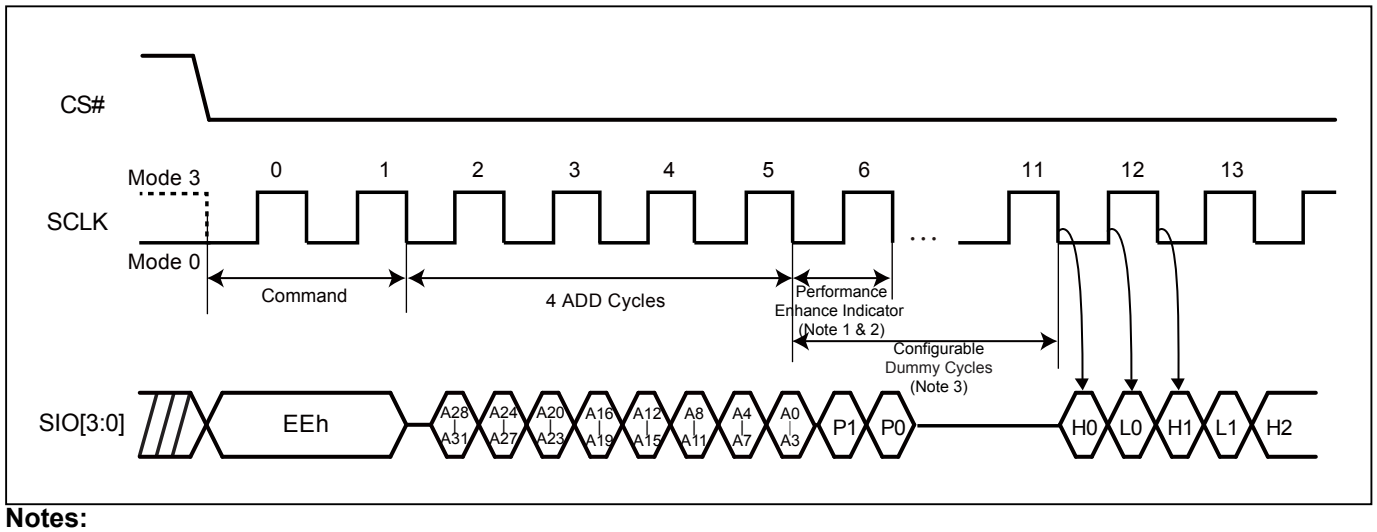
Notes:
1. Hi-impedance is inhibited for this clock cycle.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will result in entering the performance enhance mode.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

Figure 55. Fast Quad I/O DT Read (4DTRD4B) Sequence (SPI Mode)



Notes:
1. Hi-impedance is inhibited for this clock cycle.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will result in entering the performance enhance mode.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

Figure 56. Fast Quad I/O DT Read (4DTRD4B) Sequence (QPI Mode)



Notes:
1. Hi-impedance is inhibited for this clock cycle.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will result in entering the performance enhance mode.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

9-22. Burst Read

The Burst Read feature allows applications to fill a cache line with a fixed length of data without using multiple read commands. Burst Read is disabled by default at power-up or reset. Burst Read is enabled by setting the Burst Length. When the Burst Length is set, reads will wrap on the selected boundary (8/16/32/64-bytes) containing the initial target address. For example if an 8-byte Wrap Depth is selected, reads will wrap on the 8-byte-page-aligned boundary containing the initial read address.

To set the Burst Length, drive CS# low → send SET BURST LENGTH instruction code (C0h) → send WRAP CODE →drive CS# high. Refer to the table below for valid 8-bit Wrap Codes and their corresponding Wrap Depth.

Data	Wrap Around	Wrap Depth
00h	Yes	8-byte
01h	Yes	16-byte
02h	Yes	32-byte
03h	Yes	64-byte
1xh	No	X

Once Burst Read is enabled, it will remain enabled until the device is power-cycled or reset. The SPI and QPI mode 4READ and 4READ4B read commands support the wrap around feature after Burst Read is enabled. To change the wrap depth, resend the Burst Read instruction with the appropriate Wrap Code. To disable Burst Read, send the Burst Read instruction with Wrap Code 1xh. QPI “EBh” "ECh" and SPI “EBh” "ECh" support wrap around feature after wrap around is enabled. Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Figure 57. Burst Read (SPI Mode)

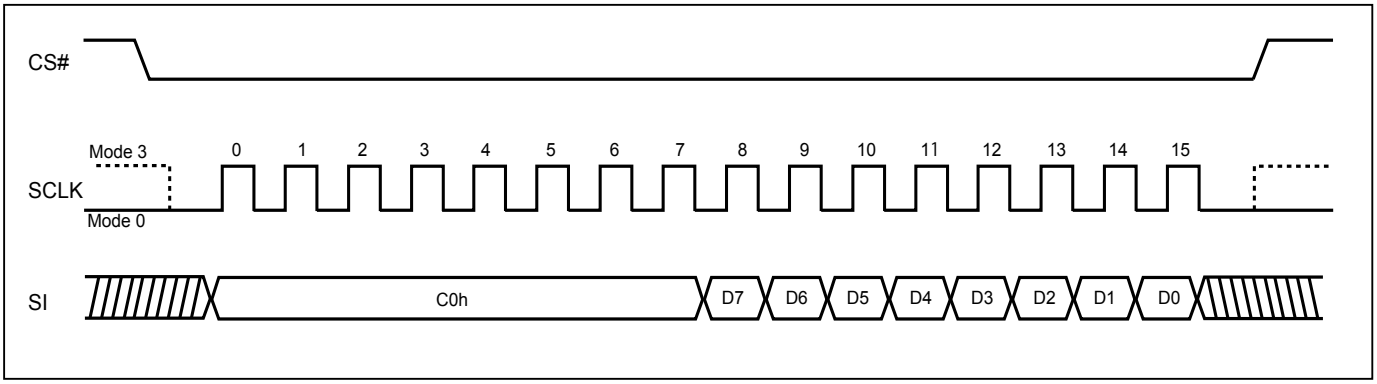
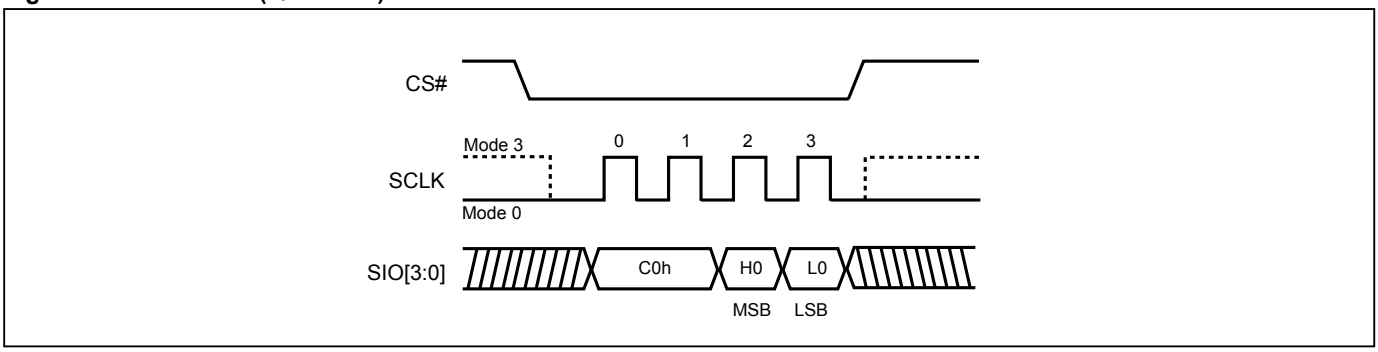


Figure 58. Burst Read (QPI Mode)



Note: MSB=Most Significant Bit
LSB=Least Significant Bit

9-23. Performance Enhance Mode - XIP (execute-in-place)

The device could waive the command cycle bits if the two cycle bits after address cycle toggles.

Performance enhance mode is supported in both SPI and QPI mode.

In QPI mode, “EBh” "ECh" "EDh" "EEh" and SPI “EBh” "ECh" "EDh" "EEh" commands support enhance mode. The performance enhance mode is not supported in dual I/O mode.

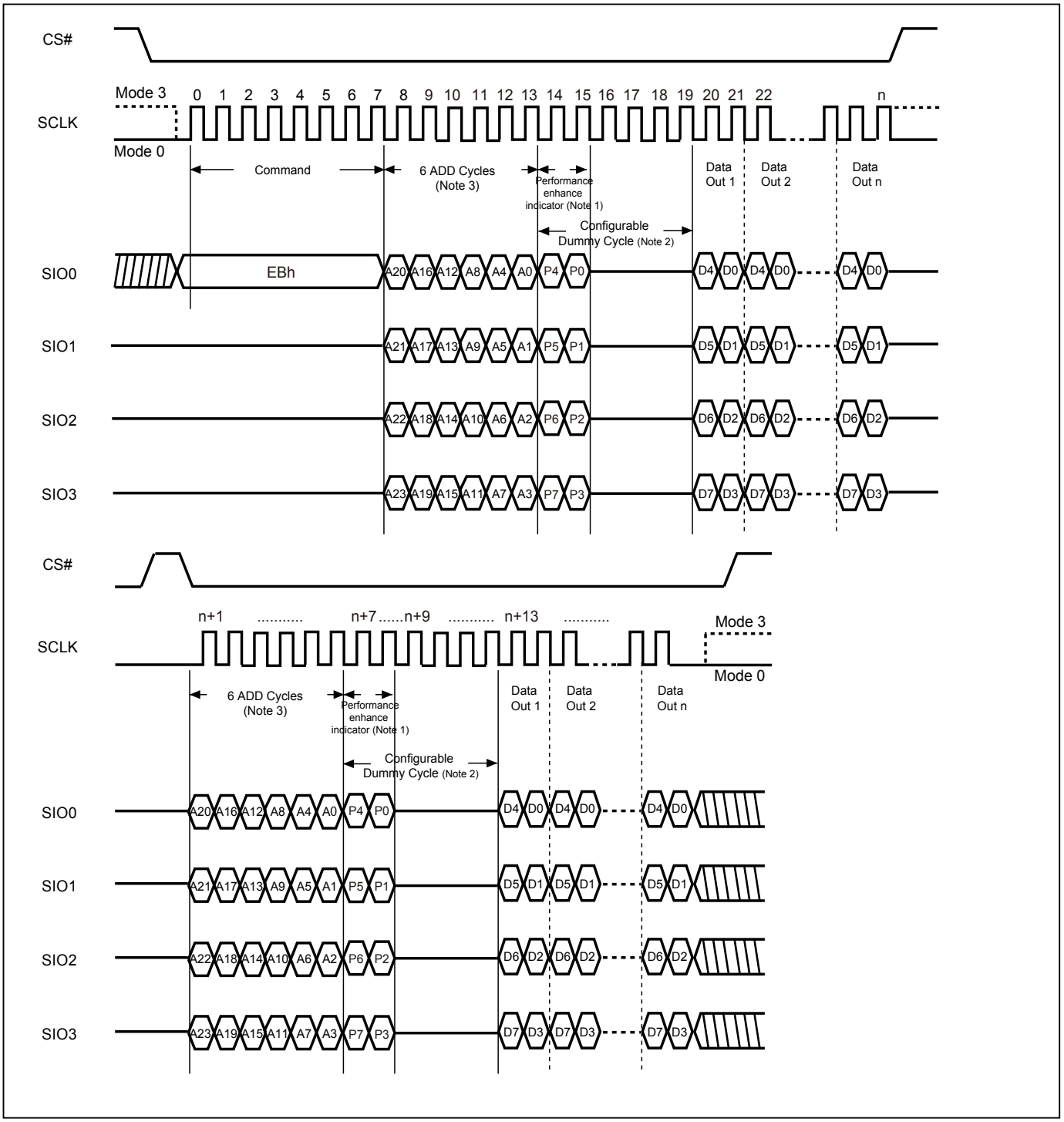
To enter performance-enhancing mode, P[7:4] must be toggling with P[3:0]; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and skip the next 4READ instruction. To leave enhance mode, P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh, 00h, AAh or 55h along with CS# is afterwards raised and then lowered. Issuing ”FFh” data cycle can also exit enhance mode. The system then will leave performance enhance mode and return to normal operation.

To conduct the Performance Enhance Mode Reset operation in SPI mode, FFh data cycle(8 clocks in 3-byte address mode)/3FFh data cycle(10 clocks in 4-byte address mode), should be issued in 1I/O sequence. In QPI Mode, FFFFFFFFh data cycle(8 clocks in 3-byte address mode)/FFFFFFFFFFh data cycle (10 clocks in 4-byte address mode), in 4I/O should be issued. If the system controller is being Reset during operation, the flash device will return to the standard SPI operation.

After entering enhance mode, following CS# go high, the device will stay in the read mode and treat CS# go low of the first clock as address instead of command cycle.

This sequence of issuing 4READ instruction especially useful in random access: CS# goes low→send 4READ instruction→3-bytes or 4-bytes address interleave on SIO3, SIO2, SIO1 & SIO0→performance enhance toggling bit P[7:0]→ 4 dummy cycles (Default) →data out until CS# goes high → CS# goes low (The following 4READ instruction is not allowed, hence 8 cycles of 4READ can be saved comparing to normal 4READ mode) → 3-bytes or 4-bytes random access address.

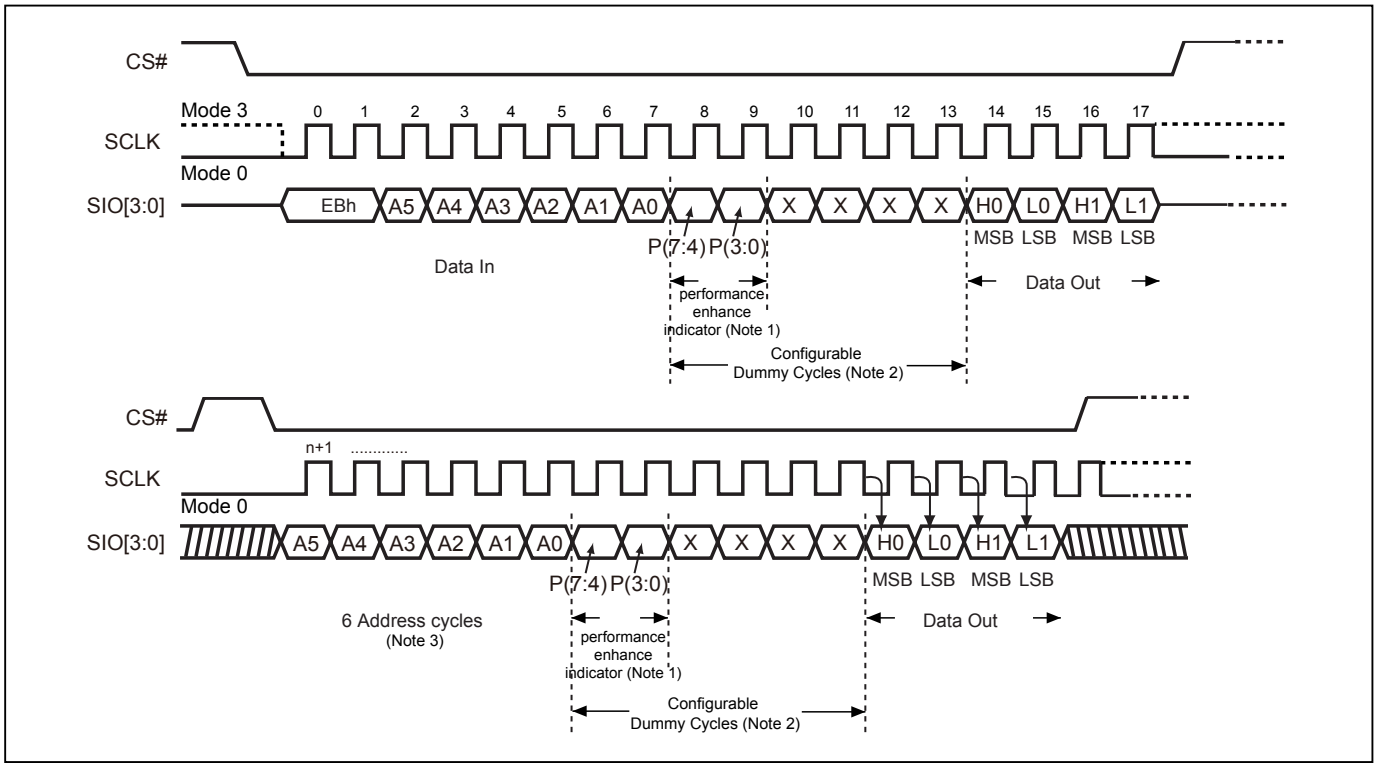
Figure 59. 4 x I/O Read Performance Enhance Mode Sequence (SPI Mode)



Notes:

1. If not using performance enhance recommend to keep 1 or 0 in performance enhance indicator. Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.
3. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 60. 4 x I/O Read Performance Enhance Mode Sequence (QPI Mode)



Notes:

1. If not using performance enhance recommend to keep 1 or 0 in performance enhance indicator. Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.
3. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

9-24. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (Please refer to *"Table 4. Memory Organization"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. Address bits [Am-A12] (Am is the most significant address) select the sector address.

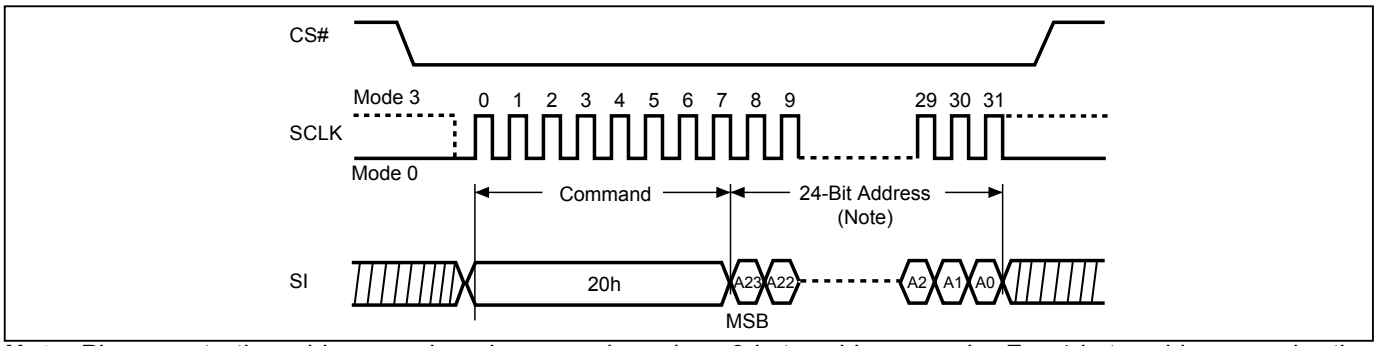
To enter the 4-byte address mode, please refer to *"9-11. Enter 4-byte mode (EN4B)"* section.

The sequence of issuing SE instruction is: CS# goes low→ send SE instruction code→ 3-byte or 4-byte address on SI→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

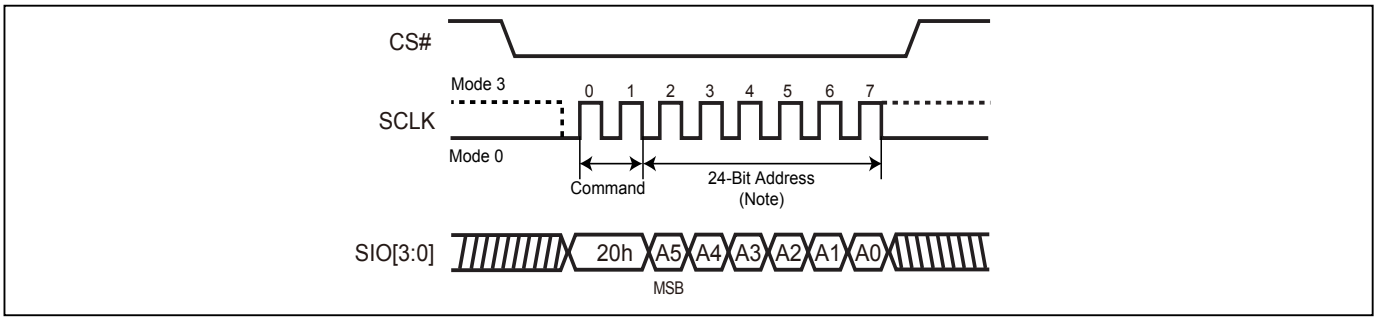
The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB (WPSEL=1; Individual Sector Protect Mode), the Sector Erase (SE) instruction will not be executed on the block.

Figure 61. Sector Erase (SE) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 62. Sector Erase (SE) Sequence (QPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

9-25. Block Erase (BE32K)

The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (Please refer to *"Table 4. Memory Organization"*) is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

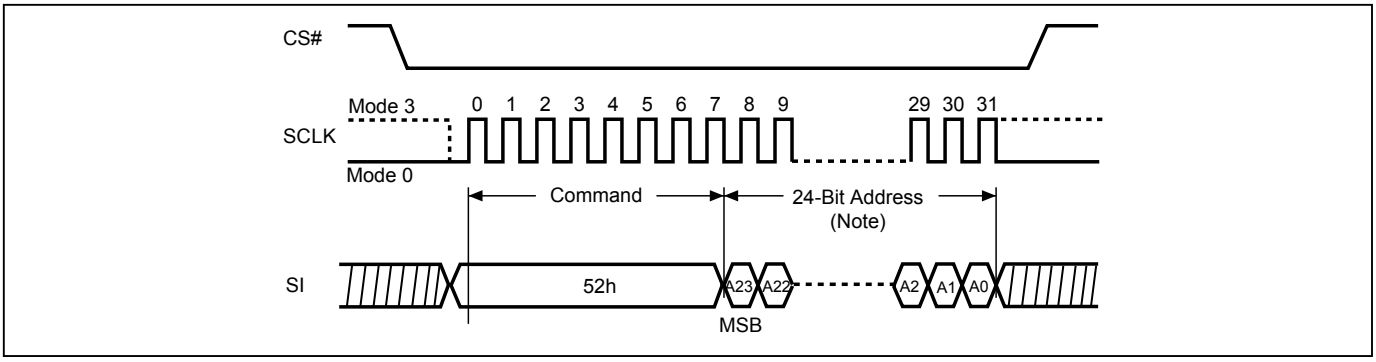
Address bits [Am-A15] (Am is the most significant address) select the 32KB block address. The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte address mode, please refer to *"9-11. Enter 4-byte mode (EN4B)"* section.

The sequence of issuing BE32K instruction is: CS# goes low→ send BE32K instruction code→ 3-byte or 4-byte address on SI→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

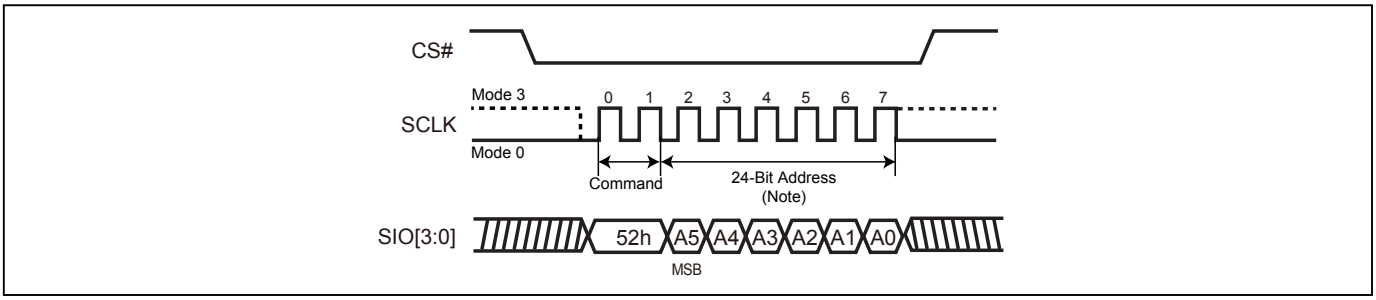
The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while during the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB (WPSEL=1; Individual Sector Protect Mode), the Block Erase (BE32K) instruction will not be executed on the block.

Figure 63. Block Erase 32KB (BE32K) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 64. Block Erase 32KB (BE32K) Sequence (QPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

9-26. Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to *"Table 4. Memory Organization"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

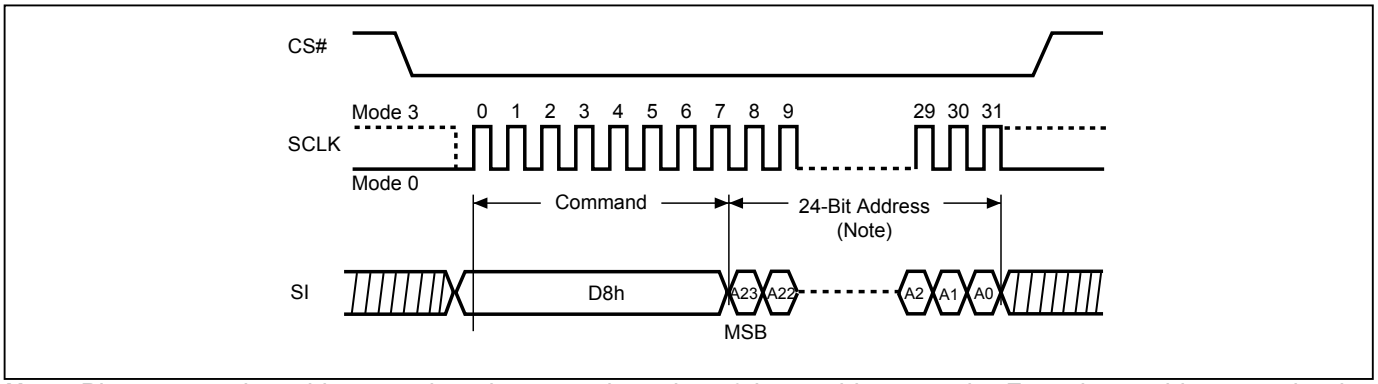
The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte address mode, please refer to the *"9-11. Enter 4-byte mode (EN4B)"* Mode section.

The sequence of issuing BE instruction is: CS# goes low→ send BE instruction code→ 3-byte or 4-byte address on SI→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

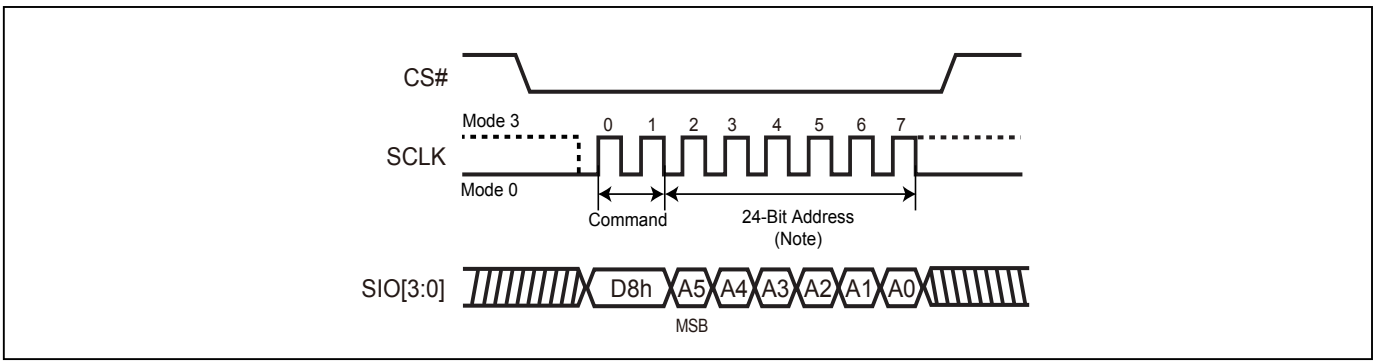
The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the Block is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB (WPSEL=1; Individual Sector Protect Mode), the Block Erase (BE) instruction will not be executed on the block.

Figure 65. Block Erase (BE) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 66. Block Erase (BE) Sequence (QPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

9-27. Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→send CE instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared.

When the chip is under "Block protect (BP) Mode" (WPSEL=0). The Chip Erase (CE) instruction will not be executed, if one (or more) sector is protected by BP3-BP0 bits. It will be only executed when BP3-BP0 all set to "0".

When the chip is under "Advances Sector Protect Mode" (WPSEL=1). The Chip Erase (CE) instruction will be executed on unprotected block. The protected Block will be skipped. If one (or more) 4K byte sector was protected in top or bottom 64K byte block, the protected block will also skip the chip erase command.

Figure 67. Chip Erase (CE) Sequence (SPI Mode)

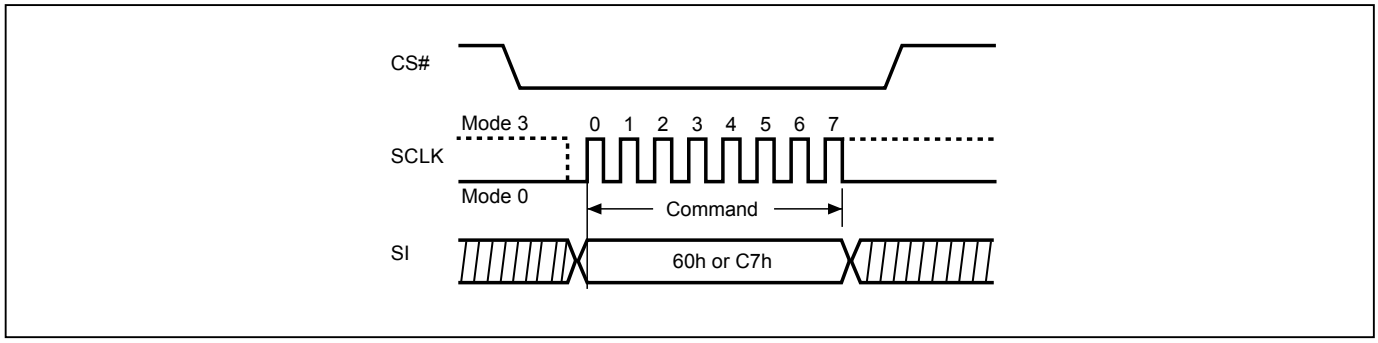
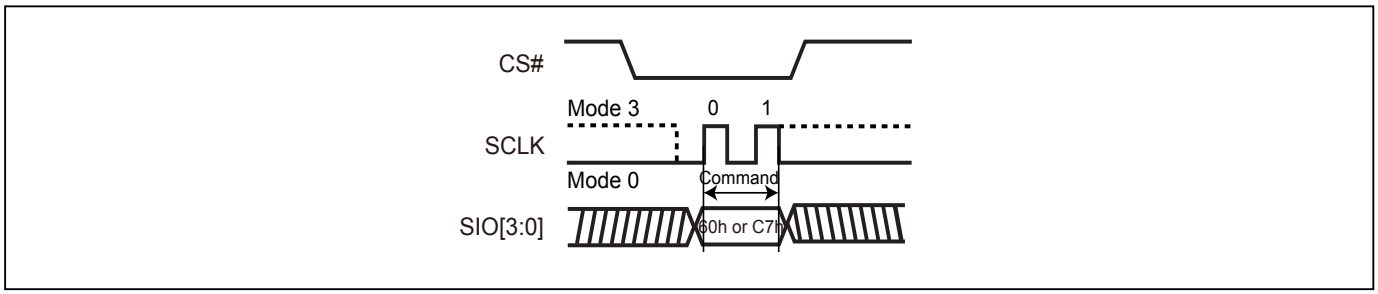


Figure 68. Chip Erase (CE) Sequence (QPI Mode)



9-28. Page Program (PP)

The Page Program (PP) instruction is for programming memory bits to "0". One to 256 bytes can be sent to the device to be programmed. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). If more than 256 data bytes are sent to the device, only the last 256 data bytes will be accepted and the previous data bytes will be disregarded. The Page Program instruction requires that all the data bytes fall within the same 256-byte page. The low order address byte A[7:0] specifies the starting address within the selected page. Bytes that will cross a page boundary will wrap to the beginning of the selected page. The device can accept (256 minus A[7:0]) data bytes without wrapping. If 256 data bytes are going to be programmed, A[7:0] should be set to 0.

Please refer to *"9-42. ECC (Error Correction Code)"* for the partial program or double program restrictions.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte address mode, please refer to *"9-11. Enter 4-byte mode (EN4B)"* section.

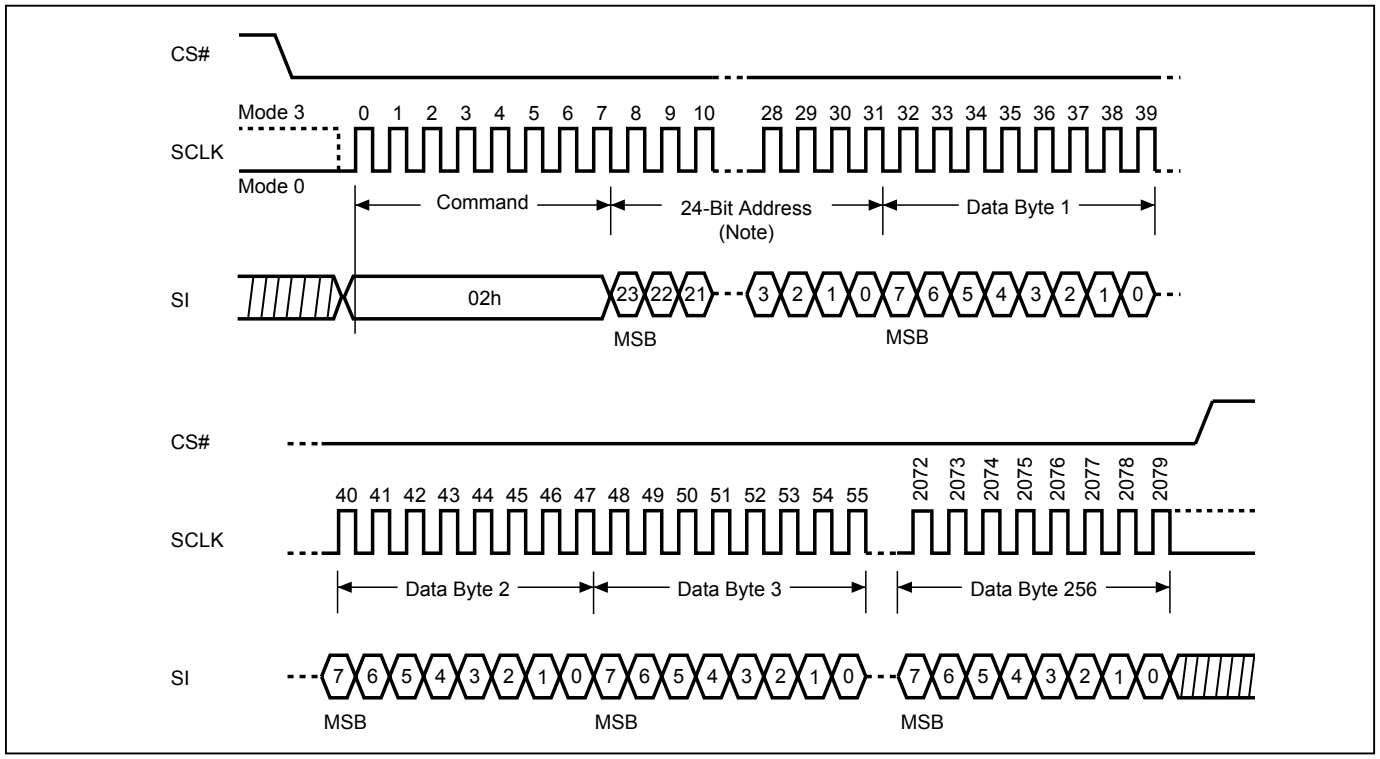
The sequence of issuing PP instruction is: CS# goes low→ send PP instruction code→ 3-byte or 4-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB (WPSEL=1; Individual Sector Protect Mode), the Page Program (PP) instruction will not be executed.

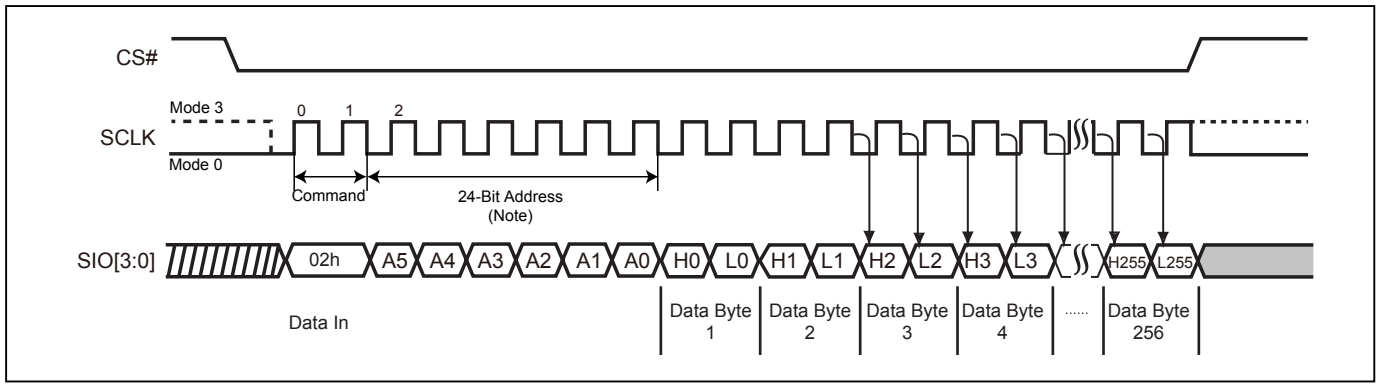
Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Figure 69. Page Program (PP) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 70. Page Program (PP) Sequence (QPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

9-29. 4 x I/O Page Program (4PP)

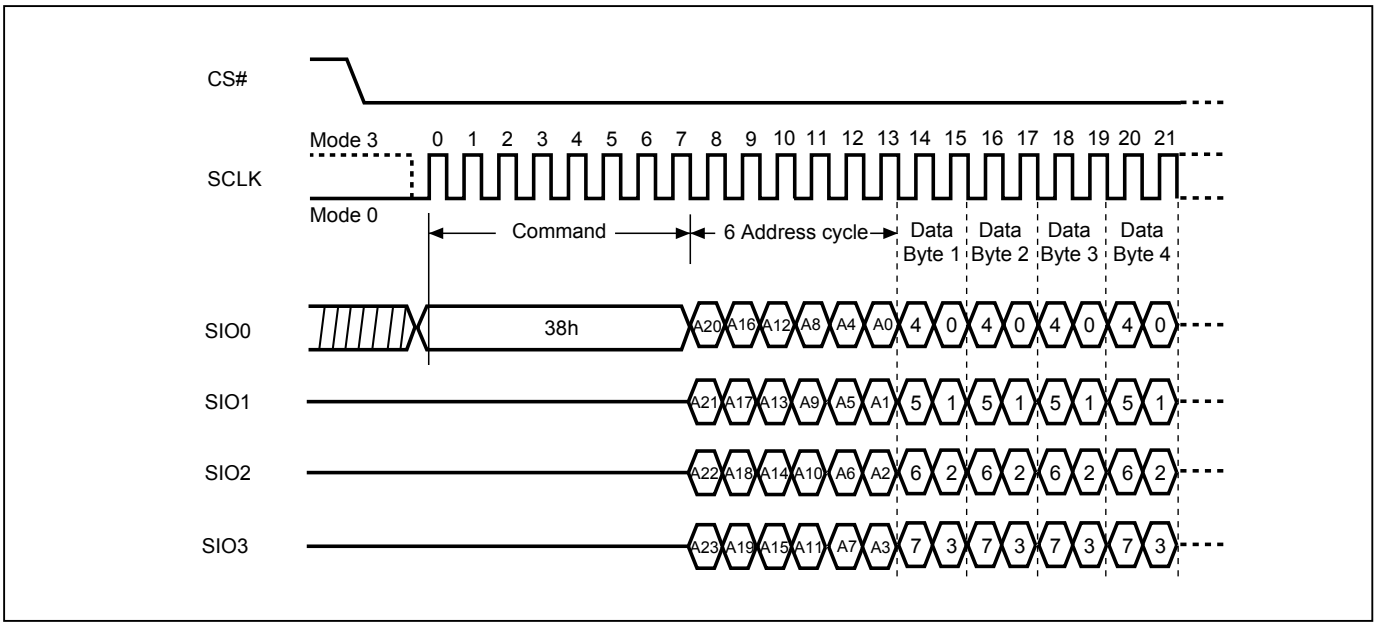
The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of application. The other function descriptions are as same as standard page program.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte address mode, please refer to the *"9-11. Enter 4-byte mode (EN4B)"* section.

The sequence of issuing 4PP instruction is: CS# goes low→ send 4PP instruction code→ 3-byte or 4-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→CS# goes high.

If the page is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB (WPSEL=1; Individual Sector Protect Mode), the Quad Page Program (4PP) instruction will not be executed.

Figure 71. 4 x I/O Page Program (4PP) Sequence (SPI Mode only)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

9-30. Deep Power-down (DP)

The Deep Power-down (DP) instruction places the device into a minimum power consumption state, Deep Power-down mode, in which the quiescent current is reduced from ISB1 to ISB2.

The sequence of issuing DP instruction: CS# goes low→ send DP instruction code→ CS# goes high. The CS# must go high at the byte boundary (after exactly eighth bits of the instruction code have been latched-in); otherwise the instruction will not be executed. Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. SIO[3:1] are "don't care".

After CS# goes high there is a delay of tDP before the device transitions from Stand-by mode to Deep Power-down mode and before the current reduces from ISB1 to ISB2. Once in Deep Power-down mode, all instructions will be ignored except Release from Deep Power-down (RDP).

The device exits Deep Power-down mode and returns to Stand-by mode if it receives a Release from Deep Power-down (RDP) instruction, power-cycle, or reset.

Figure 72. Deep Power-down (DP) Sequence (SPI Mode)

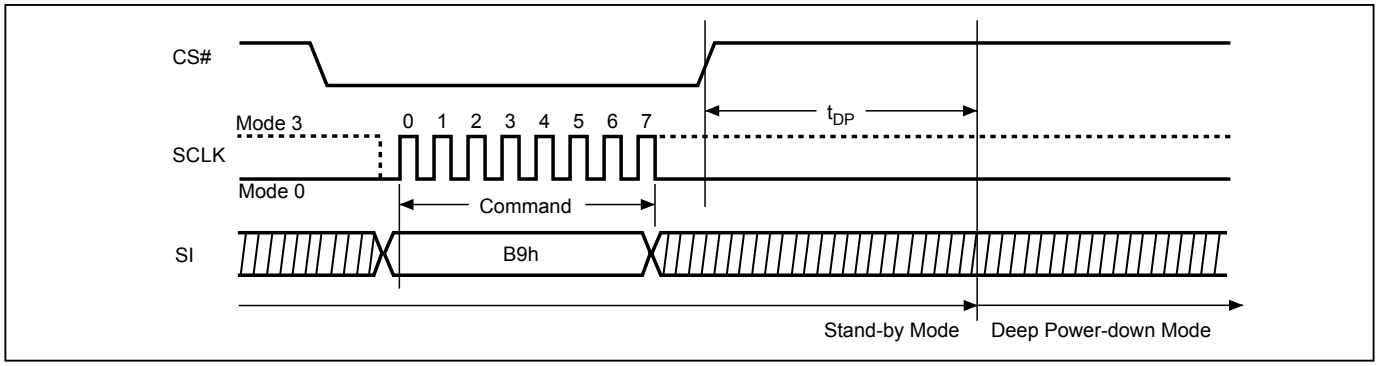
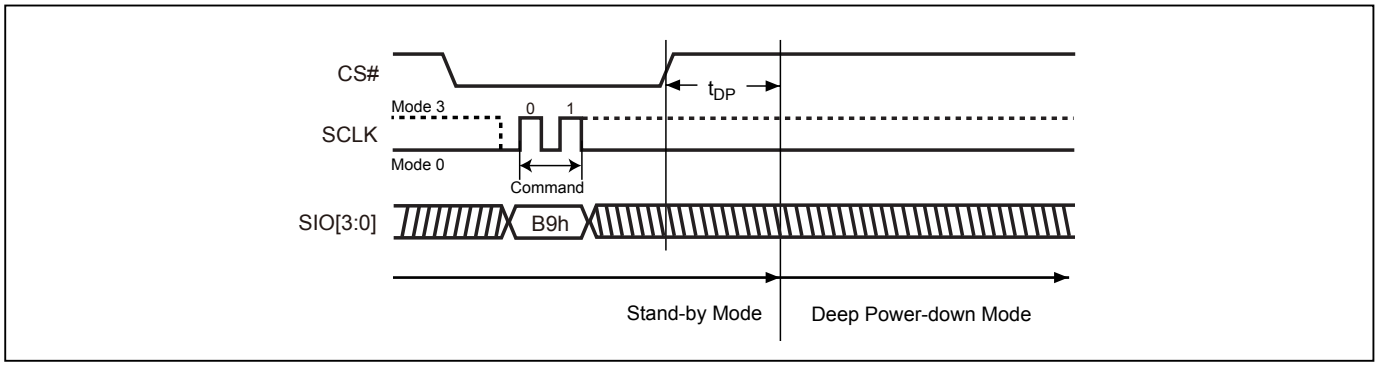


Figure 73. Deep Power-down (DP) Sequence (QPI Mode)



9-31. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 4K-bit secured OTP mode. While device is in 4K-bit secured OTPmode, main array access is not available. The additional 4K-bit secured OTP is independent from main array and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ send ENSO instruction to enter Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Please note that after issuing ENSO command user can only access secure OTP region with standard read or program procedure. Furthermore, once security OTP is lock down, only read related commands are valid.

9-32. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 4K-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ send EXSO instruction to exit Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

9-33. Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 8K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is: CS# goes low→ send WRSCUR instruction → CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

Figure 74. Write Security Register (WRSCUR) Sequence (SPI Mode)

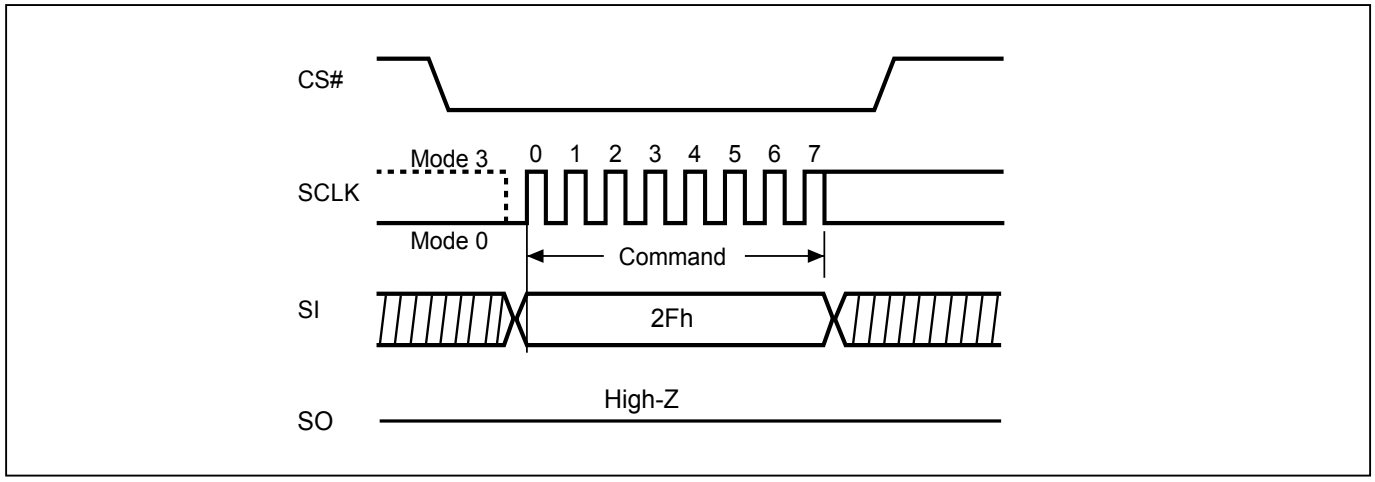
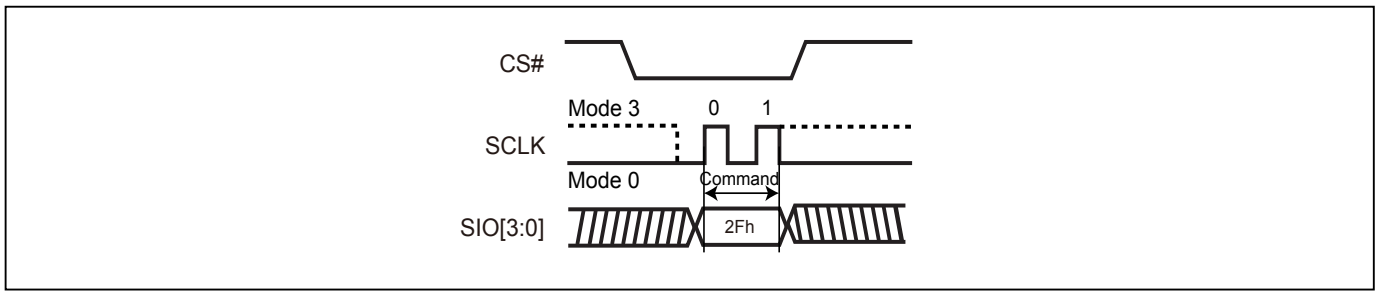


Figure 75. Write Security Register (WRSCUR) Sequence (QPI Mode)



9-34. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is: CS# goes low→send RDSCUR instruction→Security Register data out on SO→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Figure 76. Read Security Register (RDSCUR) Sequence (SPI Mode)

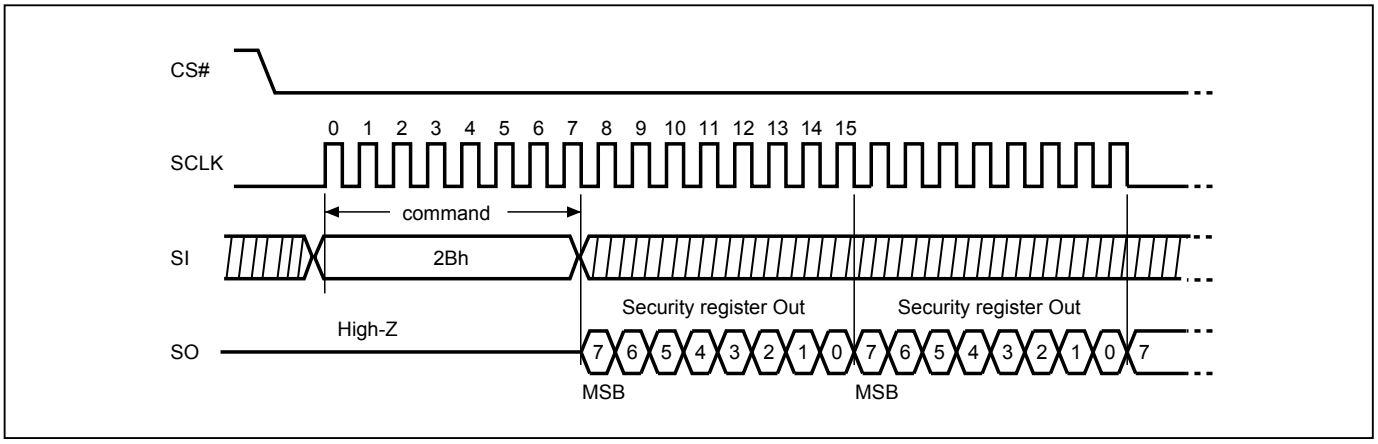
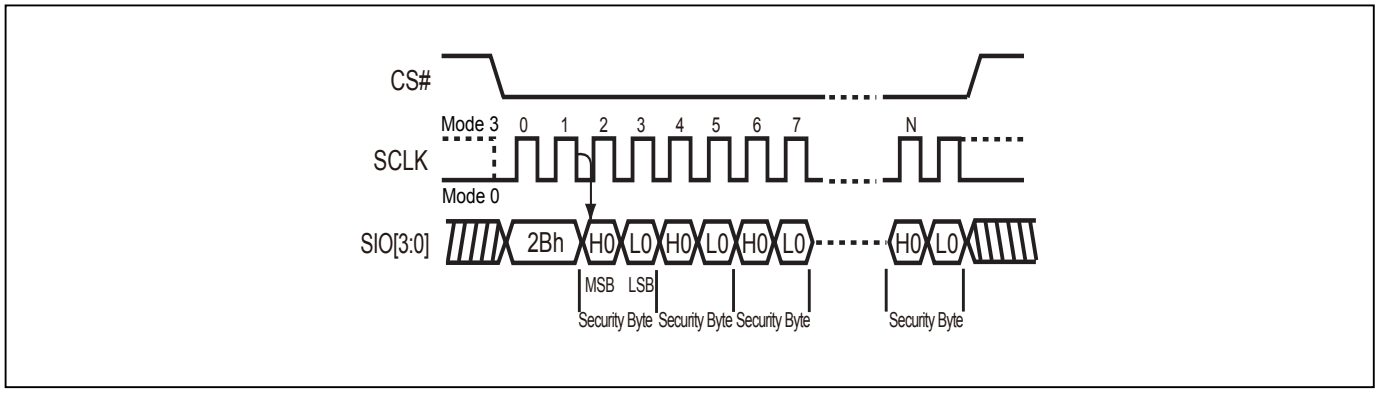


Figure 77. Read Security Register (RDSCUR) Sequence (QPI Mode)



Security Register

The definition of the Security Register bits is as below:

Write Protection Selection bit. Please reference to *"9-35. Write Protection Selection (WPSEL)"*.

Erase Fail bit. The Erase Fail bit indicates the status of last Erase operation. The bit will be set to "1" if the erase operation failed or the erase region is protected. It will be automatically cleared to "0" if the next erase operation succeeds. Please note that it does not interrupt or stop any operation in the flash memory.

Program Fail bit. The Program Fail bit indicates the status of last Program operation. The bit will be set to "1" if the program operation failed or the program region is protected. It will be automatically cleared to "0" if the next program operation succeeds. Please note that it does not interrupt or stop any operation in the flash memory.

Erase Suspend bit. Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

Program Suspend bit. Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

Secured OTP Indicator bit. The Secured OTP indicator bit shows the 2nd 4K-bit Secured OTP area is locked by factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 1st 4K-bit Secured OTP area cannot be updated any more. While it is in 8K-bit secured OTP mode, main array access is not allowed.

Table 12. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WPSEL	E_FAIL	P_FAIL	Reserved	ESB (Erase Suspend bit)	PSB (Program Suspend bit)	LDSO (lock-down 1st 4K-bit Secured OTP)	Secured OTP Indicator bit (2nd 4K-bit Secured OTP)
0=Block Lock (BP) protection mode 1=Individual Sector protection mode (default=0)	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	-	0=Erase is not suspended 1= Erase suspended (default=0)	0=Program is not suspended 1= Program suspended (default=0)	0 = not lock-down 1 = lock-down (Secured OTP can no longer be programmed)	0= nonfactory lock 1= factory lock
Non-volatile bit (OTP)	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Non-volatile bit (OTP)	Non-volatile bit (OTP)

9-35. Write Protection Selection (WPSEL)

There are two write protection methods provided on this device, (1) Block Protection (BP) mode or (2) Individual Sector Protection mode. The protection modes are mutually exclusive. The WPSEL bit selects which protection mode is enabled. If WPSEL=0 (factory default), BP mode is enabled and Individual Sector Protection mode is disabled. If WPSEL=1, Individual Sector Protection mode is enabled and BP mode is disabled. The WPSEL command is used to set WPSEL=1. A WREN command must be executed to set the WEL bit before sending the WPSEL command. Please note that the WPSEL bit is an OTP bit. Once WPSEL is set to "1", it cannot be programmed back to "0".

When WPSEL = 0: Block Lock (BP) protection mode,
The memory array is write protected by the BP3~BP0 bits.

When WPSEL =1: Individual Sector protection mode,
Blocks are individually protected by their own SPB or DPB. On power-up, all blocks are write protected by the Dynamic Protection Bits (DPB) by default. The Individual Sector Protection instructions WRLR, RDLR, WRSPB, ESSPB, WRDPB, RDDPB, GBLK, and GBULK are activated. The BP3~BP0 bits of the Status Register are disabled and have no effect. Hardware protection is performed by driving WP#=0. Once WP#=0 all blocks and sectors are write protected regardless of the state of each SPB or DPB.

The sequence of issuing WPSEL instruction is: CS# goes low → send WPSEL instruction to enable the Individual Sector Protect mode → CS# goes high.

Figure 78. Write Protection Selection

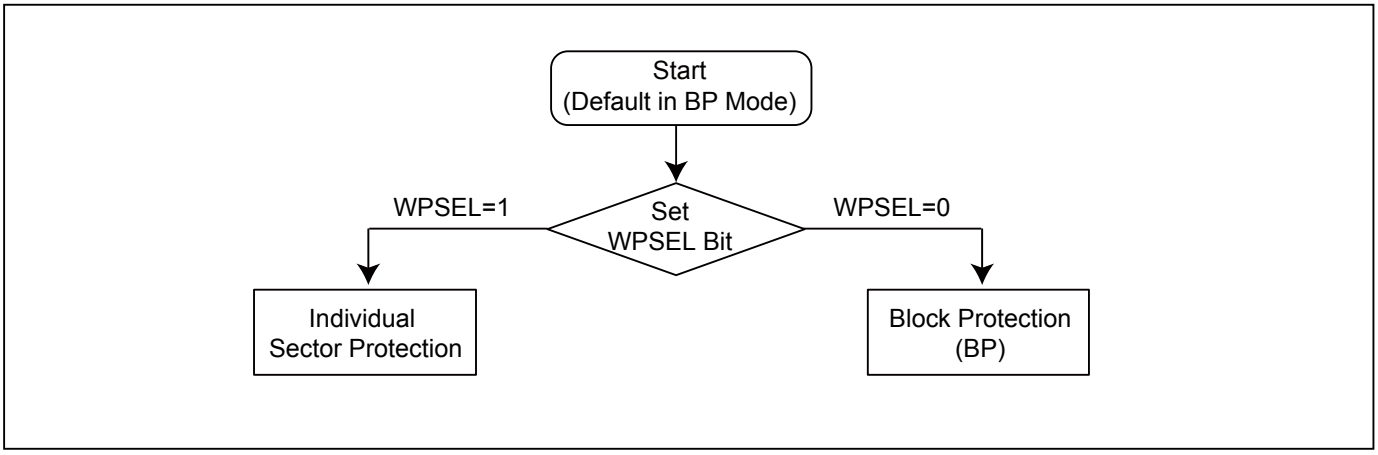
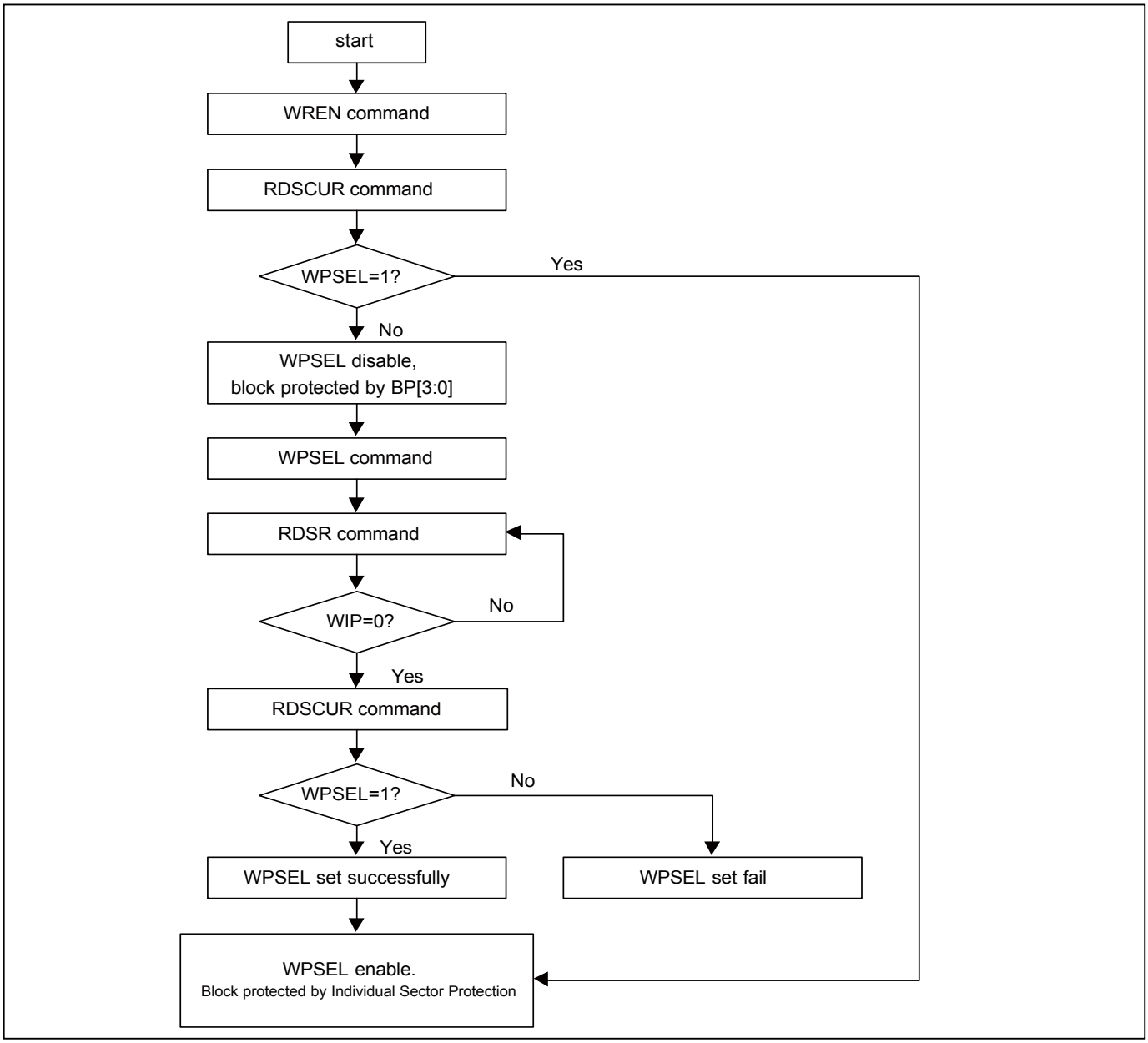


Figure 79. WPSEL Flow



9-36. Advanced Sector Protection

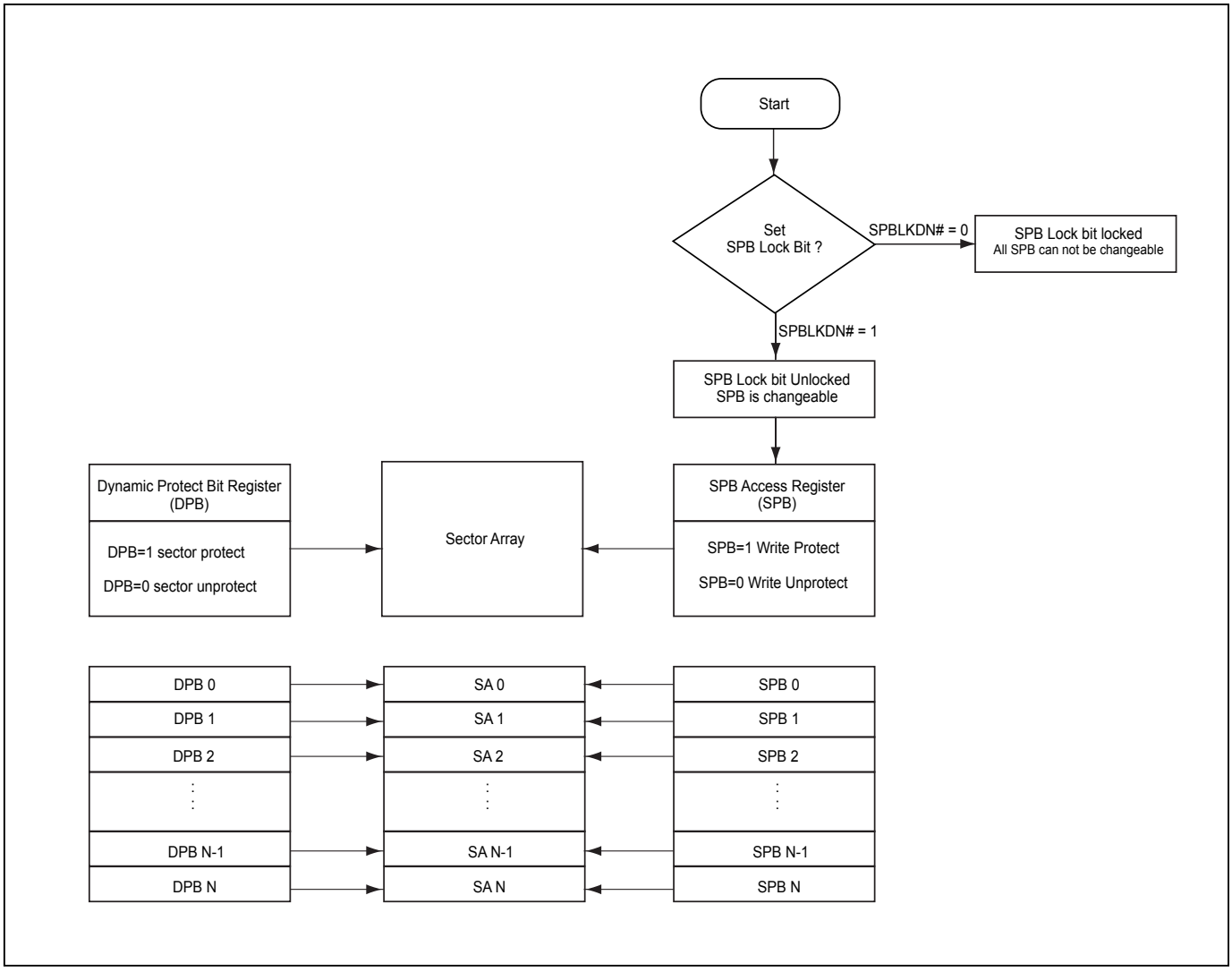
Advanced Sector Protection can protect individual 4KB sectors in the bottom and top 64KB of memory and protect individual 64KB blocks in the rest of memory.

There is one non-volatile Solid Protection Bit (SPB) and one volatile Dynamic Protection Bit (DPB) assigned to each 4KB sector at the bottom and top 64KB of memory and to each 64KB block in the rest of memory. A sector or block is write-protected from programming or erasing when its associated SPB or DPB is set to “1”. Please refer to *"9-36-5. Sector Protection States Summary Table"* for the sector state with the protection status of DPB/SPB bits.

The figure below helps describing an overview of these methods. The device is default to the Solid mode when shipped from factory. The detail algorithm of advanced sector protection is shown as follows:

Solid Protection mode permits the SPB bits to be modified after power-on or a reset. The figure below is an overview of Advanced Sector Protection.

Figure 80. Advanced Sector Protection Overview



9-36-1. Lock Register

The Lock Register is a 16-bit one-time programmable register. Lock Register bit [6] is SPB Lock Down Bit (SPBLKDN) which is an unique bit assigned to control all SPB bit status.

When SPBLKDN is 1, SPB can be changed. When it is locked as 0, all SPB can not be changed anymore, and SPBLKDN bit itself can not be altered anymore, either.

The Lock Register is programmed using the WRLR (Write Lock Register) command. A WREN command must be executed to set the WEL bit before sending the WRLR command.

Table 13. Lock Register

Bits	Field Name	Function	Type	Default State	Description
15 to 7	RFU	Reserved	OTP	1	Reserved for Future Use
6	SPBLKDN	SPB Lock Down	OTP	1	1 = SPB changeable 0 = freeze SPB
5 to 0	RFU	Reserved	OTP	1	Reserved for Future Use

Figure 81. Read Lock Register (RDLR) Sequence (SPI Mode only)

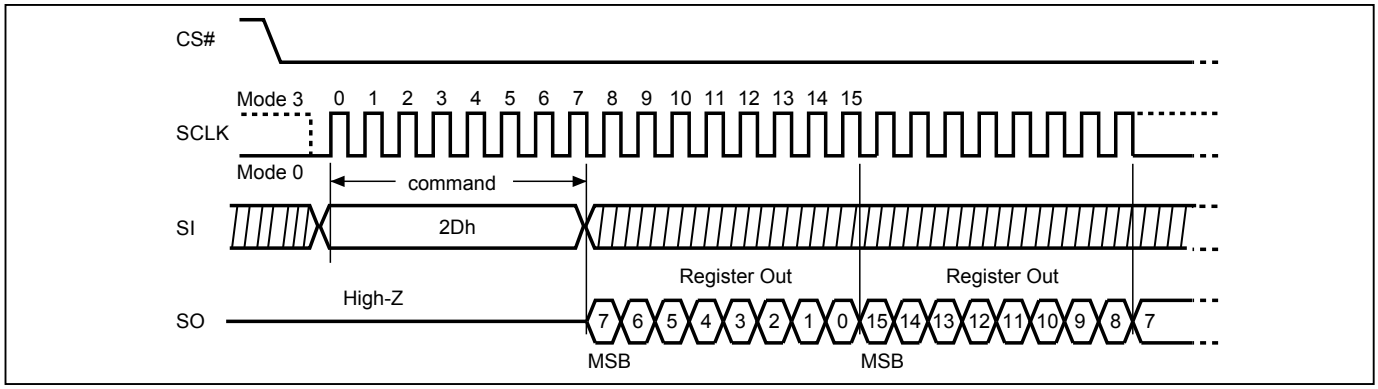
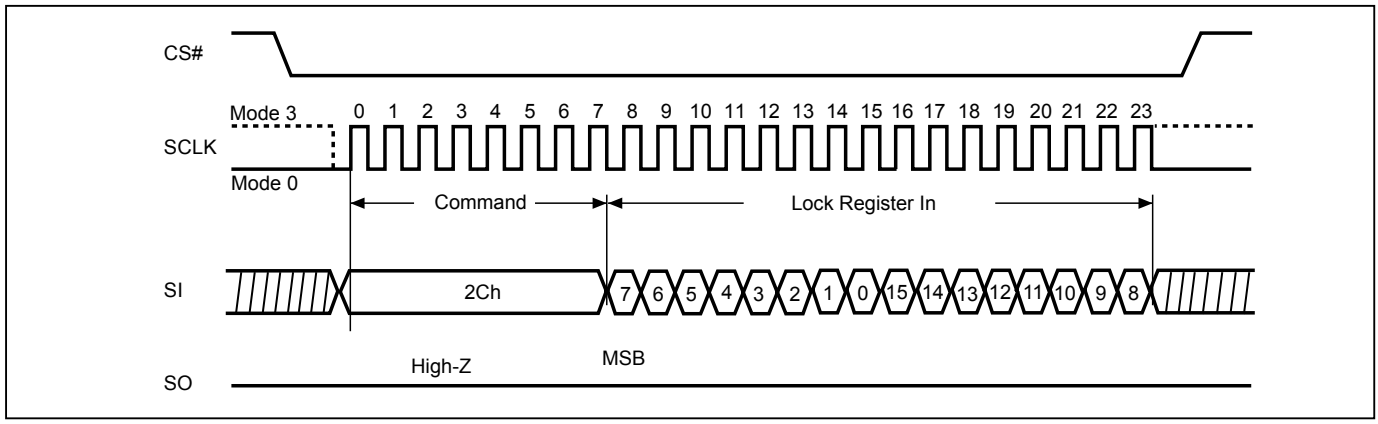


Figure 82. Write Lock Register (WRLR) Sequence (SPI Mode only)



9-36-2. Solid Protection Bits

The Solid Protection Bits (SPBs) are nonvolatile bits for enabling or disabling write-protection to sectors and blocks. The SPB bits have the same endurance as the Flash memory. An SPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the remaining memory. The factory default state of the SPB bits is “0”, which has the sector/block write-protection disabled.

When an SPB is set to “1”, the associated sector or block is write-protected. Program and erase operations on the sector or block will be inhibited. SPBs can be individually set to “1” by the WRSPB command. However, the SPBs cannot be individually cleared to “0”. Issuing the ESSPB command clears all SPBs to “0”. A WREN command must be executed to set the WEL bit before sending the WRSPB or ESSPB command.

The RDSPB command reads the status of the SPB of a sector or block. The RDSPB command returns 00h if the SPB is “0”, indicating write-protection is disabled. The RDSPB command returns FFh if the SPB is “1”, indicating write-protection is enabled.

Note: If SPBLKDN=0, commands to set or clear the SPB bits will be ignored.

Table 14. SPB Register

Bit	Description	Bit Status	Default	Type
7 to 0	SPB (Solid Protection Bit)	00h = Unprotect Sector / Block FFh = Protect Sector / Block	00h	Non-volatile

Figure 83. Read SPB Status (RDSPB) Sequence (SPI Mode only)

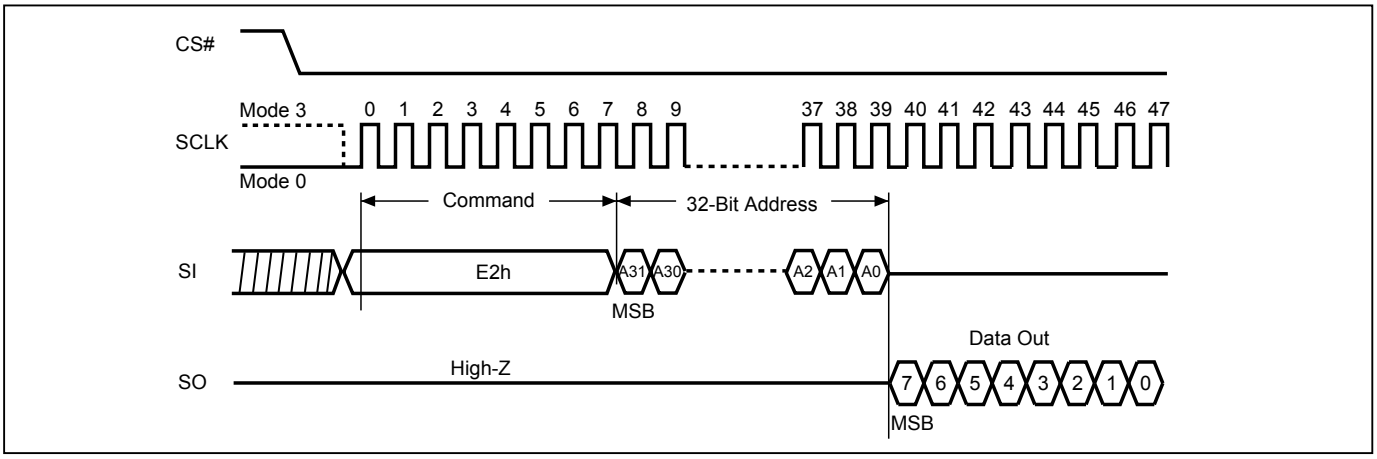


Figure 84. SPB Erase (ESSPB) Sequence (SPI Mode only)

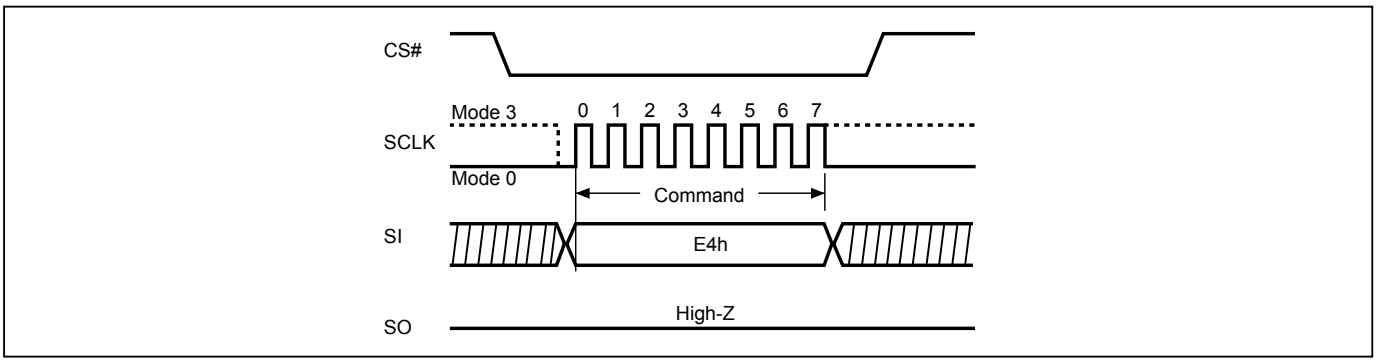
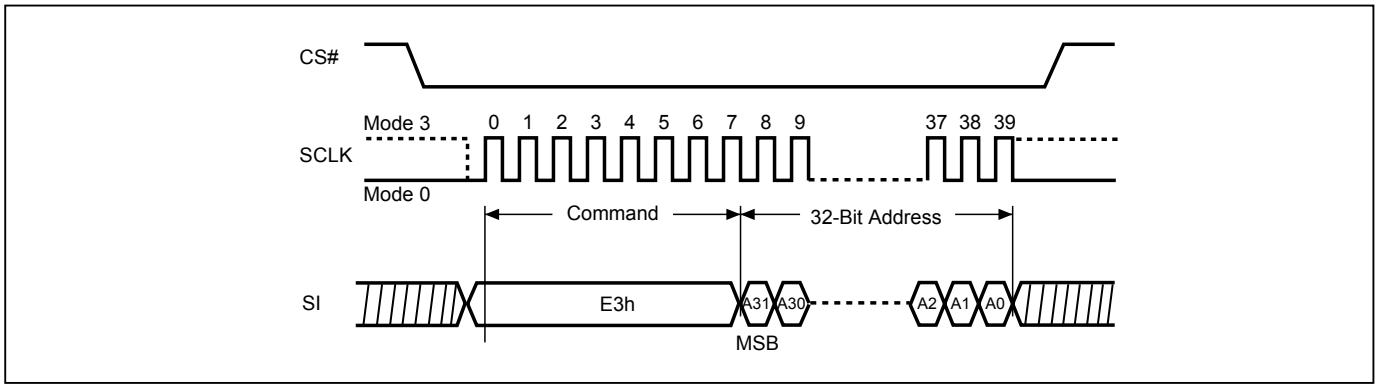


Figure 85. SPB Program (WRSPB) Sequence (SPI Mode only)



9-36-3. Dynamic Protection Bits

The Dynamic Protection Bits (DPBs) are volatile bits for quickly and easily enabling or disabling write-protection to sectors and blocks. A DPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the rest of the memory. The DBPs can enable write-protection on a sector or block regardless of the state of the corresponding SPB. However, the DPB bits can only unprotect sectors or blocks whose SPB bits are “0” (unprotected).

When a DPB is “1”, the associated sector or block will be write-protected, preventing any program or erase operation on the sector or block. All DPBs default to “1” after power-on or reset. When a DPB is cleared to “0”, the associated sector or block will be unprotected if the corresponding SPB is also “0”.

DPB bits can be individually set to “1” or “0” by the WRDPB command. The DBP bits can also be globally cleared to “0” with the GBULK command or globally set to “1” with the GBLK command. A WREN command must be executed to set the WEL bit before sending the WRDPB, GBULK, or GBLK command.

The RDDPB command reads the status of the DPB of a sector or block. The RDDPB command returns 00h if the DPB is “0”, indicating write-protection is disabled. The RDDPB command returns FFh if the DPB is “1”, indicating write-protection is enabled.

Table 15. DPB Register

Bit	Description	Bit Status	Default	Type
7 to 0	DPB (Dynamic Protection Bit)	00h = Unprotect Sector / Block FFh = Protect Sector / Block	FFh	Volatile

Figure 86. Read DPB Register (RDDPB) Sequence (SPI Mode only)

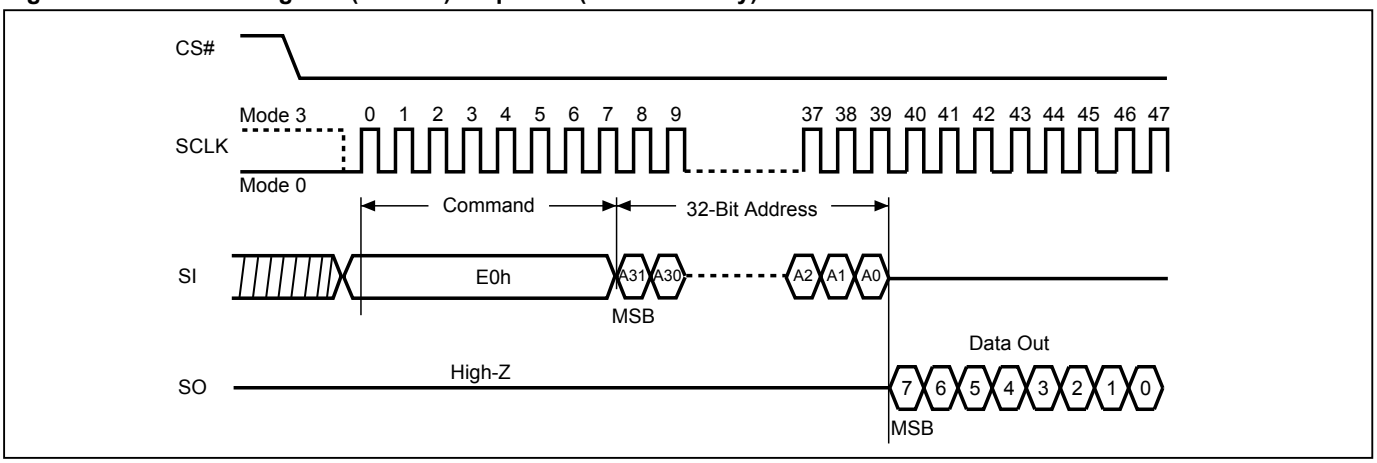
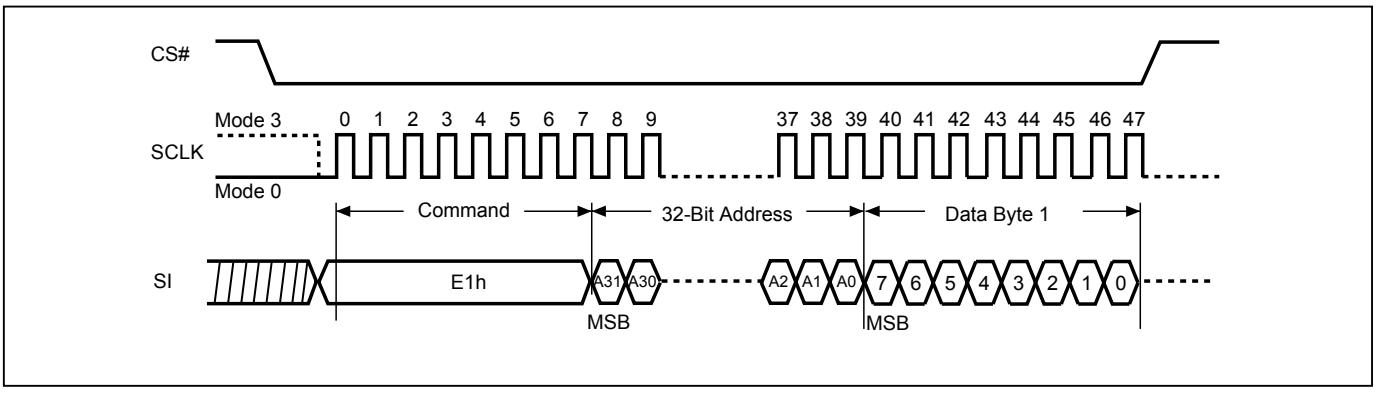


Figure 87. Write DPB Register (WRDPB) Sequence (SPI Mode only)



9-36-4. Gang Block Lock/Unlock (GBLK/GBULK)

These instructions are only effective if WPSEL=1. The GBLK and GBULK instructions provide a quick method to set or clear all DPB bits at once.

The WREN (Write Enable) instruction is required before issuing the GBLK/GBULK instruction.
The sequence of issuing GBLK/GBULK instruction is: CS# goes low → send GBLK/GBULK (7Eh/98h) instruction →CS# goes high.

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

9-36-5. Sector Protection States Summary Table

Protection Status		Sector/Block Protection State
DPB	SPB	
0	0	Unprotected
0	1	Protected
1	0	Protected
1	1	Protected

9-37. Program Suspend and Erase Suspend

The Suspend instruction interrupts a Page Program, Sector Erase, or Block Erase operation to allow access to the memory array.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

After the program or erase operation has entered the suspended state, the memory array can be read except for the page being programmed or the sector or block being erased (*"Table 16. Readable Area of Memory While a Program or Erase Operation is Suspended"*).

Table 16. Readable Area of Memory While a Program or Erase Operation is Suspended

Suspended Operation	Readable Region of Memory Array
Page Program	All but the Page being programmed
Sector Erase (4KB)	All but the 4KB Sector being erased
Block Erase (32KB)	All but the 32KB Block being erased
Block Erase (64KB)	All but the 64KB Block being erased

When the Serial NOR Flash receives the Suspend instruction, there is a latency of tPSL or tESL (*"Figure 88. Suspend to Read Latency"*) before the Write Enable Latch (WEL) bit clears to “0” and the PSB or ESB sets to “1”, after which the device is ready to accept one of the commands listed in *"Table 17. Acceptable Commands During Program/Erase Suspend after tPSL/tESL"* (e.g. FAST READ). Refer to *"Table 26. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 2.7V - 3.6V)"* for tPSL and tESL timings.

"Table 18. Acceptable Commands During Suspend (tPSL/tESL not required)" lists the commands for which the tPSL and tESL latencies do not apply. For example, RDSR, RDSCUR, RSTEN, and RST can be issued at any time after the Suspend instruction.

Security Register bit 2 (PSB) and bit 3 (ESB) can be read to check the suspend status (please refer to *"Table 12. Security Register Definition"*). The PSB (Program Suspend Bit) sets to “1” when a program operation is suspended. The ESB (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The PSB or ESB clears to “0” when the program or erase operation is resumed.

Figure 88. Suspend to Read Latency

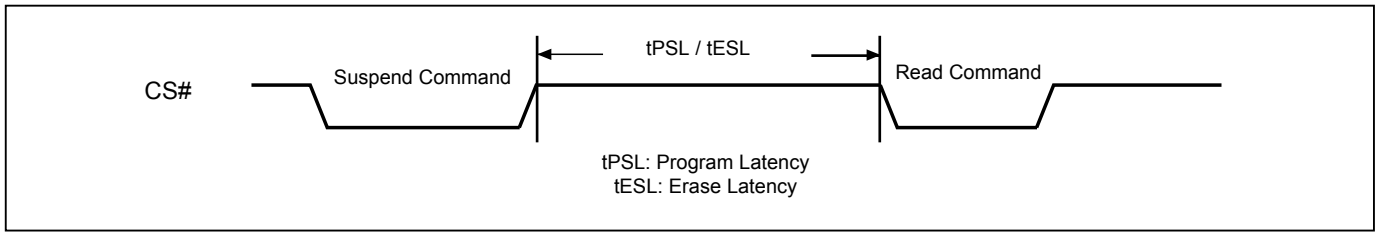


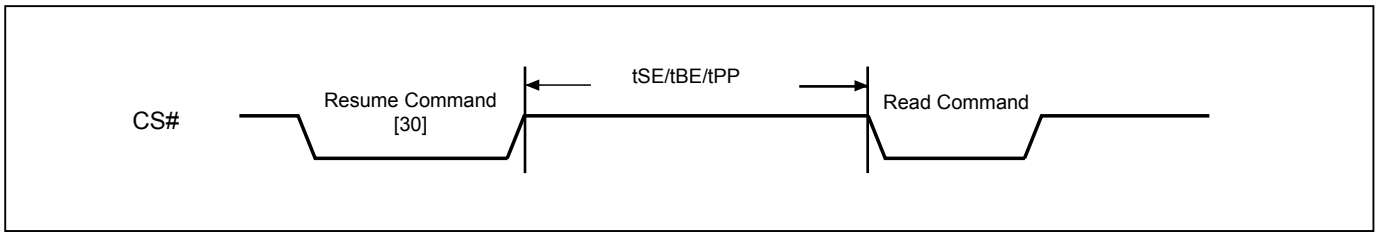
Table 17. Acceptable Commands During Program/Erase Suspend after tPSL/tESL

Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
READ	03h	•	•
FAST READ	0Bh	•	•
DREAD	3Bh	•	•
QREAD	6Bh	•	•
2READ	BBh	•	•
4READ	EBh	•	•
4DTRD	EDh	•	•
RDSFDP	5Ah	•	•
RDID	9Fh	•	•
RDSPB	E2h	•	•
RDDPB	E0h	•	•
QPIID	AFh	•	•
REMS	90h	•	•
ENSO	B1h	•	•
EXSO	C1h	•	•
WREN	06h	•	•
EQIO	35h	•	•
RSTQIO	F5h	•	•
RESUME	30h	•	•
SBL	C0h	•	•

Table 18. Acceptable Commands During Suspend (tPSL/tESL not required)

Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
WRDI	04h	•	•
RDSR	05h	•	•
RDCR	15h	•	•
RDSCUR	2Bh	•	•
RDLR	2Dh	•	•
RES	ABh	•	•
RSTEN	66h	•	•
RST	99h	•	•
NOP	00h	•	•

Figure 89. Resume to Read Latency



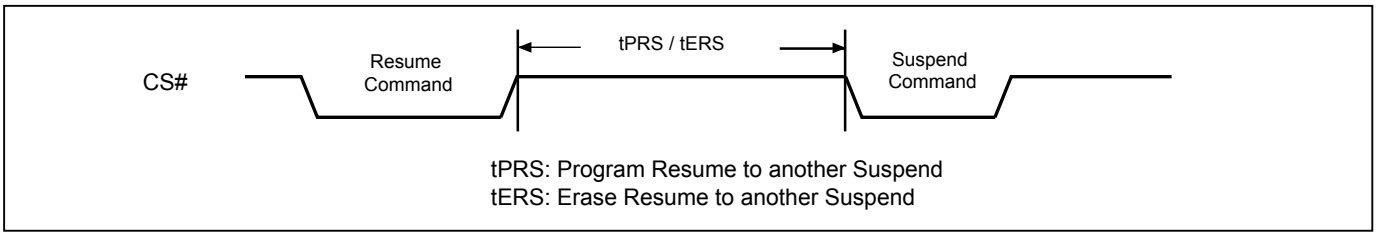
9-38. Program Resume and Erase Resume

The Resume instruction resumes a suspended Page Program, Sector Erase, or Block Erase operation. Before issuing the Resume instruction to restart a suspended erase operation, make sure that there is no Page Program operation in progress.

Immediately after the Serial NOR Flash receives the Resume instruction, the WEL and WIP bits are set to “1” and the PSB or ESB is cleared to “0”. The program or erase operation will continue until finished (*"Figure 89. Resume to Read Latency"*) or until another Suspend instruction is received. A resume-to-suspend latency of tPRS or tERS must be observed before issuing another Suspend instruction (*"Figure 90. Resume to Suspend Latency"*).

Please note that the Resume instruction will be ignored if the Serial NOR Flash is in “Performance Enhance Mode”. Make sure the Serial NOR Flash is not in “Performance Enhance Mode” before issuing the Resume instruction.

Figure 90. Resume to Suspend Latency



9-39. No Operation (NOP)

The “No Operation” command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

9-40. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

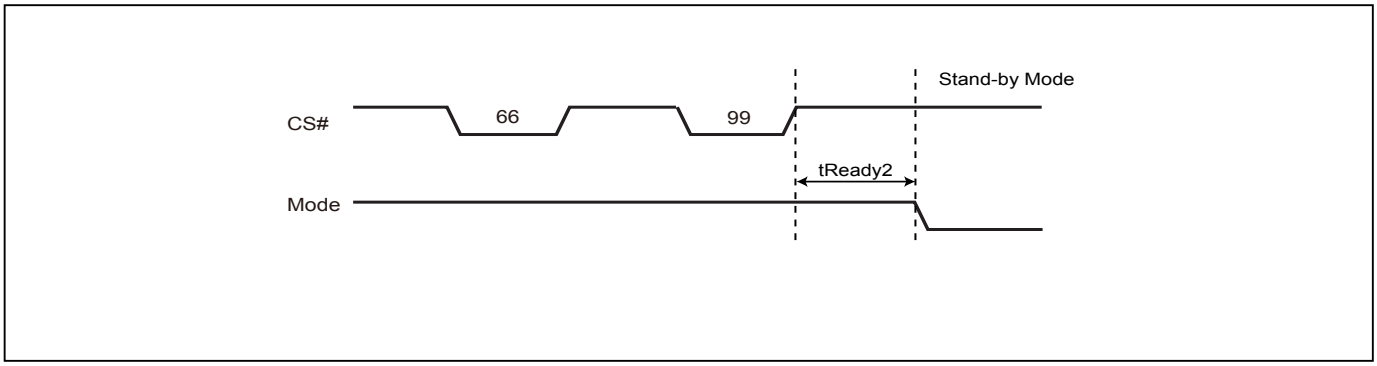
To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. For details, please refer to *"Table 21. Reset Timing-(Other Operation)"* for tREADY2.

Figure 91. Software Reset Recovery



Note: Refer to *"Table 21. Reset Timing-(Other Operation)"* for tREADY2 data.

Figure 92. Reset Sequence (SPI mode)

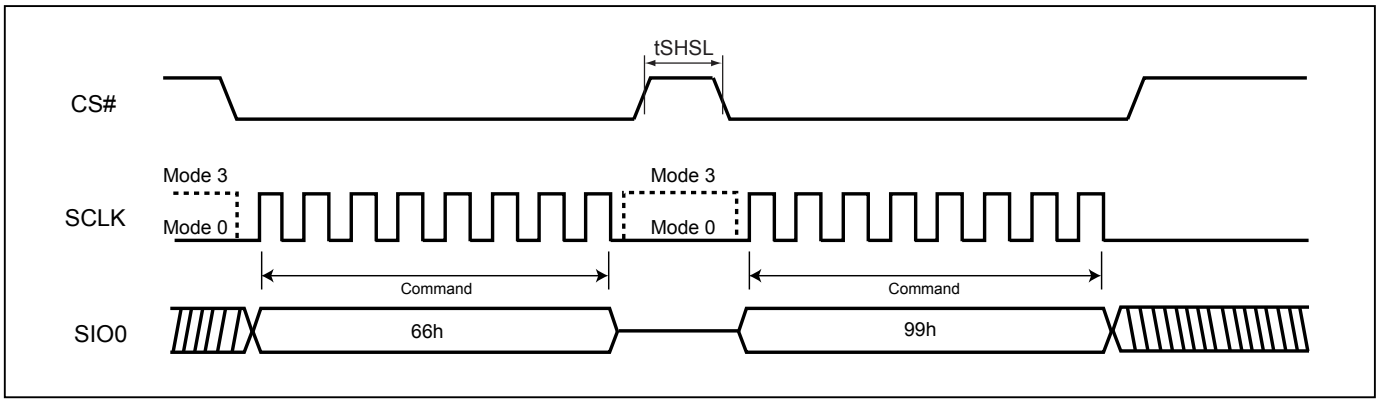
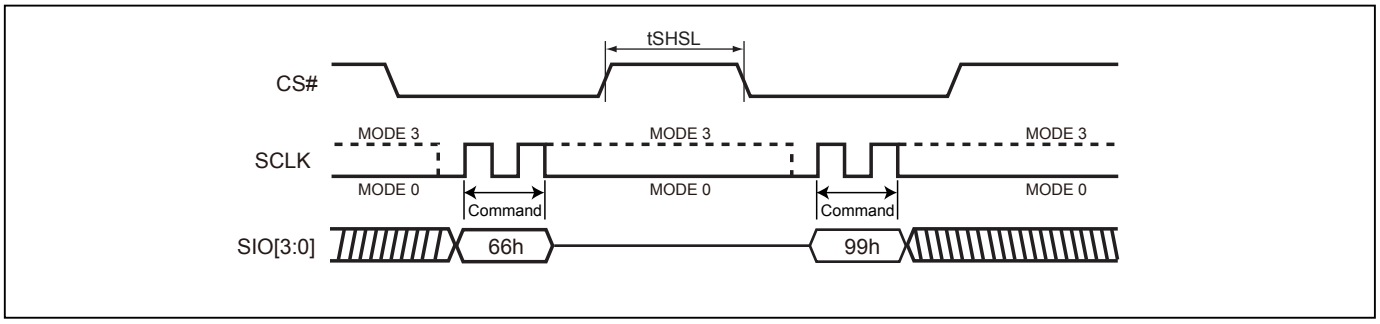


Figure 93. Reset Sequence (QPI mode)



9-41. Read SFDP Mode (RDSFDP)

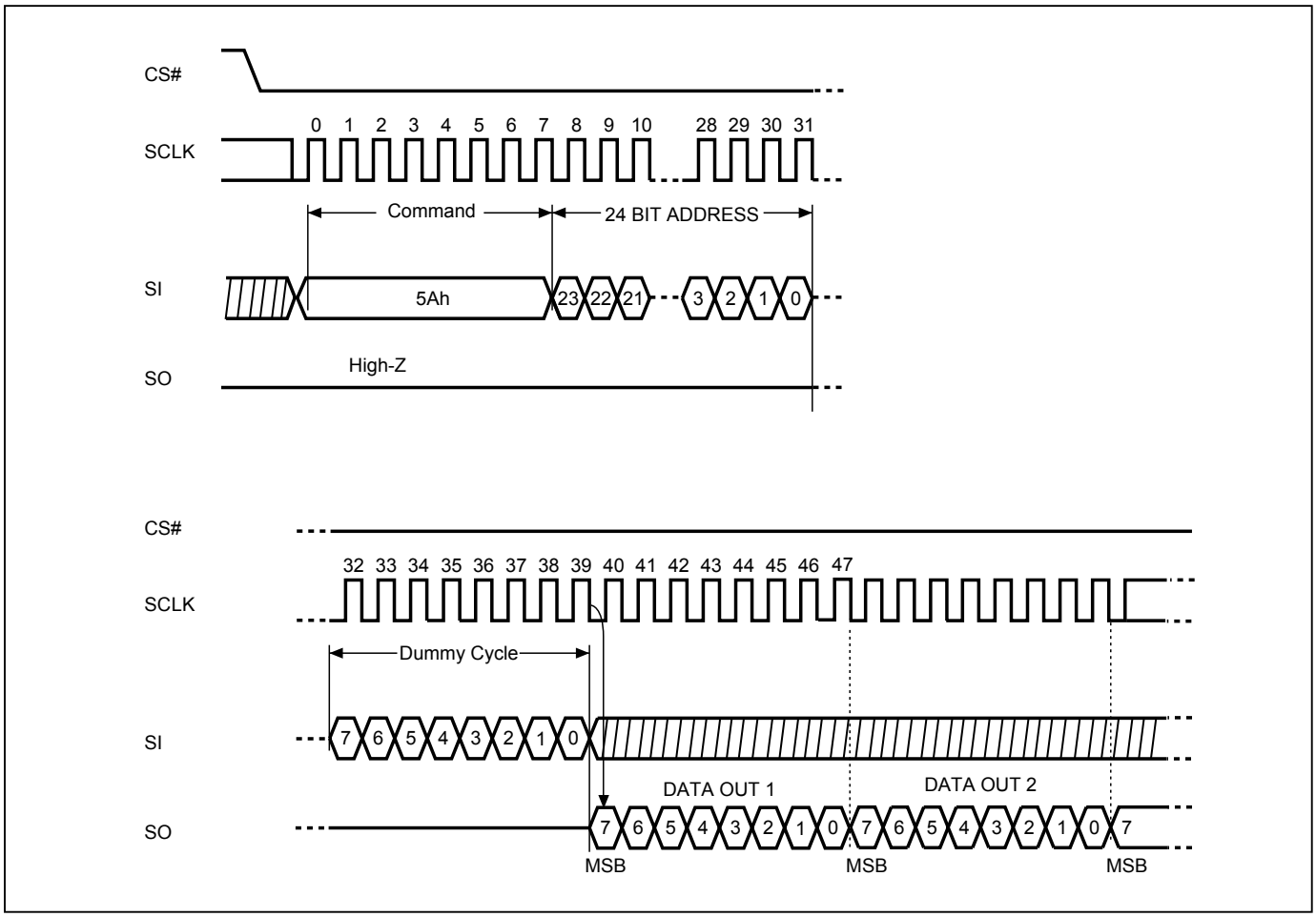
The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation, drive CS# high at any time during data out.

SFDP is a JEDEC standard, JESD216B.

For SFDP register values detail, please contact local Macronix sales channel for Application Note.

Figure 94. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence



9-42. ECC (Error Correction Code)

The ECC algorithm uses a Hamming code that can correct a single bit error per 16-byte chunk. The internal state machine will automatically generate the ECC during a page program operation and automatically correct bit errors during a read operation. The chunks are 16-byte aligned within a 256 byte page as shown in *"Table 19. 16-Byte Chunks within a Page"*.

It is recommended that data be programmed in full 256-byte pages. If writing less than a full page, it is recommended that data be programmed in multiples of 16-byte chunks instead of a byte or a word at a time. If writing less than 16 bytes to a chunk, it is recommended that the data be written with a single page program operation and that the chunk not be written again until after the 4k byte sector containing the chunk is erased.

ECC checking of a 16 byte chunk will be disabled if the chunk has been double programmed (i.e., a subsequent page program operation has modified any byte of the chunk). Once ECC checking on a chunk is disabled, ECC checking for the chunk will not be re-activated until the 4K-byte sector containing the chunk is erased. Data integrity is highest when ECC is enabled. If internal ECC is disabled, the data integrity of the chunk may be compromised.

Table 19. 16-Byte Chunks within a Page

Chunk#	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16 Bytes	B0 ~B15	B16 ~B31	B32 ~B47	B48 ~B63	B64 ~B79	B80 ~B95	B96 ~B111	B112 ~B127	B128 ~B143	B144 ~B159	B160 ~B175	B176 ~B191	B192 ~B207	B208 ~B223	B224 ~B239	B240 ~B255

10. RESET

Driving the RESET# pin low for a period of tRLRH or longer will reset the device. After the reset cycle, the device is in the following states:
- Standby mode
- All the volatile bits such as WEL/WIP/SRAM lock bit will return to the default status as power on.
- 3-byte address mode

If the device is under programming or erasing, driving the RESET# pin low will also terminate the operation and data could be lost. During the resetting cycle, the SO data becomes high impedance and the current will be reduced to minimum.

While Reset operation is during erase suspend, no matter what status the flash device is in, its Reset Recovery time should be referred to the Recovery time of the Erase activity in progress.

Figure 95. RESET Timing

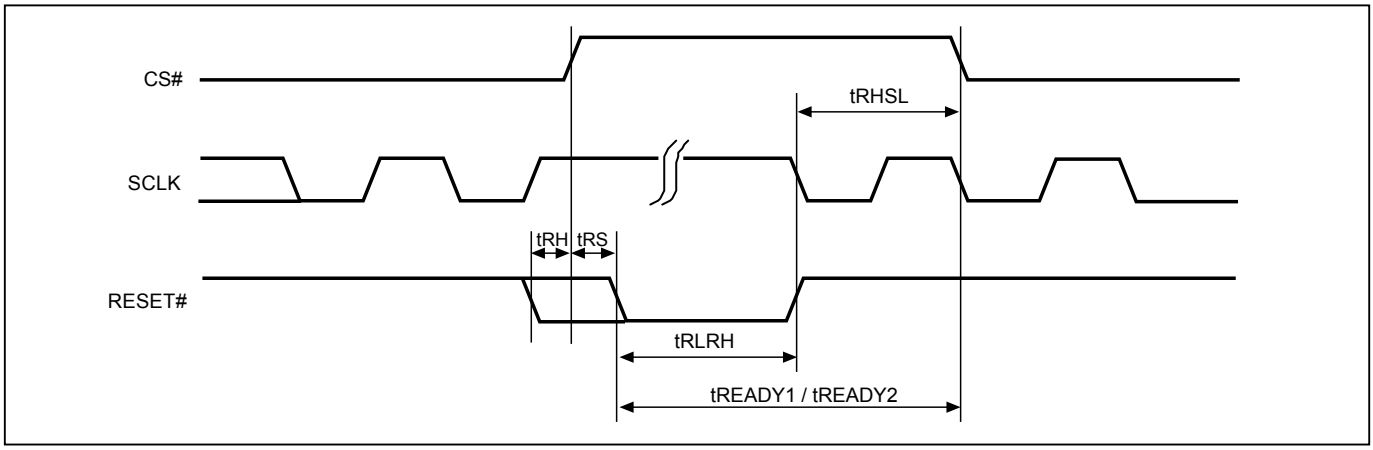


Table 20. Reset Timing-(Power On)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	15			ns
tRH	Reset# hold time	15			ns
tRLRH	Reset# low pulse width	10			us
tREADY1	Reset Recovery time	35			us

Table 21. Reset Timing-(Other Operation)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	15			ns
tRH	Reset# hold time	15			ns
tRLRH	Reset# low pulse width	10			us
tREADY2	Reset Recovery time (During instruction decoding)	40			us
	Reset Recovery time (for read operation)	35			us
	Reset Recovery time (for program operation)	310			us
	Reset Recovery time(for SE4KB operation)	12			ms
	Reset Recovery time (for BE64KB/BE32KB operation)	25			ms
	Reset Recovery time (for Chip Erase operation)	100			ms
	Reset Recovery time (for WRSR operation)	40			ms

Note: For the Reset activity during Erase suspend, its tREADY2 timing should be referred to the Erase activity in progress.

10-1. In-Band-Reset

In-Band RESET is JEDEC-JESD252.01 compliance, which specifies a signaling protocol to perform a hardware reset by using only the CS#, SCLK, and the SI pin without a dedicated hardware RESET# pin.

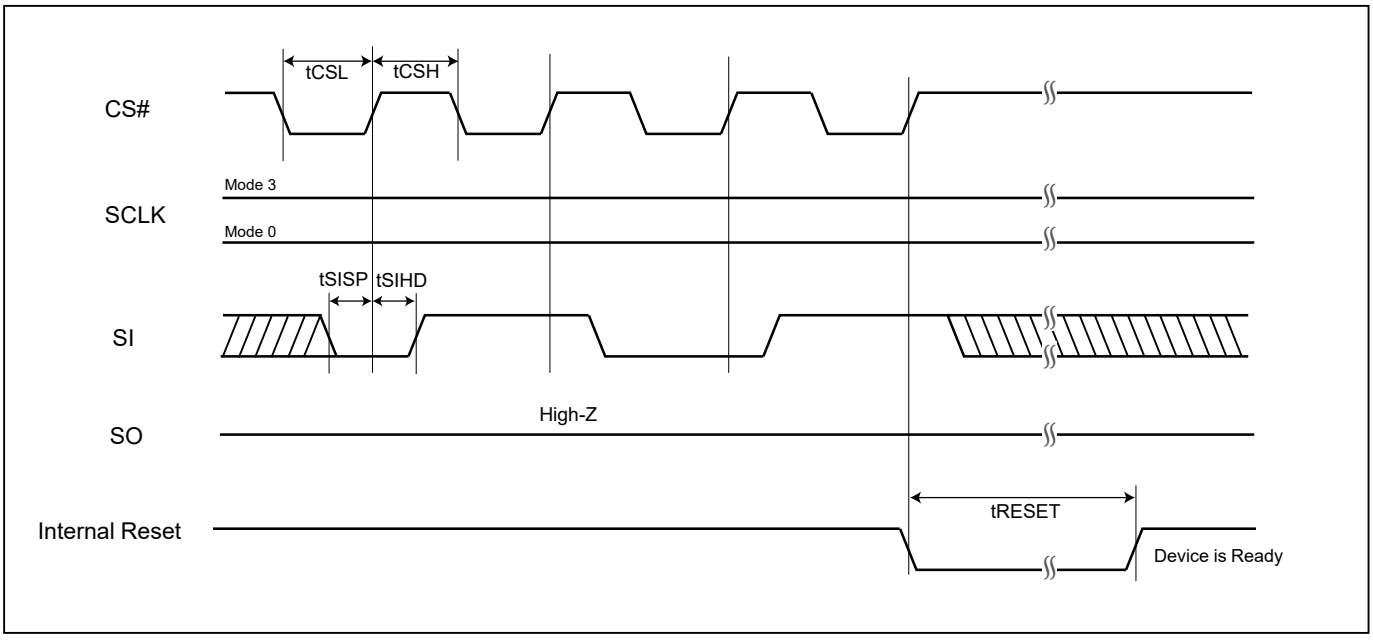
The procedure of initiating the reset request is: CS# goes low → SCLK remains stable in either a high or low state → SI pin goes low by the host, simultaneously with CS# going low → CS# goes high.

After the fourth CS# pulse, the flash device triggers its internal reset. Please note that SI is low on the first CS# pulse, high on the second CS# pulse, low on the third CS# pulse, high on the fourth CS# pulse. This provides a 5h pattern to differentiate it from random noise.

Table 22. In-Band-Reset Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
tCSL	CS# Low hold Time	500			ns
tCSH	CS# High hold time	500			ns
tSISP	Serial Data Input Setup Time	5			ns
tSIHD	Serial Data Input Hold Time	5			ns
tRESET	RESET Recovery Time			100	ms

Figure 96. Reset Signaling Protocol



11. POWER-ON STATE

The device is in the states below when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage until the VCC reaches the following levels:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.
Please refer to the *"Figure 104. Power-up Timing"*.

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during this stage if a write, program, erase cycle is in progress.

12. ELECTRICAL SPECIFICATIONS

Table 23. ABSOLUTE MAXIMUM RATINGS

RATING		VALUE
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to 4.0V

NOTICE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+2.0V or -2.0V for period up to 20ns, and please refer to *"Figure 97. Maximum Negative Overshoot Waveform"* and *"Figure 98. Maximum Positive Overshoot Waveform"*.

Figure 97. Maximum Negative Overshoot Waveform

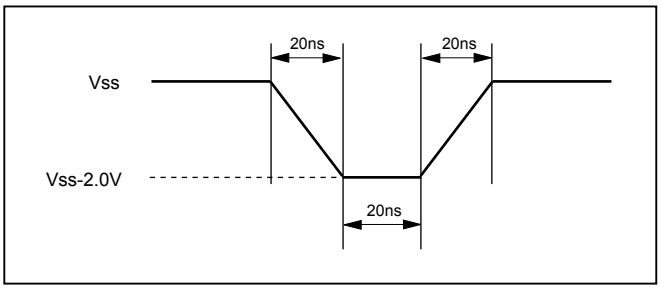


Figure 98. Maximum Positive Overshoot Waveform

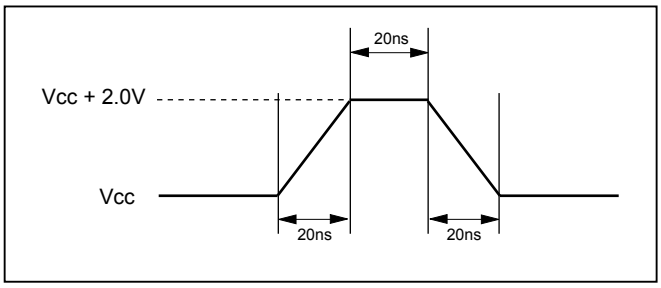


Table 24. CAPACITANCE TA = 25°C, f = 1.0 MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			35	pF	VIN = 0V
COUT	Output Capacitance			32	pF	VOUT = 0V

Figure 99. DATA INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL

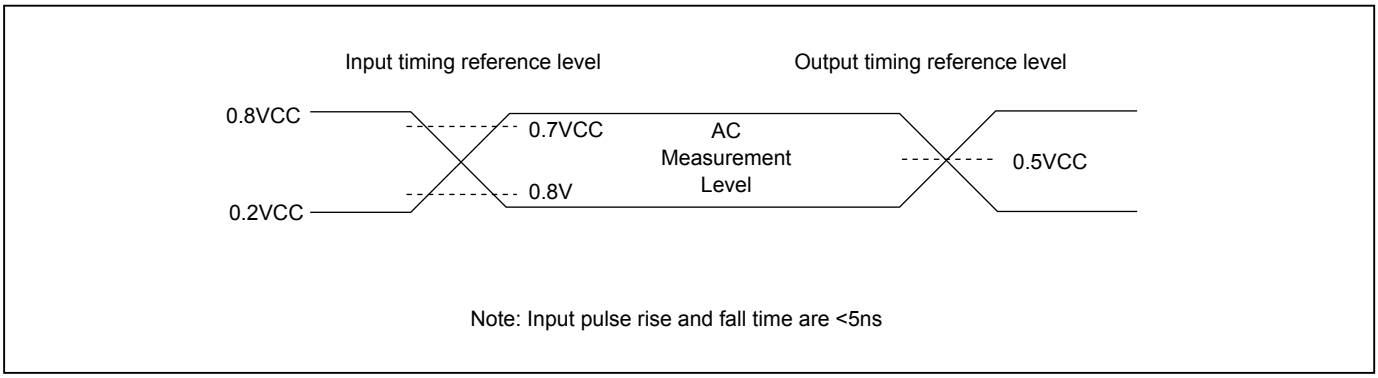


Figure 100. OUTPUT LOADING

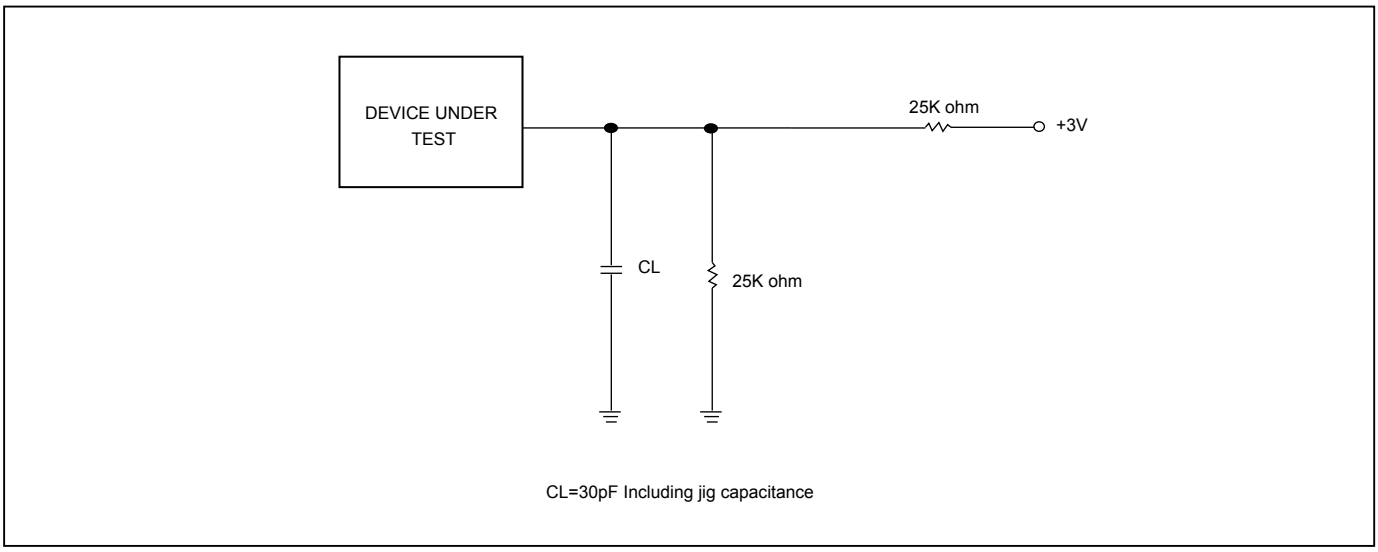


Figure 101. SCLK TIMING DEFINITION

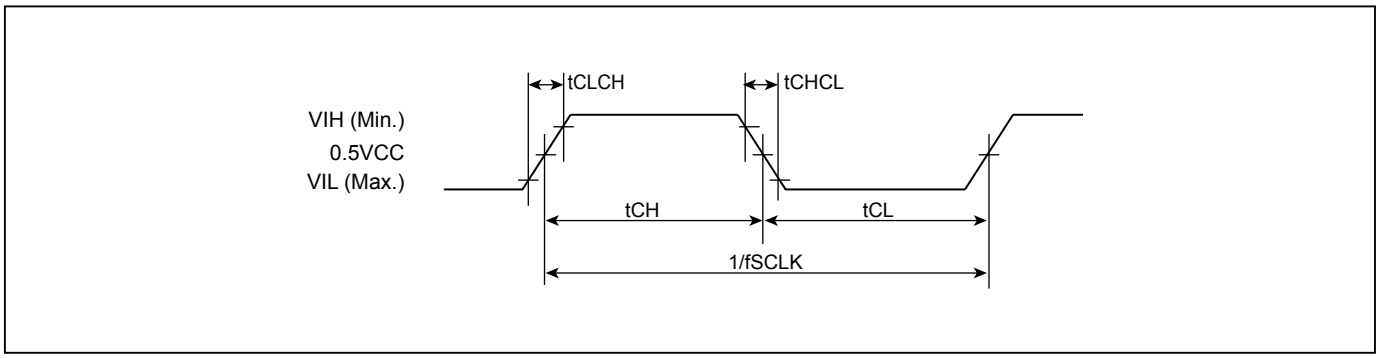


Table 25. DC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 2.7V - 3.6V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			±4	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			±4	uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		30	200	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			6	40	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1		28	50	mA	f=120MHz, (1I 2O read) SCLK=0.1VCC/0.9VCC, SO=Open
				24	40	mA	f=104MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				24	30	mA	f=84MHz, (DTR 4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		12	25	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			20	24	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector/Block (32K, 64K) Erase Current (SE/BE/BE32K)	1		10	25	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		28	50	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5		0.8	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.2	V	IOL = 100uA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes :

1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 26. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 2.7V - 3.6V)

Symbol	Alt.	Parameter			Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for all commands (except Read)			D.C.		120	MHz
fRSCLK	fR	Clock Frequency for READ instructions					50	MHz
fTSCLK	fT	Clock Frequency for 2READ/DREAD instructions			Please refer to *"Table 10. Dummy Cycle and Frequency Table (MHz)"*.			MHz
	fQ	Clock Frequency for 4READ/QREAD instructions						MHz
tCH(1)	tCLH	Clock High Time	Others (fSCLK/fTSCLK)	> 66MHz	45% x (1/fSCLK)			ns
				≤ 66MHz	7			ns
			Normal Read (fRSCLK)		7			ns
tCL(1)	tCLL	Clock Low Time	Others (fSCLK/fTSCLK)	> 66MHz	45% x (1/fSCLK)			ns
				≤ 66MHz	7			ns
			Normal Read (fRSCLK)		7			ns
tCLCH(5)		Clock Rise Time (peak to peak)			0.1			V/ns
tCHCL(5)		Clock Fall Time (peak to peak)			0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)			4			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)			4			ns
tDVCH/ tDVCL	tDSU	Data In Setup Time			2			ns
tCHDX/ tCLDX(9)	tDH	Data In Hold Time			2			ns
tCHSH		CS# Active Hold Time (relative to SCLK)			4			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)			4			ns
tSHSL	tCSH	CS# Deselect Time	From Read to next Read		7			ns
			From Write/Erase/Program to Read Status Register		30			ns
tSHQZ(5)	tDIS	Output Disable Time					8	ns
tCLQV(9)	tV	Clock Low to Output Valid Loading	Loading: 30pF				8	ns
			Loading: 15pF				6	ns
tCLQX(9)	tHO	Output Hold Time	Loading: 30pF		1			ns
			Loading: 15pF		1			ns
tWHSL(3)		Write Protect Setup Time			20			ns
tSHWL(3)		Write Protect Hold Time			100			ns
tDP(5)		CS# High to Deep Power-down Mode					10	us
tRES1(5)		CS# High to Standby Mode without Electronic Signature Read					30	us
tRES2(5)		CS# High to Standby Mode with Electronic Signature Read					30	us
tW		Write Status/Configuration Register Cycle Time					40	ms
tWREAW		Write Extended Address Register				40		ns
tPP		Page Program Cycle Time				0.25	1	ms
tSE		Sector Erase Cycle Time				30	400	ms
tBE32		Block Erase (32KB) Cycle Time				180	1000	ms
tBE		Block Erase (64KB) Cycle Time				380	2000	ms
tCE		Chip Erase Cycle Time				220	600	s
tESL(6)		Erase Suspend Latency					25	us
tPSL(6)		Program Suspend Latency					25	us
tPRS(7)		Latency between Program Resume and next Suspend			0.3	100		us
tERS(8)		Latency between Erase Resume and next Suspend			0.3	400		us
tQVD(9)		Data Output Valid Time Difference among all SIO pins					600	ps

Notes:

1. tCH + tCL must be greater than or equal to 1/Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
4. Test condition is shown as *"Figure 99. DATA INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL"* and *"Figure 100. OUTPUT LOADING"*.
5. The value guaranteed by characterization, not 100% tested in production.
6. Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".
7. For tPRS, minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.
8. For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.
9. Not 100% tested.

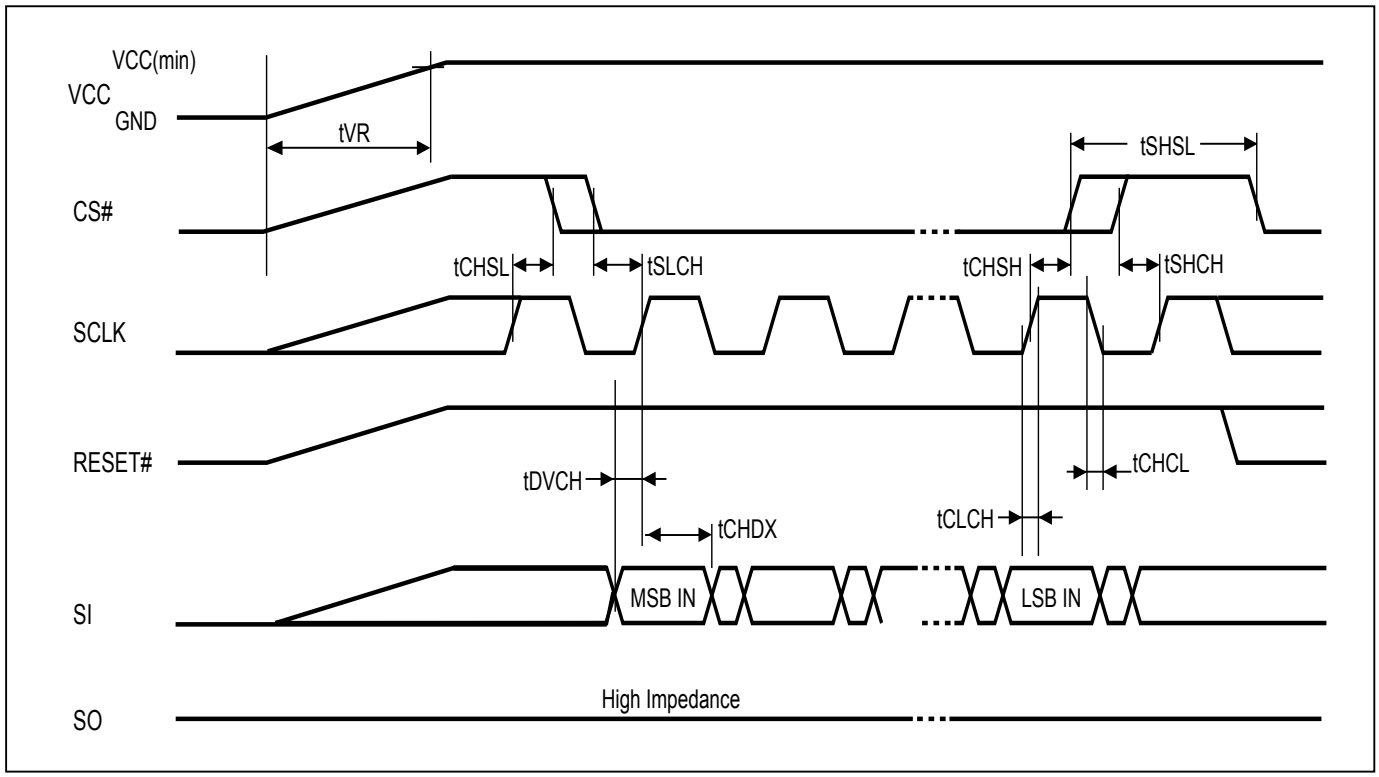
13. OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in *Figure 102* and *Figure 103* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 102. AC Timing at Device Power-Up



Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1		500000	us/V

Notes:
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *"Table 26. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 2.7V - 3.6V)"*.

Figure 103. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

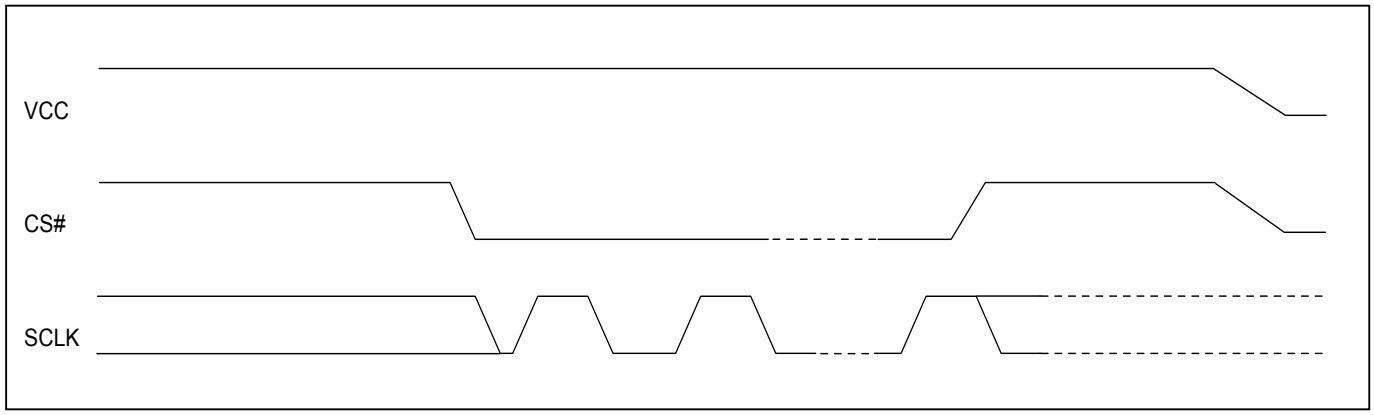


Figure 104. Power-up Timing

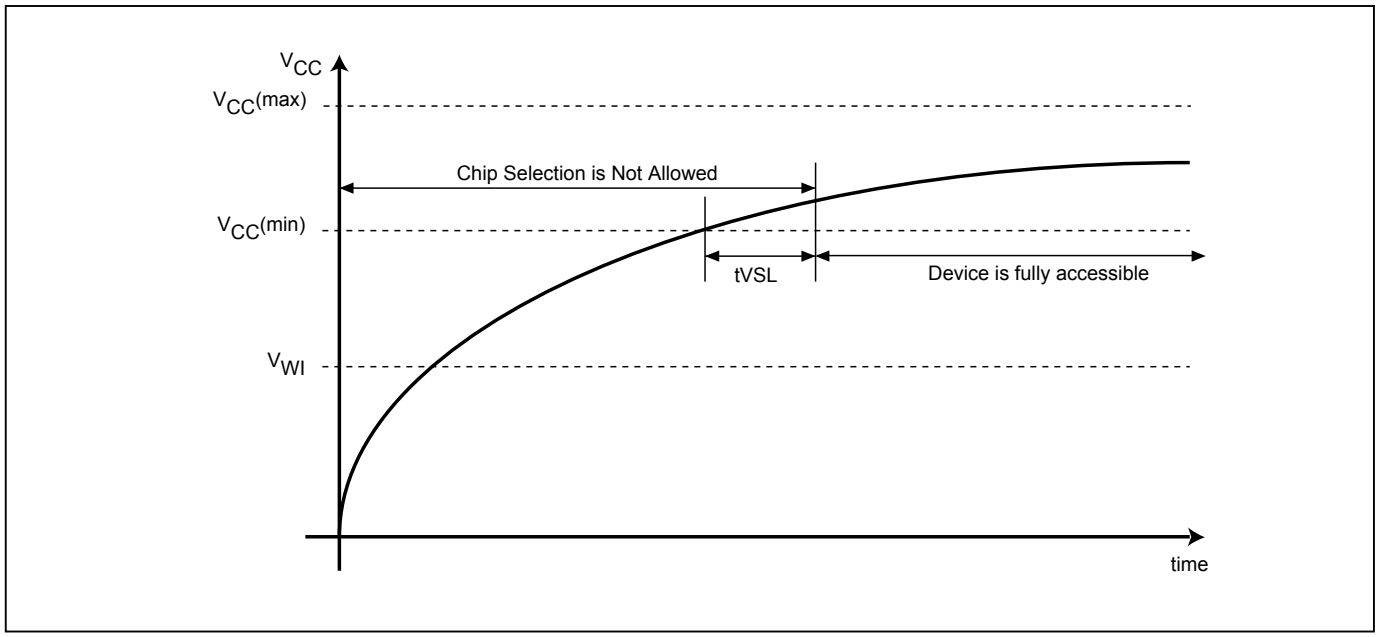


Figure 105. Power Up/Down and Voltage Drop

When powering down the device, VCC must drop below V_{PWD} for at least tPWD to ensure the device will initialize correctly during power up. Please refer to *"Figure 105. Power Up/Down and Voltage Drop"* and *"Table 27. Power-Up/Down Voltage and Timing"* below for more details.

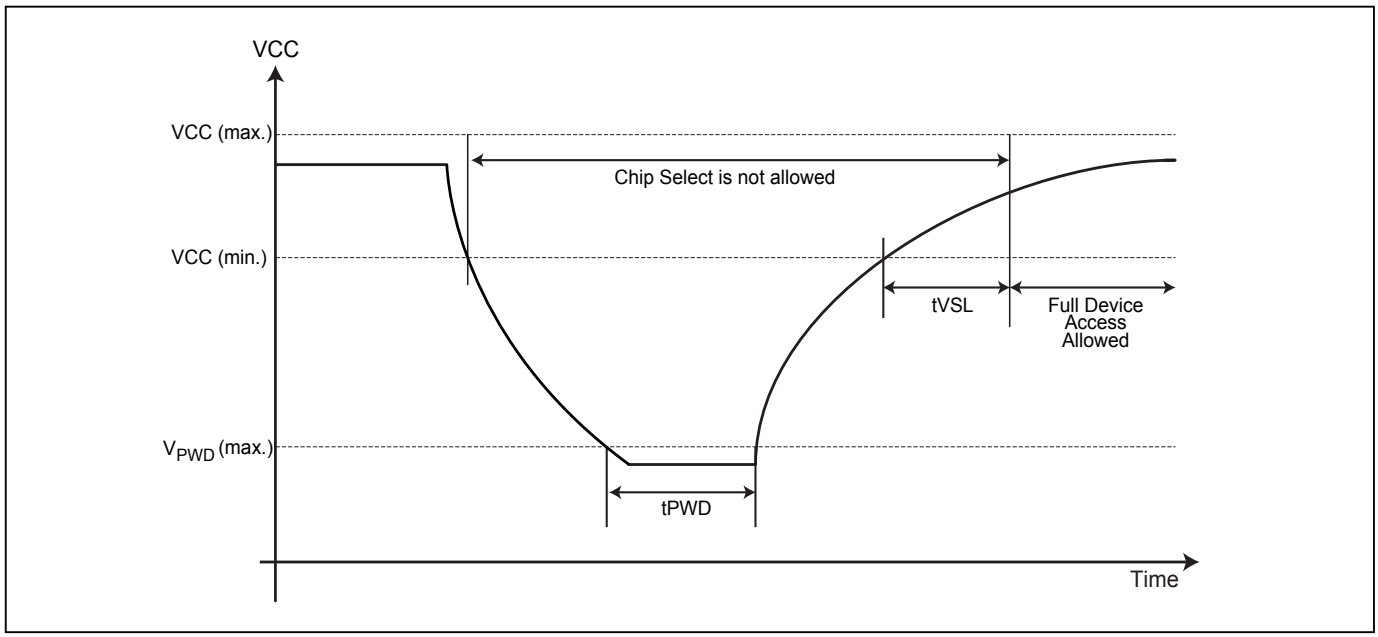


Table 27. Power-Up/Down Voltage and Timing

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC(min.) to device operation	6000		us
VWI	Write Inhibit Voltage	1.5	2.5	V
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initialization will occur		0.9	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVR	VCC Rise Time		500000	us/V
VCC	VCC Power Supply	2.7	3.6	V

Note: These parameters are characterized only.

13-1. INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

14. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Min.	Typ. (1)	Max. (2)	Unit
Write Status Register Cycle Time			40	ms
Sector Erase Cycle Time (4KB)		30	400	ms
Block Erase Cycle Time (32KB)		0.18	1	s
Block Erase Cycle Time (64KB)		0.38	2	s
Chip Erase Cycle Time		220	600	s
Page Program Time		0.25	1	ms
Erase/Program Cycle		100,000		cycles

Notes:
1. Typical program and erase time assumes the following conditions: 25°C, 3.3V, and all zero pattern.
2. Under worst conditions of 2.7V, highest operation temperature, post program/erase cycling.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.

15. ERASE AND PROGRAMMING PERFORMANCE (Factory Mode)

Parameter	Min.	Typ.	Max.	Unit
Sector Erase Cycle Time (4KB)		18		ms
Block Erase Cycle Time (32KB)		100		ms
Block Erase Cycle Time (64KB)		200		ms
Chip Erase Cycle Time		160		s
Page Program Time		0.16		ms
Erase/Program Cycle			50	cycles

Notice:
1. Factory Mode must be operated in 20°C to 45°C and VCC 3.0V-3.6V.
2. In Factory mode, the Erase/Program operation should not exceed 50 cycles, and "ERASE AND PROGRAMMING PERFORMANCE" 100k cycles will not be affected.
3. During factory mode, Suspend command (B0h) cannot be executed.

16. DATA RETENTION

Parameter	Condition	Min.	Max.	Unit
Data retention	55˚C	20		years

17. LATCH-UP CHARACTERISTICS

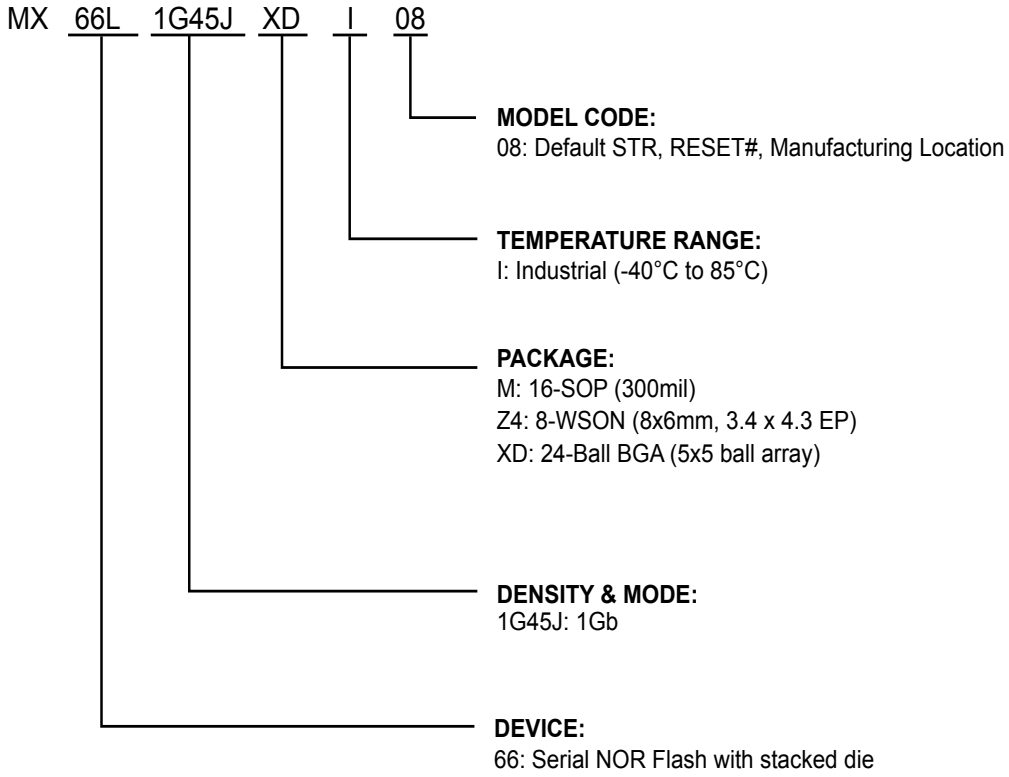
	Min.	Max.
Input Voltage with respect to GND on all power pins		1.5 VCCmax
Input Current on all non-power pins	-100mA	+100mA
Test conditions: VCC = VCCmax, one pin at a time (compliant to JEDEC JESD78 standard).		

18. ORDERING INFORMATION

Please contact Macronix regional sales for the latest product selection and available form factors.

PART NO.	Package	Temp.	I/O Configuration			H/W Configuration	Remark
			CS#	Default I/O	Dummy Cycle	H/W Pin	
MX66L1G45JMI08	16-SOP (300mil)	-40°C to 85°C	1 Pin	Standard	Standard	Reset#	Support Factory Mode
MX66L1G45JZ4I08	8-WSON (8x6mm, 3.4 x 4.3 EP)	-40°C to 85°C	1 Pin	Standard	Standard	Reset#	Support Factory Mode
MX66L1G45JXDI08	24-Ball BGA (5x5 ball array)	-40°C to 85°C	1 Pin	Standard	Standard	Reset#	Support Factory Mode

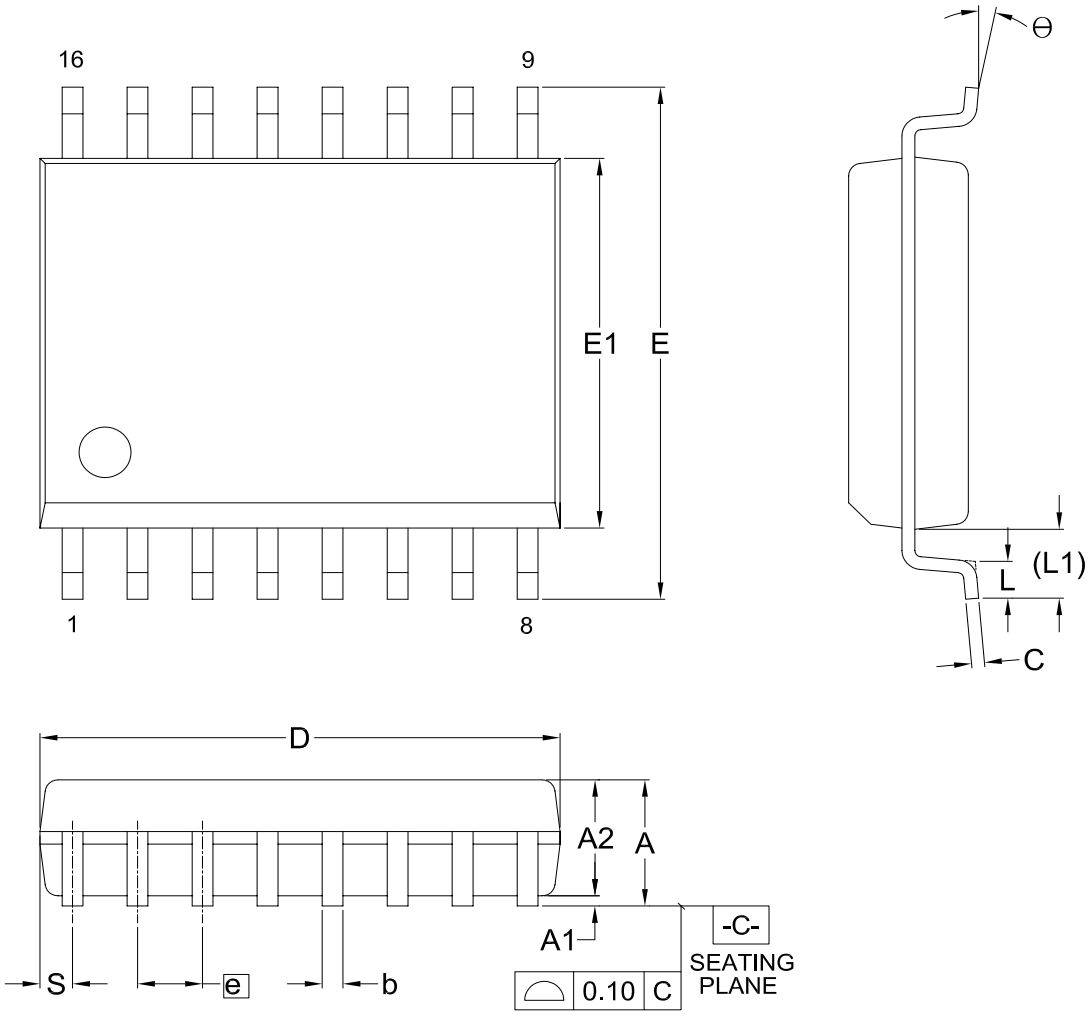
19. PART NAME DESCRIPTION



20. PACKAGE INFORMATION

20-1. 16-pin SOP (300mil)

Doc. Title: Package Outline for SOP 16L (300MIL)

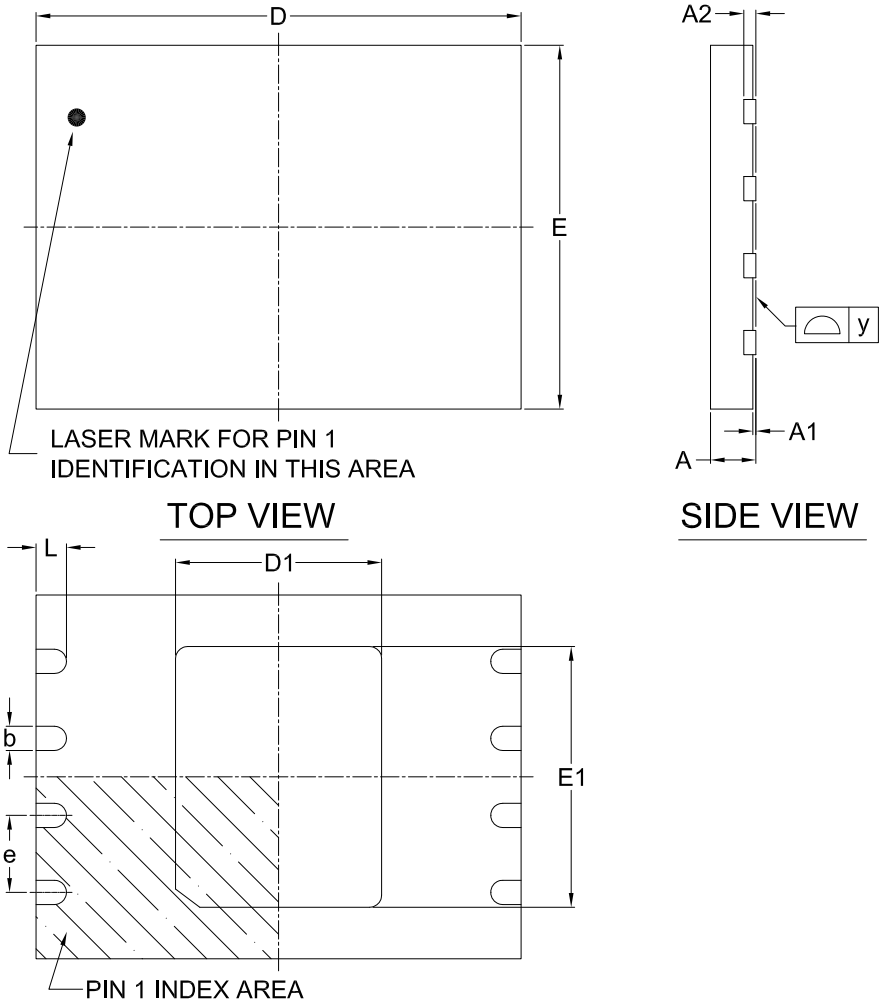


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.25	0.31	0.20	10.10	10.10	7.42	---	0.40	1.31	0.51	0°
	Nom.	---	0.20	2.35	0.41	0.25	10.30	10.30	7.52	1.27	0.84	1.44	0.64	5°
	Max.	2.65	0.30	2.45	0.51	0.30	10.50	10.50	7.60	---	1.27	1.57	0.77	8°
Inch	Min.	---	0.004	0.089	0.012	0.008	0.397	0.397	0.292	---	0.016	0.052	0.020	0°
	Nom.	---	0.008	0.093	0.016	0.010	0.405	0.405	0.296	0.050	0.033	0.057	0.025	5°
	Max.	0.104	0.012	0.096	0.020	0.012	0.413	0.413	0.299	---	0.050	0.062	0.030	8°

20-2. 8-land WSON (8x6mm 3.4 x 4.3EP)

Doc. Title: Package Outline for WSON 8L (8x6x0.8MM, LEAD PITCH 1.27MM, E.P. 3.4x4.3MM)



Note:

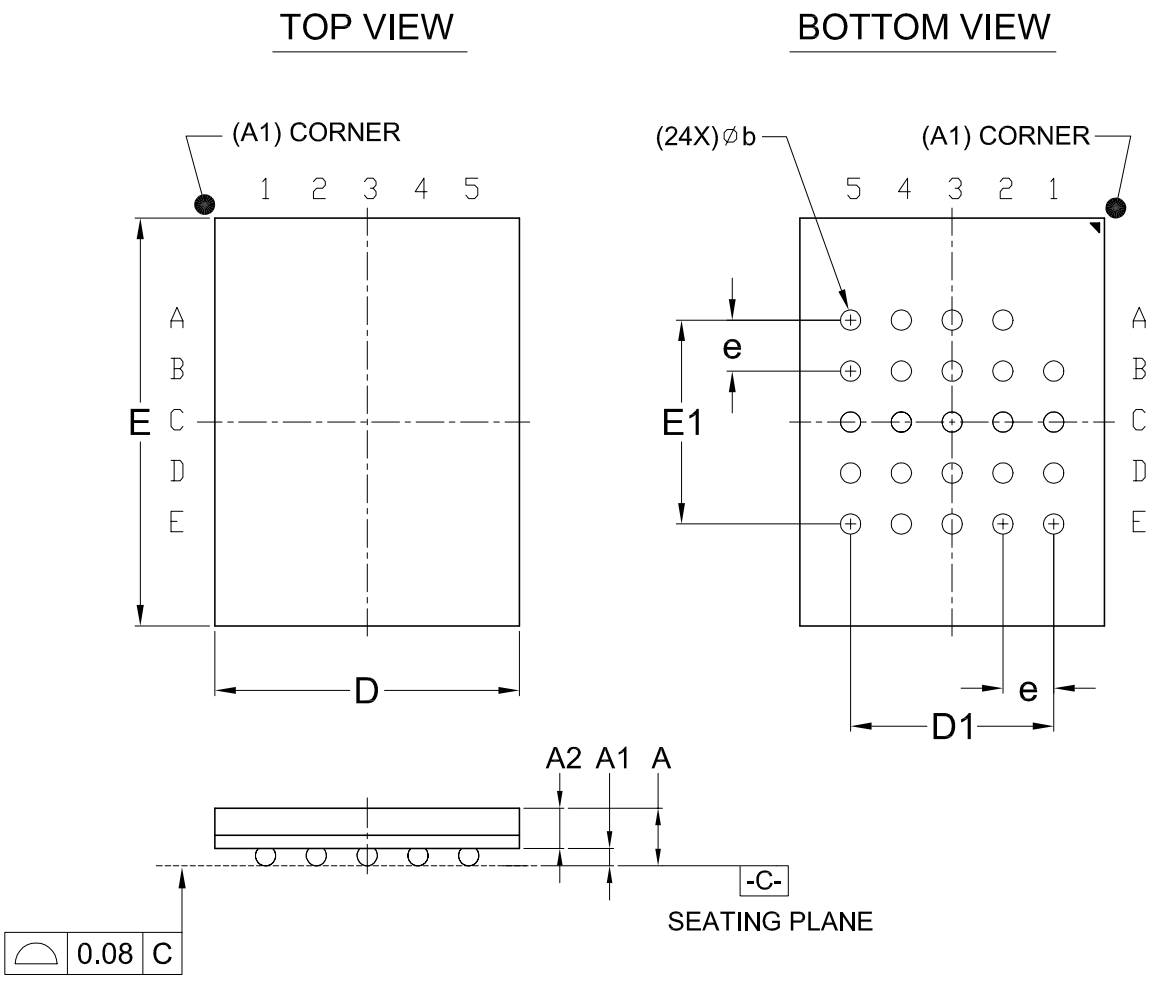
This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	---	0.35	7.90	3.35	5.90	4.25	0.45	---	0.00
	Nom.	---	---	0.20	0.40	8.00	3.40	6.00	4.30	0.50	1.27	---
	Max.	0.80	0.05	---	0.48	8.10	3.45	6.10	4.35	0.55	---	0.05
Inch	Min.	0.028	---	---	0.014	0.311	0.132	0.232	0.167	0.018	---	0.00
	Nom.	---	---	0.008	0.016	0.315	0.134	0.236	0.169	0.020	0.05	---
	Max.	0.032	0.002	---	0.019	0.319	0.136	0.240	0.171	0.022	---	0.002

20-3. 24-Ball BGA (5x5 ball array)

Doc. Title: Package Outline for CSP 24BALL (6x8x1.2MM, BALL PITCH 1.0MM, BALL DIAMETER 0.4MM, 5x5 BALL ARRAY)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	5.90	---	7.90	---	---
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	4.00	1.00
	Max.	1.20	0.35	---	0.45	6.10	---	8.10	---	---
Inch	Min.	---	0.010	0.026	0.014	0.232	---	0.311	---	---
	Nom.	---	0.012	---	0.016	0.236	0.157	0.315	0.157	0.039
	Max.	0.047	0.014	---	0.018	0.240	---	0.319	---	---

21. REVISION HISTORY

Revision	Descriptions	Page
October 12, 2021		
0.00	1. Initial Release.	All
April 22, 2022		
0.01	1. Revised *"Table 17. Acceptable Commands During Program/Erase Suspend after tPSL/tESL"*.	P85
	2. Added *"9-42. ECC (Error Correction Code)"* and removed tBP parameter.	P5, 68, 90, 97, 102
	3. Description modifications.	P7
November 28, 2022		
0.02	1. Optimized ICC2 and ICC4 values.	P96
	2. Description modifications.	P92
	3. Revised Output Driver Strength information.	P37-38
	4. Revised the maximum page program time.	P97, 102
	5. Changed document status as "Prelimary" to align with the product status.	All

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