Broadband Silicon Capacitor BBSC 0402 47nF BV30

Rev. 3.01

General description

BBSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.

The BBSC is suitable for DC blocking, feedback, coupling and bypassing applications in all broadband optoelectronics and High-speed data system.

The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive, offers unique performances with low insertion loss, low reflection and phase stability from 34KHz to 40GHz.

These capacitors in ultra-deep trenches in silicon have been developed in a semiconductor process, in order to integrate trench MOS capacitor providing high capacitance value of 47nF (for kHz–MHz range) and high frequency MIM capacitors for low capacitance value for GHz range), both in a SMT0402.

The BBSC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability. BBSC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (+70ppm/K).

Assembly: Flip chip or embedded applications through existing laminated packages (LGA, BGA) or rigid PCB, FR4 or flex platforms.

Finishing ENIG or SAC305 type 6 or in optional with copper pads for embedding.

Key features

- Broadband performance to 40GHz
- Resonance free
- Phase stability
- Insertion loss < 0.7dB typ. up to 40GHz
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55°C to +150°C)
  - Voltage <-0.1%/Volt
  - Negligible capacitance loss through ageing
- Low profile: 400µm, 100µm on request
- Break down voltage: 30V
- Low leakage current < 100pA
- High reliability
- High operating temperature (up to 150°C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300°C)
- Compatible with EIA 0402 footprint

Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- High volumetric efficiency (i.e. *capacitance* per unit *volume)*
- Broadband test equipment

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Functional diagram

The next figure provides implementation set-up diagram.

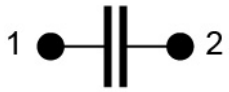

Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	47	-	nF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	20	150	°C
T_{STG}	Storage temperature (2)		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	70	-	ppm/K
RV_{DC}	Rated voltage (3)		-	-	16(4) 14.7(5)	V_{DC}
BV	Break down voltage	@+25°C	30	-	-	V
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV_{DC}, @+25°C	-	-	-0.1	$\%/V_{DC}$
IR	Insulation resistor	@RV_{DC}, +25°C, 120s	-	10	-	GΩ
ESR	Equivalent Serial Resistance	@+25°C, shunt mode	-	400	-	mΩ
ESL	Equivalent Serial Inductance	@+25°C, SRF shunt mode	-	250	-	pH
Fc_{-3dB}	Cut-off frequency at 3dB	@+25°C	-	34	40	kHz
IL	Insertion loss	@ 20 GHz, +25°C	-	0.4	-	dB
		@ 40GHz, +25°C	-	0.7	-	dB
RL	Return loss	Up to 40 GHz, +25°C	16	-	-	dB
ESD	HBM stress (6)	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

(1): other tolerance available upon request
(2): without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic lifetime prediction at 100°C continuous operation
(5): 10 years of intrinsic lifetime prediction at 150°C continuous operation
(6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

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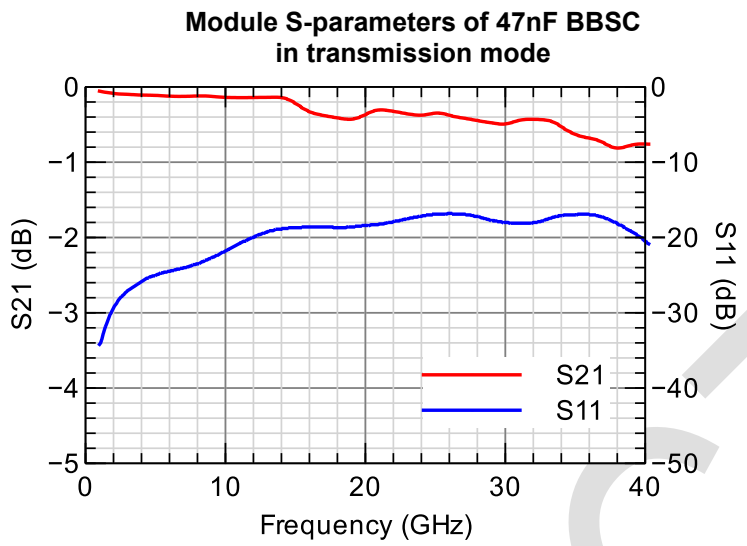
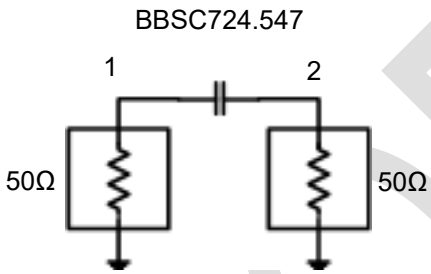


Figure 2 - 47nF BBSC measurement results (module of S-parameters)

Schematic of 47nF BBSC in transmission mode



10-mil Rogers 4350B.
Microstrip mode – line width = 0.551 mm and gap = 0.246 mm.
(nominal 50 ohm characteristic impedance).

Figure 3 – 47nF BBSC measurement schematic

Example of surface mounted 0402

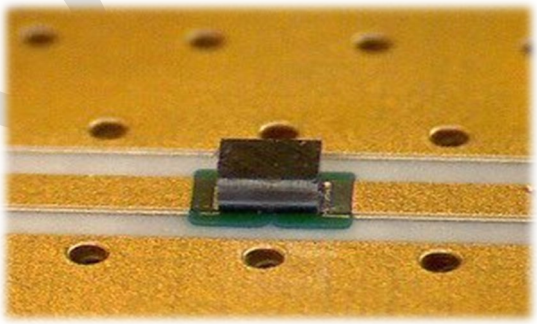


Figure 4 – micro picture of BBSC mounted on board in coplanar mode

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Pinning definition

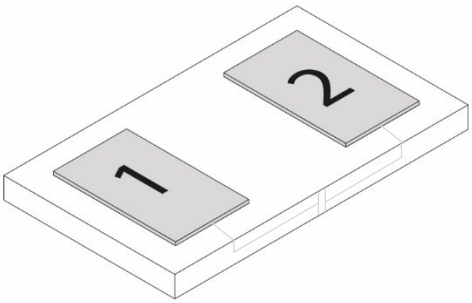

Figure 5 Pin configuration

pin #	Symbol	Coordinates X / Y
1	Signal	-330.0 / 0.0
2	Signal	330.0 / 0.0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

Ordering Information for BBSC724.547

Type number	Package		
	Packaging	Finishing	Description
939113724547-F1N	6” film frame carrier(1)	ENIG(2)	BBSC 0402 - 47nF – 2 pads – 1.20mm x 0.70mm x 0.40mm
939113724547-T3N	T&R 1 000units(3)	ENIG(2)	BBSC 0402 - 47nF – 2 pads – 1.20mm x 0.70mm x 0.40mm
939114724547-F1N	6” film frame carrier(1)	ENIG(2)	BBSC 0402 - 47nF – 2 pads – 1.20mm x 0.70mm x 0.10mm
939114724547-T3N	T&R 1 000units(3)	ENIG(2)	BBSC 0402 - 47nF – 2 pads – 1.20mm x 0.70mm x 0.10mm

(1) Other film frame carrier are possible on request
(2) ENIG : Min 0.1µm Au / 5µm Ni
(3) Missing capacitors can reach 0.5%
(4) Refer to Figure7

Table 3 - Packaging and ordering information

Product Name	Die Name	Description
BBSC724.547	UJ0402547	BBSC 47nF/0402/BV30 – 2 pads – 1.2 x 0.7 x 0.40 mm (4)
BBSC724.547	UJ0402547	BBSC 47nF/0402/BV30 – 2 pads – 1.2 x 0.7 x 0.10 mm (4)

Table 4 - Die information

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Pad Metallization

The Surface Mounted Capacitor is delivered as standard with NiAu finishing [ENIG (0.1µm Au / 5µm Ni)].
Other Metallization, such as SAC305, Copper, Thick Gold or Aluminum pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

For further information, please see our mounting application note.

Package outline

The product is delivered as a bare die.

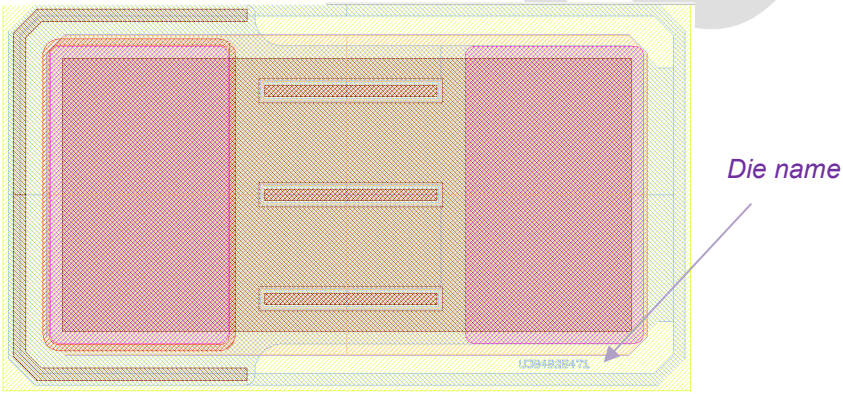

Figure 6 - Micro photography of a 47nF Capacitor

L (mm)	W (mm)	T (mm)	c (mm)	p (mm)	e (mm)	t (mm)
1.2 ±0.04	0.7 ±0.04	0.40 or 0.10 ±0.01	0.30	0.40	0.50	0.005(1)

(1) Standard with ENIG

Table 5 - Dimensions and tolerances

PROJECT

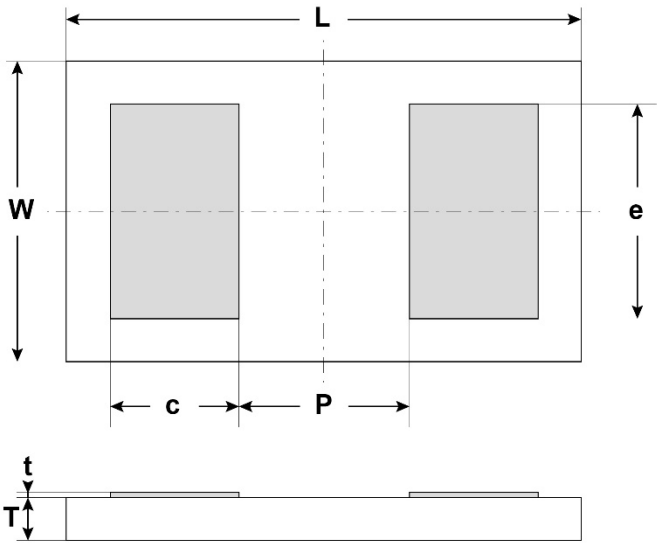

Figure 7 - Package outline drawing

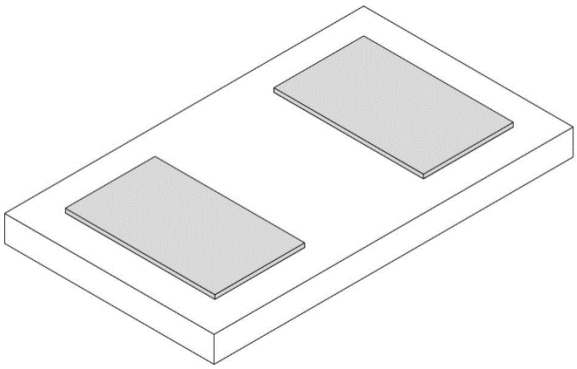

Figure 8 - Package isometric view

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Assembly

BBSC series is compatible with standard reflow technology.

It is recommended to design mirror pads on the PCB.

For further information, please see our mounting application note.

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 9 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Tape and Reel: (Die orientation (flip) within the case related to T&R orientation)

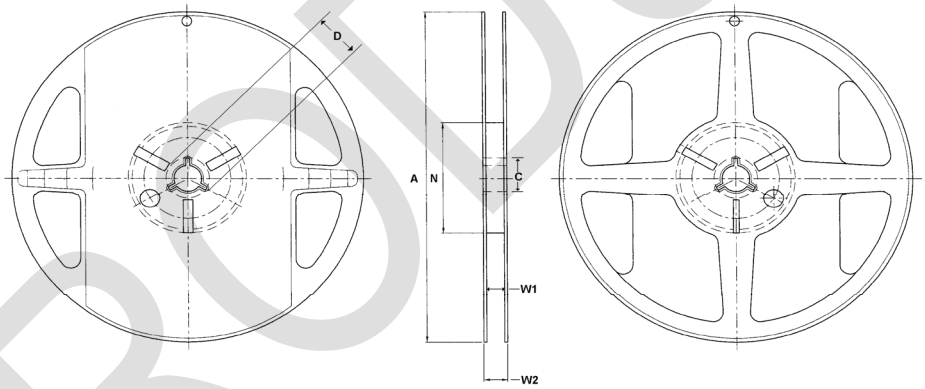

Figure 10 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	93	11.5

Table 6 - Reel dimensions (mm)

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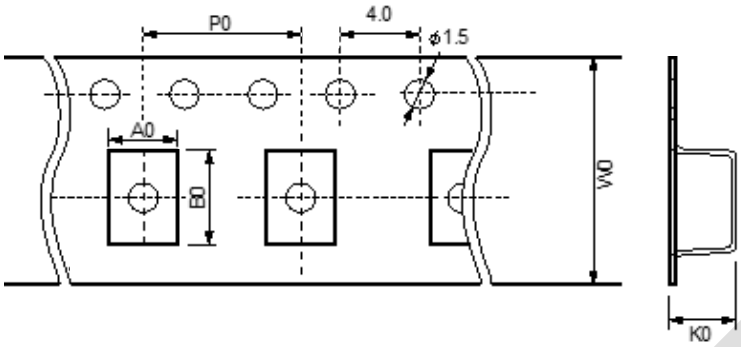

Figure 11 – Tape drawing (not to scale)

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Quantity per reel
A0	B0	K0			
0.92	1.31	0.56	8	4	1 000

Table 7 - Tape dimensions (mm)

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Film frame carrier

With UV curable dicing tape (UV performed).

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

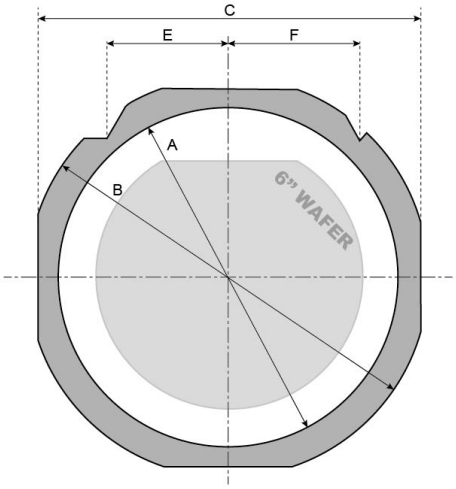

Figure 12 FF070 Frame with a 6" wafer

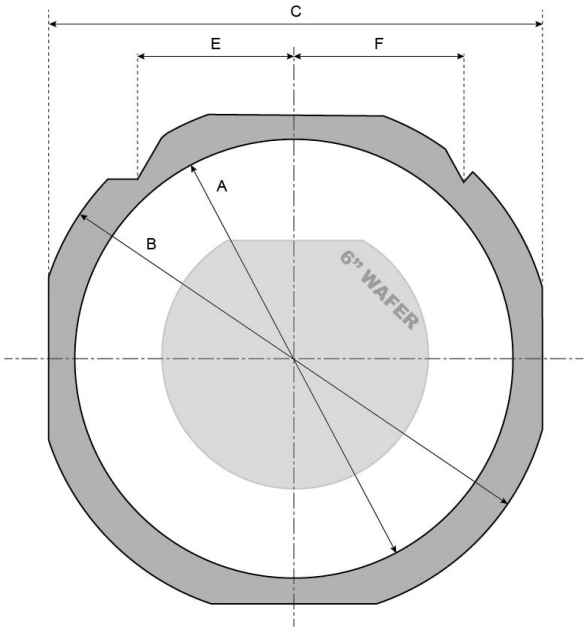

Figure 13 FF108 Frame with a 6" wafer

Frame Reference	Frame Style	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F
FF070 (1)	DTF-2-6-1	7.638”	8.976”	8.346”	0.048’’	2.370”	2.5’’
FF108 (1)	DTF-2-8-1	9.842”	11.653”	10.866”	0.048”	2.381”	2.5’’

Table 8 - Frame dimensions (inches)

(1) or equivalent

PROOF

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author.
Release 1.00	2016 November 07th	Objective specification	OGA
Release 1.04	2021 April 28th	Minor update	OGA
Release 2.00	2021 April 30th	Preliminary version	LLR, SCA, CGU, OGA, DDE
Release 3.00	2021 May 28th	Product version	LLR, SCA, CGU, OGA, DDE
Release 3.01	2025 October 20th	Ordering information has been updated according to the latest product lineup and specification.	HFU - CGU

Disclaimer / Life support applications

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