BroadBand Silicon Capacitor BBSC 0201M 22nF BV11

Rev. 2.00

General description

BBSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products. The BBSC is suitable for DC blocking, feedback, coupling and bypassing applications in all broadband optoelectronics and High-speed data system. The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with low insertion loss, low reflection and phase stability from 73 KHz to 40 GHz.

These capacitors in ultra-deep trenches in silicon have been developed in a semiconductor process, in order to integrate trench MOS capacitor providing high capacitance value of 22 nF (for kHz–MHz range) and high frequency MIM capacitors for low capacitance value (for GHz range), combined in a 0201M [0.6x0.3mm] case.

The BBSC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability. BBSC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (+70ppm/K).

Assembly: Suitable for surface mounted application on rigid PCB, ceramic substrate, FR4 (laminate) or flex platforms.

Bump finishing: SAC305 type 6.

Copper pads optional for embedding version and ENIG for un-bumped version, as an optional finishing.

Key features

- Broadband performance up to 40 GHz
- Resonance free
- Phase stability
- Insertion loss < 0.3dB Typ. up to 40 GHz.
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage <-0.1%/Volt
  - Negligible capacitance loss through ageing
- Low profile: 140 µm including bump height (SAC305 40µm bumps after reflow)
- Break down voltage : 11V
- Low leakage current < 100pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 01005 footprint and with EIA 0201 outline

Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- High volumetric efficiency *(i.e.* capacitance *per unit* volume)
- Broadband test equipment

Preliminary

Functional diagram

The next figure provides implementation set-up diagram.

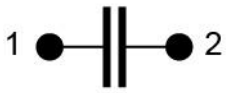

Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	22	-	nF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	20	150	°C
T_{STG}	Storage temperature (2)		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	70	-	ppm/K
RV_{DC}	Rated voltage (3)		-	-	3.8(4) 3.4(5)	V_{DC}
BV	Break down voltage	@+25°C	11	-	-	V
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV_{DC}, @+25°C	-	-	-0.1	$\%/V_{DC}$
IR	Insulation resistor	@RV_{DC}, +25°C, 120s	-	10	-	GΩ
ESL	Equivalent Serial Inductance	@+25°C, SRF shunt mode	-	100	-	pH
ESR	Equivalent Serial Resistance	@+25°C, shunt mode	-	300	-	mOhm
Fc-3dB	Cut-off frequency at 3dB	@+25°C	-	73	86	kHz
IL	Insertion loss	@ 20 GHz, +25°C	-	0.2	-	dB
		@ 40 GHz, +25°C	-	0.3	-	dB
RL	Return loss	Up to 40 GHz, +25°C	24	-	-	dB
ESD	HBM stress (6)	JS-001-2017	8	-	-	kV

Table 1 - Electrical performances

(1): other tolerance available upon request.
(2): without packaging.
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'.
(4): 10 years of intrinsic life time prediction at 100°C continuous operation.
(5): 10 years of intrinsic life time prediction at 150°C continuous operation.
(6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'.

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Module S-parameters of 22nF BBSC in transmission mode

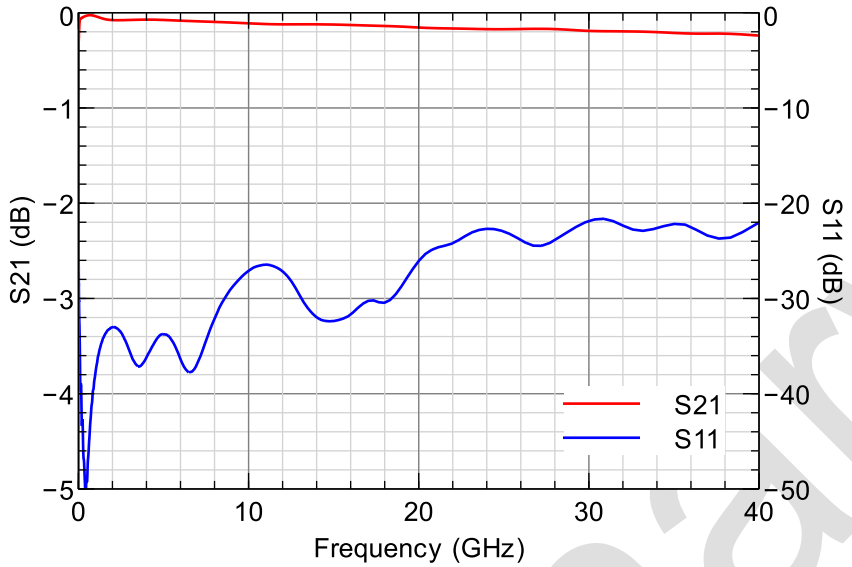
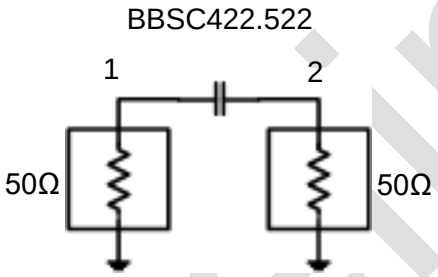


Figure 2 - 22nF BBSC measurement results (module of S-parameters)

Schematic of 22nF BBSC in transmission mode



4-mil Rogers 4350B.
Microstrip mode – line width = 0.200mm and gap = 0.200 mm.
(nominal 50 ohm characteristic impedance).

Figure 3 - 22nF BBSC measurement schematic

Example of surface mounted 0201M

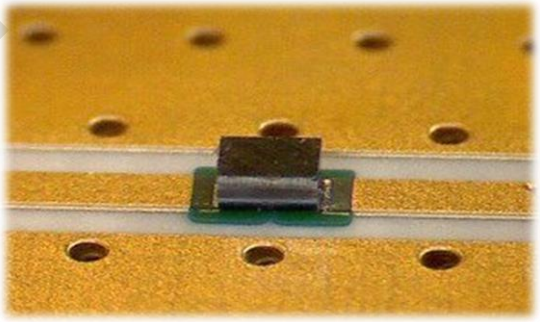


Figure 4 – micro picture of BBSC mounted on board in coplanar mode

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Pinning definition

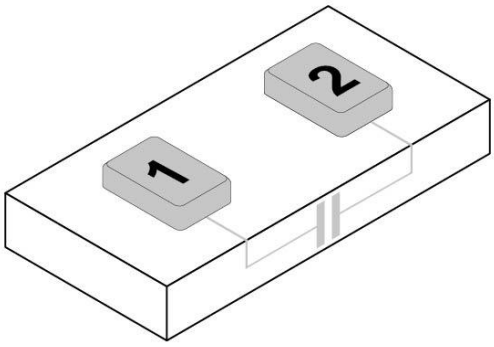

Figure 5 Pin configuration

pin #	Symbol	Coordinates X / Y
1	Signal	-150.0 / 0.0
2	Signal	150.0 / 0.0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

Ordering Information for BBSC422.522

Regardless of packaging, Murata Integrated Passive Devices delivers products with AQL level II (0.65).

Type number	Package		
	Packaging	Finishing	Description
939114422522-F1S	6” film frame carrier(1)	SAC(2)	BBSC 0201M - 22nF – 2 pads – 0.6 x 0.3 mm x 0.10mm (4)
939114422522-T3S	7” T&R (1 000 pieces/reel) (3)	SAC(2)	BBSC 0201M - 22nF – 2 pads – 0.6 x 0.3 mm x 0.10mm (4)
939114422522-T5S	7” T&R (5 000 pieces/reel) (3)	SAC(2)	BBSC 0201M - 22nF – 2 pads – 0.6 x 0.3 mm x 0.10mm (4)
939114422522-T3N	7” T&R (1 000 pieces/reel) (3)	NiAu (2)	BBSC 0201M - 22nF – 2 pads – 0.6 x 0.3 mm x 0.10mm (4)
939114422522-T5N	7” T&R (5 000 pieces/reel) (3)	NiAu (2)	BBSC 0201M - 22nF – 2 pads – 0.6 x 0.3 mm x 0.10mm (4)

(1) Other Film Frame Carrier are possible on request
(2) SAC = ENIG (0.1µm Au / 5µm Ni) + SAC305 type 6 or NiAu = ENIG (0.1µm Au / 5µm Ni
(3) Missing capacitors can reach 0.5%
(4) Refer to Figure 7

Table 3 - Packaging and ordering information

Product Name	Die Name	Description
BBSC422.522	XQM0201522	BBSC 22nF/0201M/BV11 – 2 pads – 0.6 x 0.3 x 0.10 mm

Table 4 - Die information

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Pad Metallization

The Surface Mounted Capacitor is delivered as standard with SAC305 type6 bumping.

Other Metallization, such as ENIG (0.1µm Au / 5µm Ni), Copper, Thick Gold or Aluminum pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a bare silicon die.

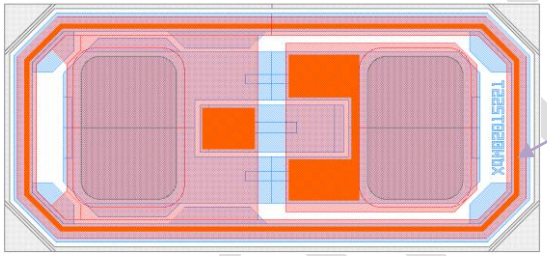

Figure 6 – Layout view

L (mm)	W (mm)	T (mm)	c (mm)	p (mm)	e (mm)	t (mm)
0.60 ±0.02	0.30 ±0.02	0.10 ±0.01	0.10	0.20	0.15	0.04(1) 0.05(2) 0.005(3)

(1) Standard with solder joint height after reflow on board.
(2) Standard with solder bump height before assembly
(3) Only in case of ENIG finishing

Table 5 - Dimensions and tolerances

Preliminary

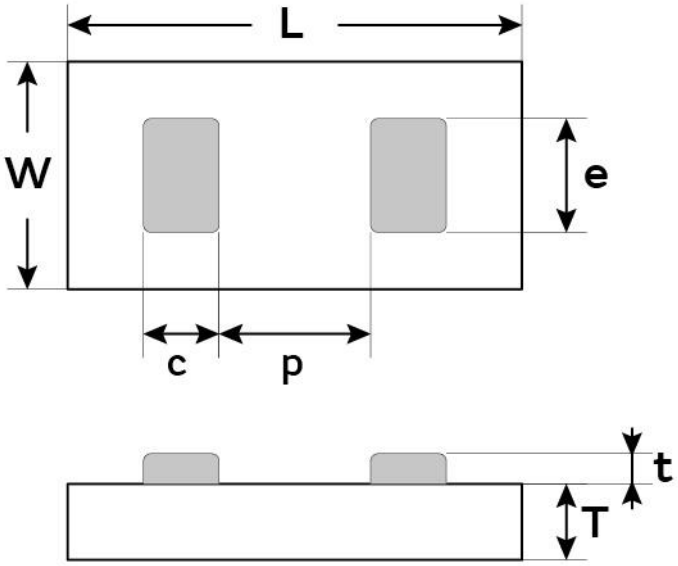

Figure 7 - Package outline drawing

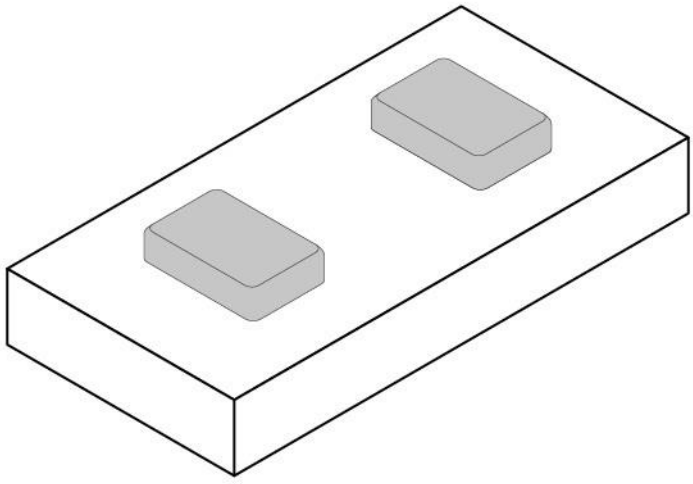

Figure 8 Isometric view

Preliminary

Assembly

BBSC series is compatible with standard reflow technology.

It is recommended to design mirror pads on the PCB.

For further information, please see our mounting application note

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 9 Scan this QR Code to access the Murata Silicon Capacitor web page

Preliminary

Packaging format

Please refer to application note ‘Products Storage Conditions and Shelf Life’.

Tape and Reel: Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

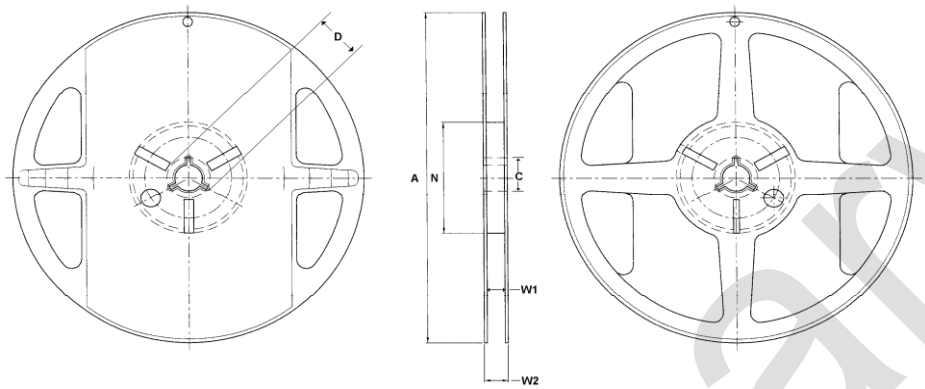

Figure 10 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	21	60	9.5	11.4

Table 6 - Reel dimensions (mm)

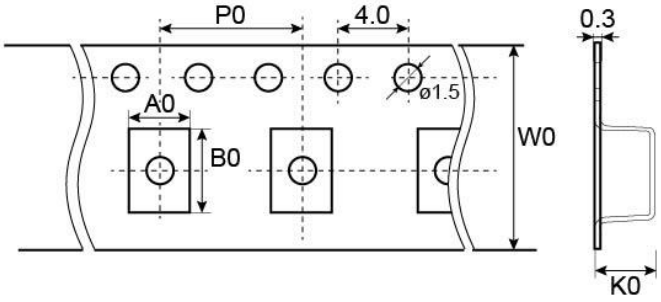

Figure 11 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Reel Capacity
Ao	Bo	Ko			
0.37 +/-0.04	0.67 +/-0.04	0.20 +/-0.04	8.00	2.00	1000 or 5000

Table 7 - Tape dimensions (mm)

Preliminary

Film frame carrier:

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

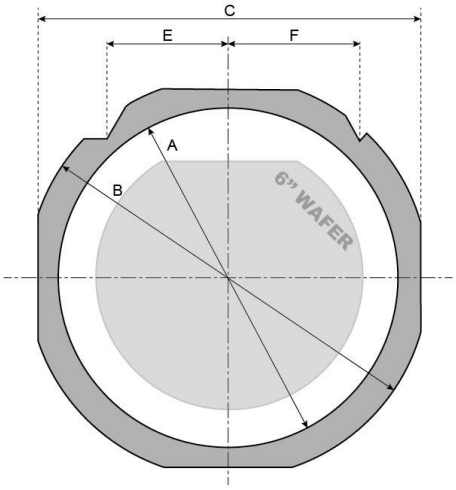

Figure 12 FF070 Frame with a 6" wafer

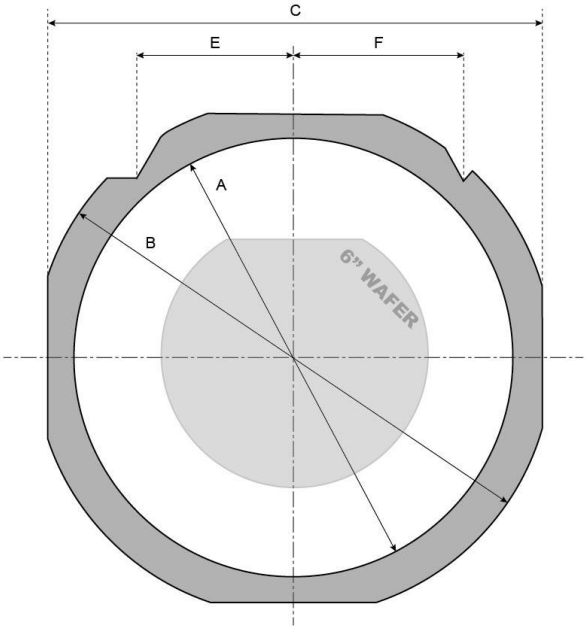

Figure 13 FF108 Frame with a 6" wafer

Frame Reference	Frame Style	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F
FF070 (1)	DTF-2-6-1	7.638”	8.976”	8.346”	0.048’’	2.370”	2.5’’
FF108 (1)	DTF-2-8-1	9.842”	11.653”	10.866”	0.048”	2.381”	2.5’’

Table 8 - Frame dimensions (inches)

(1) or equivalent

Preliminary

Expander grip ring 6” diameter:

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

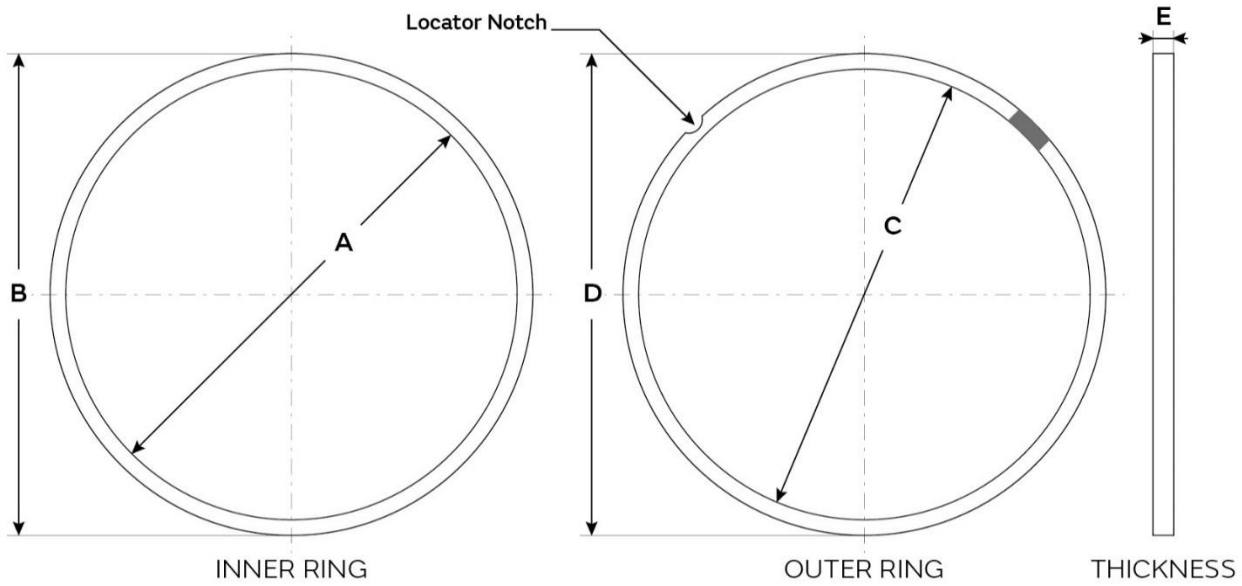

Figure 14 – Grip Ring drawing

Grip Ring Style	A	B	C	D	E	Locator Notch
GRP-2620-6 (1)	7.670”	7.973”	7.975”	8.280”	0.236”	None

Table 9 - Frame dimensions (inches)

(1) or equivalent

Preliminary

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values: Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information: Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author.
Release 1.00	2019 August 21st	Objective specification	OGA
Release 1.02	2020 Oct. 19th	Packaging update	SCA; OGA
Release 1.03	2021 May 11th	Minor update	SCA; OGA
Release 2.00	2021 June 2nd	Preliminary release	SCA; OGA; LLR; DDE, SCA; CGU, SYO; DYO

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