

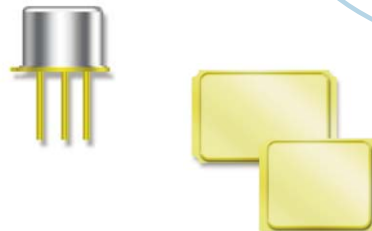
# Radiation Hardened NPN Silicon Switching Transistors

2N2221A, 2N2221AL, 2N2221AUA, 2N2221AUB  
2N2222A, 2N2222AL, 2N2222AUA, 2N2222AUB



## Features

- Qualified to MIL-PRF-19500/255
- Levels:
  - JANSM-3K Rads (Si)
  - JANSJ-10K Rads (Si)
  - JANSP-30K Rads (Si)
  - JANSL-50K Rads (Si)
  - JANSR-100K Rads (Si)
- TO-18 (TO-206AA), Surface mount UA & UB Packages



## Absolute Maximum Ratings ( $T_C = +25^\circ\text{C}$ unless otherwise noted)

Ratings	Symbol	Value	Units
Collector - Emitter Voltage	$V_{CEO}$	50	Vdc
Collector - Base Voltage	$V_{CBO}$	75	Vdc
Emitter - Base Voltage	$V_{EBO}$	6.0	Vdc
Collector Current	$I_C$	800	mAdc
Total Power Dissipation @ $T_A = +25^\circ\text{C}$	$P_T$		
2N2221A, L      2N2222A, L		0.5	W
2N2221UA      2N2222UA		0.5	
2N2221UB      2N2222UB		0.5	
Operating & Storage Temperature Range	$T_{Op}, T_{stg}$	-65 to +200	$^\circ\text{C}$

## Thermal Characteristics

Characteristics	Symbol	Maximum	Units
Thermal Resistance, Junction-to-Ambient	$R_{\theta JC}$		
2N2221A, L      2N2222A, L		325	$^\circ\text{C/W}$
2N2221UA      2N2222UA		325	
2N2221UB      2N2222UB		325	

## Electrical Characteristics ( $T_A = +15^\circ\text{C}$ , unless otherwise noted)

OFF Characteristics	Symbol	Minimum	Maximum	Units
Collector - Emitter Breakdown Voltage $I_C = 10 \text{ mAdc}$	$V_{(BR)CEO}$	50	- - -	Vdc
Collector - Base Cutoff Current $V_{CB} = 75 \text{ Vdc}$ $V_{CB} = 60 \text{ Vdc}$	$I_{CBO1}$ $I_{CBO2}$	- - -	10 10	$\mu\text{Adc}$ nAdc
Emitter - Base Cutoff Current $V_{EB} = 6.0 \text{ Vdc}$ $V_{EB} = 4.0 \text{ Vdc}$	$I_{EBO1}$ $I_{EBO2}$	- - - - - -	10 10	$\mu\text{Adc}$ nAdc
Collector - Emitter Cutoff Current $V_{CE} = 60 \text{ Vdc}, V_{BE} = 1.5 \text{ Vdc}$	$I_{CES}$	- - -	10	nAdc

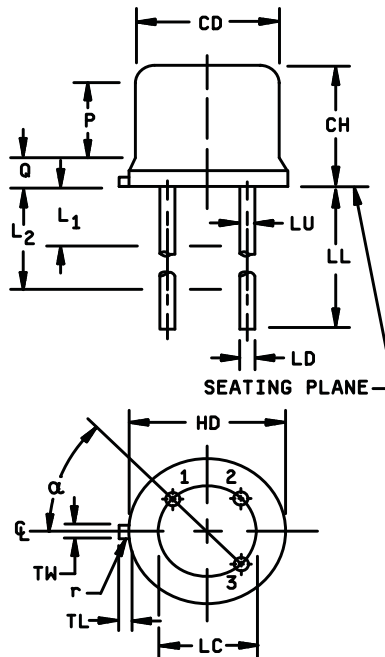


## Electrical Characteristics ( $T_A = +15^\circ\text{C}$ , unless otherwise noted)

ON Characteristics <sup>(1)</sup>		Symbol	Minimum	Maximum	Units
Forward Current Transfer Ratio $I_C = 0.1 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$ $I_C = 1.0 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$ $I_C = 10 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$ $I_C = 150 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$ $I_C = 10 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$	2N2221A, L, UA, UB	$H_{FE}$	30		
	2N2222A, L, UA, UB		50		
	2N2221A, L, UA, UB		35	150	
	2N2222A, L, UA, UB		75	325	
	2N2221A, L, UA, UB		40		
	2N2222A, L, UA, UB		100		
	2N2221A, L, UA, UB		40	120	
	2N2222A, L, UA, UB		100	300	
	2N2221A, L, UA, UB		20		
	2N2222A, L, UA, UB		30		
Collector - Emitter Saturation Voltage $I_C = 150 \text{ mAdc}, I_B = 15 \text{ mAdc}$ $I_C = 500 \text{ mAdc}, I_B = 50 \text{ mAdc}$		$V_{CE(sat)1}$ $V_{CE(sat)2}$	- - - - - -	0.3 1.0	Vdc
Base - Emitter Saturation Voltage $I_C = 150 \text{ Adc}, I_B = 0.5 \text{ Vdc}$ $I_C = 500 \text{ Adc}, I_B = 2.0 \text{ Vdc}$		$V_{BE(sat)1}$ $V_{BE(sat)2}$	0.6 - - -	1.2 2.0	Vdc
DYNAMIC Characteristics					
Small-Signal Short-Circuit Forward Current Transfer Ratio $I_C = 1.0 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ MHz}$		$h_{fe}$	30 50		
Magnitude of Small-Signal Short-Circuit Forward Current Transfer Ratio $I_C = 10 \text{ Adc}, V_{CE} = 20 \text{ Vdc}, f = 100 \text{ MHz}$		$ h_{fe} $	2.5		
Output Capacitance $V_{CB} = 10 \text{ Vdc}, I_E = 0, 100 \text{ kHz} \leq f \leq 1.0 \text{ MHz}$		$C_{obo}$	- - -	8.0	pF
Output Capacitance $V_{CB} = 0.5 \text{ Vdc}, I_E = 0, 100 \text{ kHz} \leq f \leq 1.0 \text{ MHz}$		$C_{ibo}$	- - -	25	pF
Switching Characteristics					
Turn-On Time See figure 8 of MIL-PRF-19500/255		$t_{on}$		35	ns
Turn-Off Time See Figure 9 of MIL-PRF-19500/255		$t_{off}$		300	ns

(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Outline Drawing (TO-18):

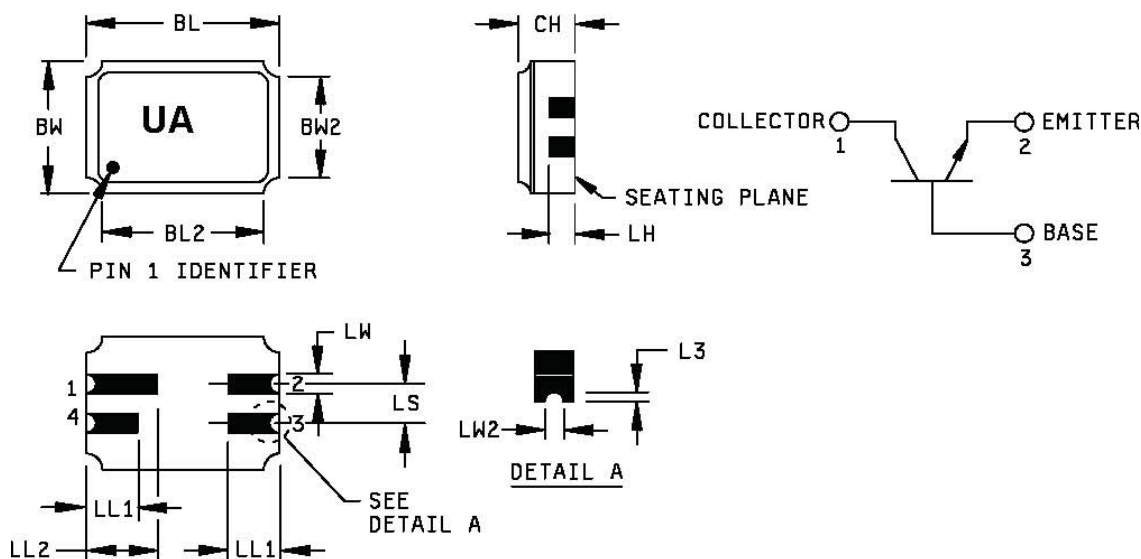


### NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TL shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L<sub>1</sub> and L<sub>2</sub>. Dimension LD applies between L<sub>2</sub> and LL minimum. Diameter is uncontrolled in L<sub>1</sub> and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
13. For L suffix devices, dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8,13
LU	.016	.019	0.41	0.48	7,8
L <sub>1</sub>		.050		1.27	7,8
L <sub>2</sub>	.250		6.35		7,8
P	.100		2.54		
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
α	45° TP		45° TP		6
1, 2, 9, 11, 12, 13					

## Outline Drawing (UA surface mount):



### NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension CH controls the overall package thickness. When a window lid is used, dimension CH must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions LW2 minimum and L3 minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on the bottom two layers, optional on the top ceramic layer.) Dimension LW2 maximum and L3 maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi$ x symbology.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.215	.225	5.46	5.71	
BL2		.225		5.71	
BW	.145	.155	3.68	3.93	
BW2		.155		3.93	
CH	.061	.075	1.55	1.90	3
L3	.003	.007	0.08	0.18	5
LH	.029	.042	0.74	1.07	
LL1	.032	.048	0.81	1.22	
LL2	.072	.088	1.83	2.23	
LS	.045	.055	1.14	1.39	
LW	.022	.028	0.56	0.71	
LW2	.006	.022	0.15	0.56	5

Pin no.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.96	
LL2	.017	.035	0.43	0.89	

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
LS <sub>1</sub>	.036	.040	0.91	1.02	
LS <sub>2</sub>	.071	.079	1.81	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r <sub>1</sub>		.012		.305	
r <sub>2</sub>		.022		.559	

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metalized areas.
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi$ x symbology.

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