

MMA041PP5

Datasheet

DC–25 GHz GaAs MMIC Distributed Low-Noise Amplifier

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Power Matters.™

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

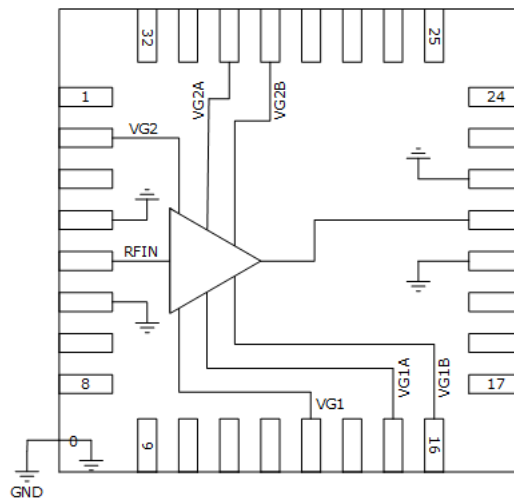
Revision 1.0 was published in May 2017. It was the first publication of this document.

2 Product Overview

MMA041PP5 is a gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) pseudomorphic high-electron-mobility transistor (pHEMT) distributed amplifier in a leadless 5 mm × 5 mm surface-mount package that operates between DC and 25 GHz. It is ideal for test instrumentation and communications infrastructure applications. The amplifier provides a flat gain of 17 dB, 2.5 dB noise figure, and 21 dBm of output power at 1 dBm gain compression while requiring only 150 mA from an 7 V supply. Output IP3 is typically 35 dBm. The MMA041PP5 amplifier features RF I/Os that are internally matched to 50 Ω. It is also available in die form as the MMA041AA.

The following image shows the primary functional blocks of the MMA041PP5 device.

Figure 1 • MMA041PP5 Functional Block Diagram



2.1 Applications

The MMA041PP5 device is designed for the following applications:

- Test and measurement instrumentation
- Electronic warfare (EW), electronic countermeasures (ECM), and electronic counter-countermeasures (ECCM)
- Military and space
- Telecom infrastructure
- Wideband microwave radios
- Microwave and millimeter-wave communication systems

2.2 Key Features

The following are key features of the MMA041PP5 device:

- Frequency range: DC to 25 GHz
- Flat gain: 17 dB
- High output IP3: 35 dBm
- Low noise figure: 2.5 dB at 10 GHz
- Supply voltage: 7 V at 150 mA
- 50 Ω matched I/O
- 32-lead 5 mm × 5 mm × 1.2 mm QFN package

3 Electrical Specifications

This section details the electrical specifications of the MMA041PP5 device.

3.1 Absolute Maximum Ratings

This following table lists the absolute maximum ratings of the MMA041PP5 device.

Table 1 • Absolute Maximum Ratings

Parameter	Rating
Storage temperature	–65 °C to 150 °C
Operating temperature	–40 °C to 85 °C
Drain bias voltage (V_D)	8 V
Gate bias voltage (V_{G1} and V_{G2})	–2 V to 0.5 V
V_D current (I_{DD})	300 mA
RF input power	19 dBm
DC power dissipation ($T = 85$ °C)	2.4 W
Channel temperature	150 °C
Thermal impedance	18 °C/W
ESD HBM	TBD

3.2 Specified Electrical Performance

The following table lists the specified electrical performance of the MMA041PP5 device at 25 °C, where V_{DD} is 7 V, I_{DD} is 150 mA, and V_{GG} is –0.4 V.

Table 2 • Specified Electrical Performance

Parameter	Frequency Range	Min	Typ	Max	Units
Operational frequency range		DC		25	GHz
Gain	DC–6 GHz	17	18		dB
Gain	6 GHz–12 GHz	16	17.5		dB
Gain	12 GHz–20 GHz	15	17		dB
Gain flatness	4 GHz–12 GHz		±0.5		dB
Gain flatness	12 GHz–20 GHz		±0.5		dB
Noise figure	1 GHz–6 GHz		2.7		dB
Noise figure	6 GHz–12 GHz		2		dB
Noise figure	12 GHz–20 GHz		2.5		dB
Input return loss	DC–6 GHz		15		dB
Input return loss	6 GHz–12 GHz		18		dB
Input return loss	12 GHz–20 GHz		13		dB
Output return loss	DC–6 GHz		13		dB
Output return loss	6 GHz–12 GHz		18		dB
Output return loss	12 GHz–20 GHz		16		dB
P1dB	DC–6 GHz		21		dBm
P1dB	6 GHz–12 GHz	21	22		dBm
P1dB	12 GHz–20 GHz	17	19		dBm
Psat	DC–6 GHz		24		dBm
Psat	6 GHz–12 GHz		24		dBm
Psat	12 GHz–20 GHz		21		dBm
OIP3	DC–6 GHz		35		dBm
OIP3	6 GHz–12 GHz		36		dBm
OIP3	12 GHz–20 GHz		36		dBm
V_{DD} (drain voltage supply)			7		V
I_{DD} (drain current)			150		mA
V_{GG} (gate voltage supply)		–1.0	–0.4	0	V

3.3 Typical Performance Curves

The following graphs show the typical electrical performance curves of the MMA041PP5 device at 25 °C, where V_{DD} is 7 V and I_{DD} is 150 mA, unless otherwise indicated.

Figure 2 • Gain vs. Temperature

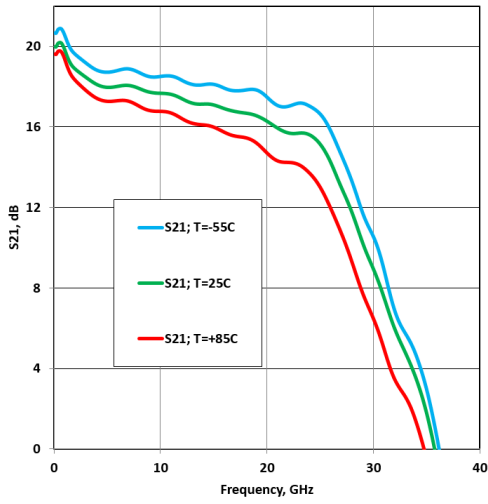


Figure 3 • Input Return Loss vs. Temperature

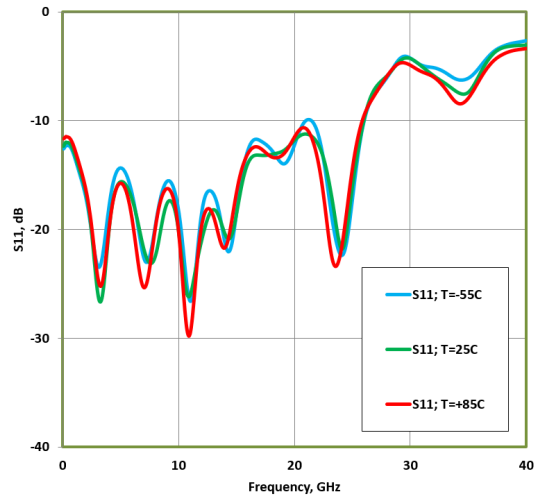


Figure 4 • Output Return Loss vs. Temperature

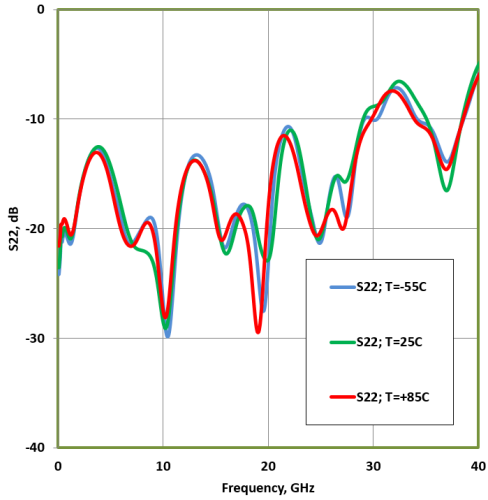


Figure 5 • Noise Figure vs. Temperature

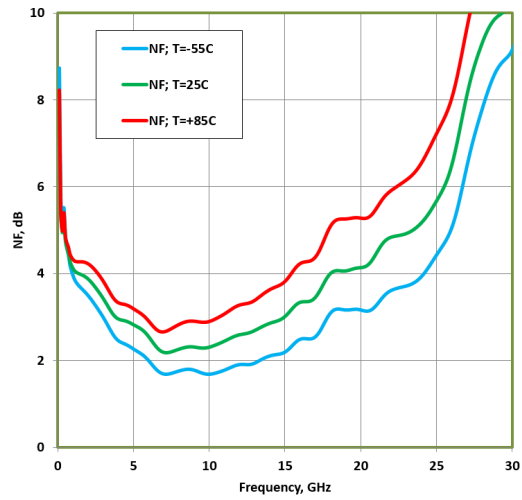


Figure 6 • P1dB and P3dB vs. Temperature

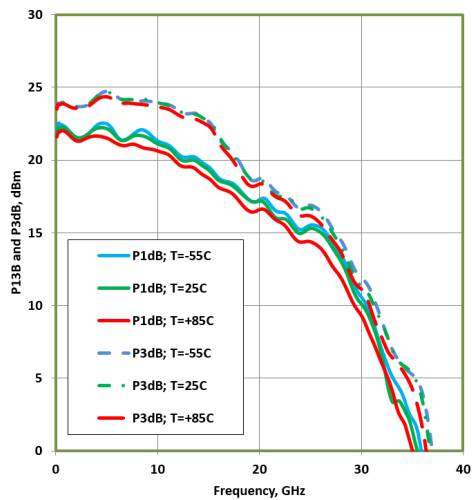
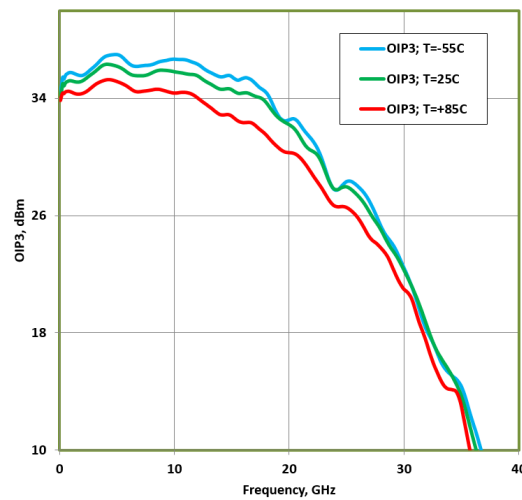


Figure 7 • Output Third Order Intercept vs. Temperature



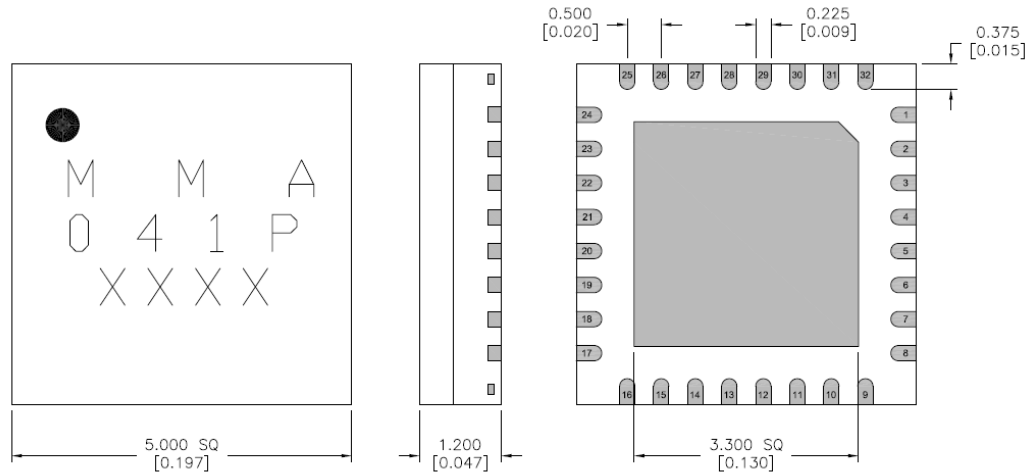
4 Package Specification

This section details the package specifications of the MMA041PP5 device.

4.1 Package Outline Drawing

The following illustration shows the package outline of the MMA041PP5 device. Dimensions are in millimeters [inches].

Figure 8 • Package Outline



4.2 Package Information

The following table lists the package information of the MMA041PP5 device. For additional packaging information, contact your Microsemi sales representative.

Table 3 • Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking
MMA041PP5	Low-stress injection molded plastic	Ni/Pd/Au	TBD	MMA 041P wwyy

4.3 Pin Descriptions

The following table describes the pins of the MMA041PP5 device.

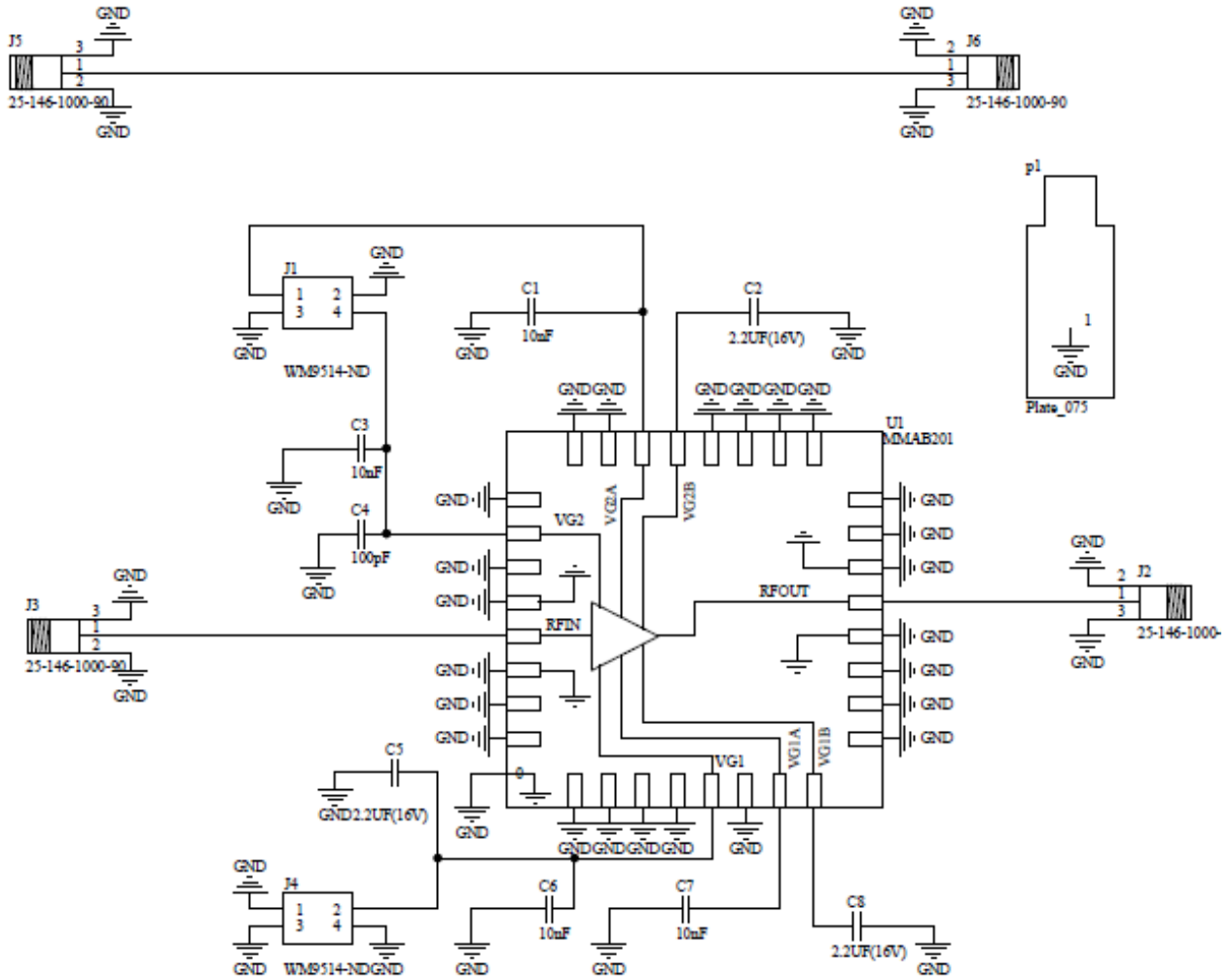
Table 4 • Pin Description

Pin Number	Pin Name	Description
1, 3, 7, 8, 9, 10, 11, 12, 14, 17, 18, 19, 23, 24, 25, 26, 27, 28, 31, 32	N/C	These pins are not connected internally. All data was measured with these pins connected to RF/DC ground externally.
2	VG2	Gate control for the amplifier. Adjust to achieve $I_{DD} = 60$ mA.
4, 6, 20, 22	GND	Ground paddle must be connected to RF/DC ground.
5	RFIN	This pin is DC-coupled and matched to 50 Ω .
13	VG1	Gate control for the amplifier. Adjust to achieve $I_{DD} = 60$ mA.
15, 16	VGAC1, VGAC2	Low-frequency termination. Connect bypass capacitors per application circuit below.
29, 30	VDAC1, VDAC2	Low-frequency termination. Connect bypass capacitors per application circuit below.
21	RFOUT	This pin is DC-coupled and matched to 50 Ω .
Backside paddle	RF/DC GND	RF/DC ground.

4.4 Application Circuit

The following illustration shows the application circuit of the MMA041PP5 device.

Figure 9 • Application Circuit



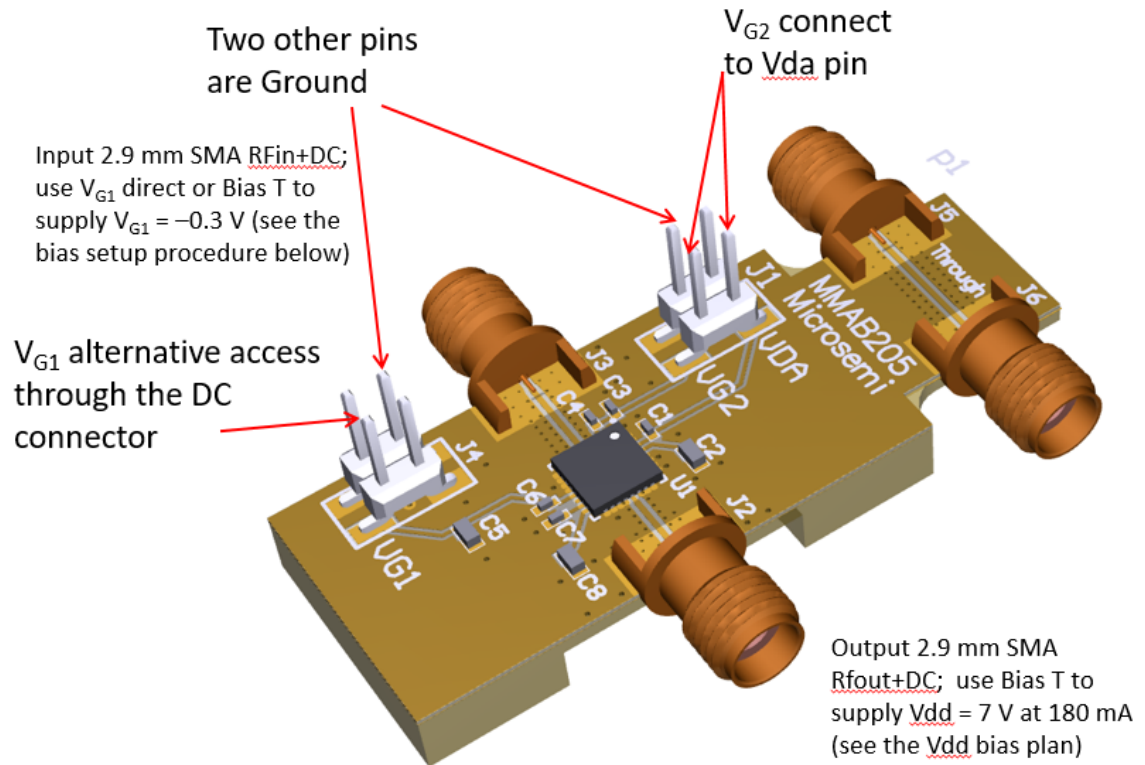
5 Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note [AN01 GaAs MMIC Handling and Die Attach Recommendations](#).

6 Evaluation Board Information

The following image shows the evaluation board of the MMA041PP5 device.

Figure 10 • Evaluation Board



The circuit board used in the application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 Ω impedance, and the package ground leads and backside ground paddle should be connected directly to the ground plane similar to the previous image.

The following table shows the list of materials for the evaluation PCB MMA041PP5E.

Table 5 • List of Materials for Evaluation PCB MMA041PP5E

Item	Description
C1, C3, C6, C7	CAP 10 nF 50 V –20% to +80% 0402 (1005 metric) thickness 0.6 mm SMD
C2, C5, C8	2.2 μ F 16 V ceramic capacitor X5R 0603 (1608 metric) 0.063" L \times 0.031" W (1.60 mm \times 0.80 mm)
C4	CAP 100 pF 50 V \pm 10% 0402 (1005 metric) thickness 0.6 mm SMD
J1, J4	Header, 2-pin, dual row
J2, J3, J5, J6	CONN 2.9 mm female PCB edge mount .012 pin
P1	Plate 749-MM-0198
U1	MMIC MMA041PP5

7 Ordering Information

The following table shows the ordering information for the MMA041PP5 device.

Table 6 • Ordering Information

Part Number	Package
MMA041PP5	5 mm × 5 mm plastic QFN package
MMA041PP5E	Evaluation board for MMA041PP5

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