Bus Arbitration Module

The MC68452 is a bipolar asynchronous bus controller which allows multiple local MPU buses to be multiplexed onto a common global bus enabling the local buses to share memory, I/O devices, and communicate with each other easily and efficiently.

- Performs Arbitration For Eight Users Of A Global Bus
- Expandable
- Implements Fixed Physical Priority
- Supports Cycle By Cycle Or Block Mode Arbitration
- 52 ns Max Arbitration Time
- Performs Arbitration For Eight Users Of A 68000 Bus
- 28 Pin Package
- +5.0 Volt Only Operation

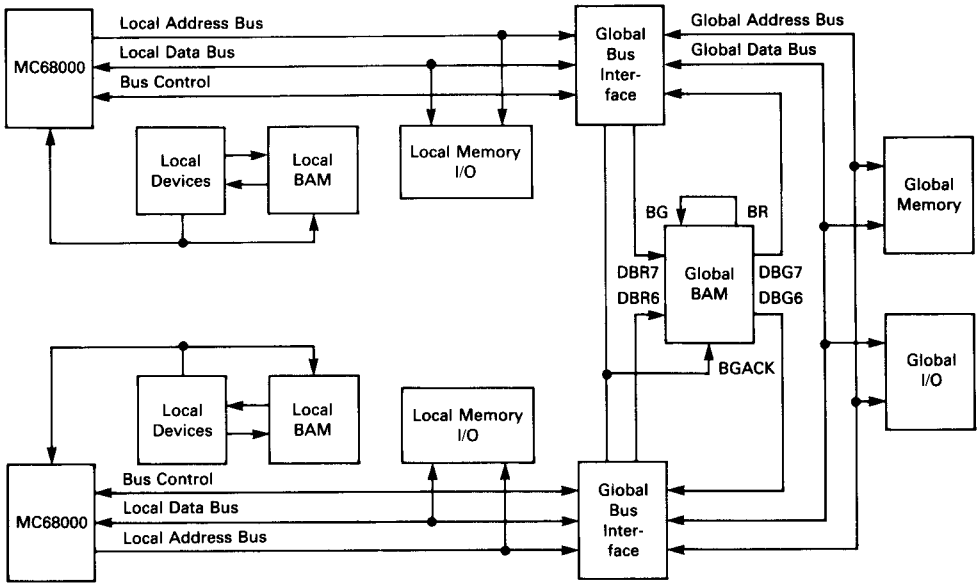

FIGURE 1 — MC68452 IN A MODERATELY COUPLED MULTI-PROCESSOR SYSTEM

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−65 to +150	°C

DC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

Parameter	Min	Max	Unit	Test Conditions
V_{IH} High Level Input Voltage	2.0		V	
V_{IL} Low Level Input Voltage		0.8	V	
V_{IK} Input Clamp Voltage		−1.5	V	V_{CC} = MIN, I_{in} = −18 mA
V_{OH} High Level Output Voltage	2.4		V	V_{CC} = MIN, I_{OH} = 2.6 mA
V_{OL} Low Level Output Voltage		0.5	V	V_{CC} = MIN, I_{OL} = 24 mA
I_{OS} Output Short Circuit Current(2)		−130	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{IH} High Level Input Current		20	μA	V_{CC} = MAX, V_{in} = 2.7 V
I_{IL} Low Level Input Current		−0.4	mA	V_{CC} = MAX, V_{in} = 0.4 V
I_{CC} Supply Current	−15	−130	mA	V_{CC} = MAX

AC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 V ± 5%, T_A = 0°C to 70°C, t_{rise} = t_{fall} = 6 ns max)

Parameter	Number*	Min	Max	Units
$\overline{DBRn}$ Low to $\overline{BR}$ Low	1	—	24	ns
$\overline{DBRn}$ High to $\overline{BR}$ High	2	—	31	ns
$\overline{BG}$ Low to $\overline{DBGn}$ Low	3	—	28	ns
$\overline{BGACK}$ Low to $\overline{DBRn}$ High	4	2.0	—	ns
$\overline{BGACK}$ Low to $\overline{DBGn}$ High	5	—	52	ns
$\overline{BGACK}$ High to $\overline{DBGn}$ Low	6	—	52	ns
$\overline{DBRn}$ Low to $\overline{BCLR}$ Low(1)	7	—	28	ns
$\overline{BGACK}$ High to $\overline{BCLR}$ High	8	—	24	ns
$\overline{DBRn}$ High to $\overline{BGACK}$ High	9	0	—	ns

*See Figure 2.

NOTES:
1. Assuming pending request is higher priority than current user.
2. No more than one output should be shorted at a time for no more than one second.

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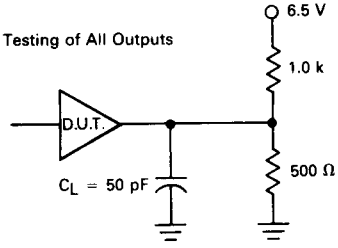
AC TEST CIRCUIT - Functional and Ac Testing of All Outputs



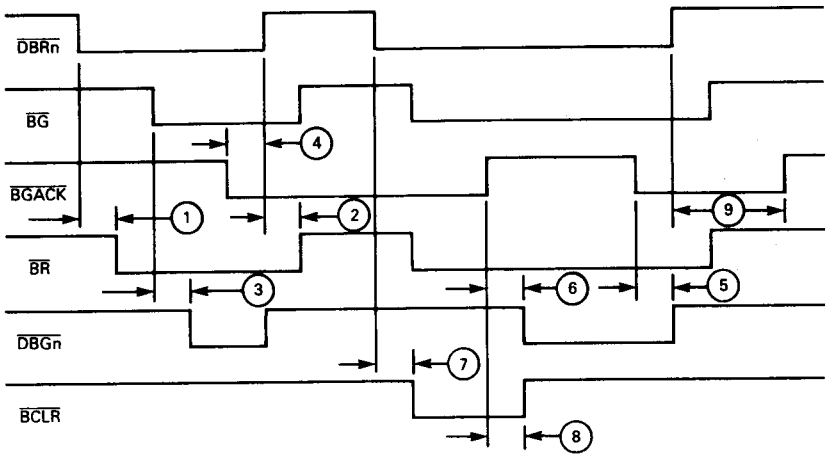


FIGURE 2 — TIMING DIAGRAM

SIGNAL DESCRIPTION

DEVICE BUS REQUEST (DBR7 – DBR0) — These eight inputs are active low and are used to indicate that a user demands a bus cycle(s). The DBR inputs are prioritized with DBR7 as the highest and DBR0 the lowest. This priority scheme is only used when two or more devices have pending requests.

DEVICE BUS GRANT (DBG7 – DBG0) — These active low outputs indicate that a user has obtained the bus, should bring BGACK active, and begin the transfer. The DBGn is removed when the user brings BGACK active.

BUS REQUEST (BR) — This output is the logical AND of all the DBRn inputs. This active low signal indicates that one or more of the DBR inputs are active.

BUS GRANT (BG) — This active low input is used to enable the DBGn outputs.

BUS GRANT ACKNOWLEDGE (BGACK) — This active low input indicates that a user has taken control of the bus. Each user must be able to generate this signal. When BGACK becomes active the DBGn will be removed.

BUS CLEAR (BCLR) — This active low output indicates that a higher priority device has a request pending. This signal is enabled by the BGACK being active. How this signal is used is totally up to the system designer. The BAM cannot force any device off the bus.

LATCH ENABLE INPUT (LEI) — This active low input is used to cascade BAMs to allow more than eight bus users. This signal should be the logical AND of all BR outputs of the BAM circuits. This signal is used to close the input request latch in all BAM circuits whenever there is a request pending in any part. This allows the encoding/decoding to proceed in all parts without spiking the outputs of any parts.

THEORY OF OPERATION

The BAM provides a central arbitration function by utilizing a separate request-grant pair for each user as opposed to multiplexing all requests onto a single line and daisy-chaining the grant. Each BAM circuit has eight DBR-DBG request-grant pairs. When a device desires to use the bus it brings its DBR low (active). Since the BAM circuit operates asynchronously there are no restrictions placed on the active transition of the DBRn signals. There are however, two minor restrictions placed on the inactive transition. The restrictions are: 1) all requests must remain active until they receive their grant signal and bring the BGACK active, and 2) the request is removed before the BGACK is released.

Each bus request line has a corresponding bus grant line (DBGn). After a requesting device brings its request active it must monitor the DBGn signal. When this signal becomes active the user has obtained the bus, should bring BGACK active, and begin transferring. The device can maintain control of the shared bus as long as the BGACK signal remains active. This three level handshake (request-grant-acknowledge) allows the BAM to support single or block type transfers with equal ease.

When the device transfer is complete it should remove the BGACK signal to allow the arbiter to determine the next user. In order for the BAM to operate properly the three level handshake must be used even if only single transfers are supported. When the BAM detects the BGACK going inactive it initiates another arbitration cycle, therefore the BGACK signal must be used properly. Although the DBGn outputs are disabled when BGACK is active the BAM has the current user number latched internally. During the transfer the current user number is compared with the highest active pending request. If the pending device is higher priority the BUS CLEAR (BCLR) will become active. Any circuitry for forcing devices off the bus and re-arbitrating must be provided external to the BAM.

Since the BAM is an asynchronous device, the bus grant outputs are *not* guaranteed to be spike free, although the internal delay paths have been equalized to minimize the occurrence of output spikes. The spikes are caused by metastabling of the internal request input latch. The arbitration cycle begins when one of the request inputs makes an active going transition. The request input latch is closed to prevent the encoder/decoder path from changing during the cycle. Requests that change just as the latches are closing may cause the latch to metastable or in essence attempt to latch in an analog level in the feedback path of the latch. If this metastable occurs in a request that is higher priority than the request that initiated the cycle the two bus grant outputs will spike alternately for approximately 50 ns. The metastable state should resolve itself into a valid digital state within this time and the outputs will stabilize to a valid state. These spikes can be removed by disabling the bus grant outputs during the arbitration cyle as shown in the circuit of Figure 3.

The BAM is an asynchronous state machine and is sensitive to noise at certain state transition times. The first critical time is the active transition of the DBRn inputs. These inputs must have a 6.0 ns maximum fall time to insure proper state transitions inside the part. This 6.0 ns specification can be easily met by having an LSTTL buffer drive a single DBRn input directly. Violation of this parameter *may* force the BAM into an invalid state. In this state the part will ignore all inputs except BGACK. The state can be cleared by bringing BGACK active for at least 20 ns and returning it to the inactive state.

The second critical time is the inactive transition of BGACK. This signal must have a 6.0 ns maximum rise time with no transitions for a minimum of 15 ns after reaching threshold. Violation of these two parameters *may* force the BAM into the same invalid state as discussed in the previous paragraph. Recovery procedures are the same as above.

MODES OF OPERATION

Local Central Arbiter

Figure 4 shows the BAM circuit in a local bus configuration. In this mode, the BAM serves as a central bus controller as opposed to the distributed control of a daisy-chain arbitration scheme. As shown, the BAM provides the interface between the local bus masters and the MC68000 MPU. The BR-BG pair of each local

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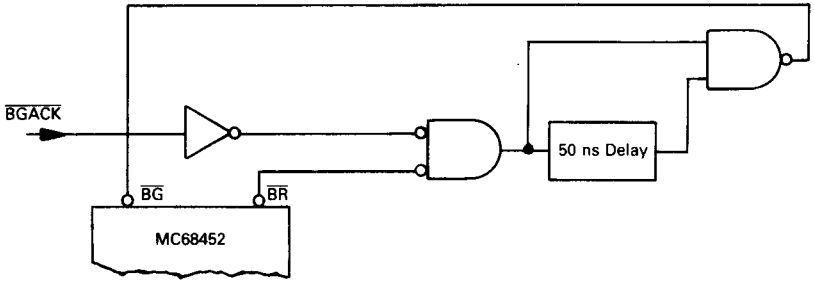

FIGURE 3 — CIRCUIT TO DISABLE GRANT OUTPUTS DURING ARBITRATION CYCLE

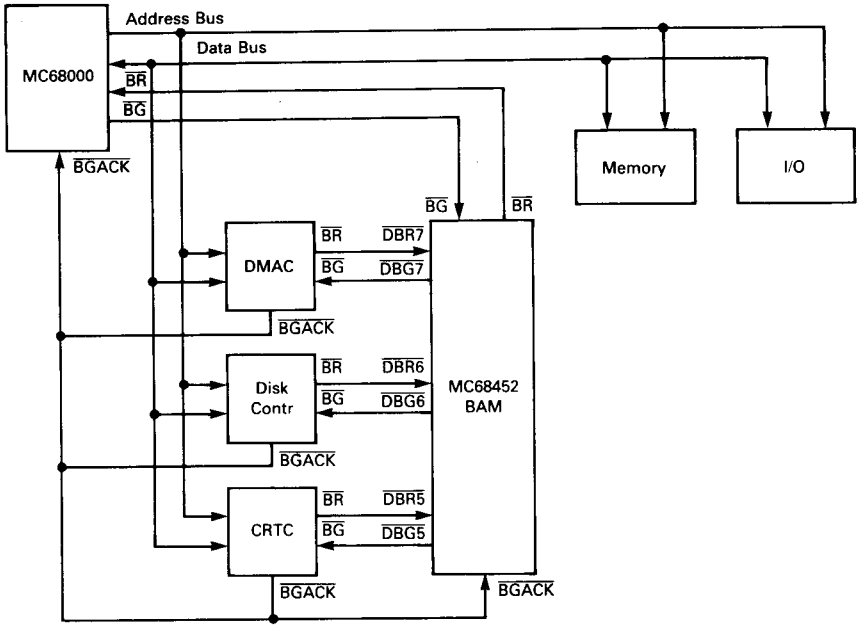

FIGURE 4 — LOCAL BUS ARBITER CONFIGURATION

bus master connect directly to the DBRn-DBGn pair of BAM. The BR-BG pair of the processor connect directly to the BR-BG pair of the BAM.

Whenever a device desires bus access it brings its BR (DBRn) active. The BAM detects the active request and makes a bus request (BR) to the processor. Within 1.5 clocks the MPU will return the BG to the BAM. This signifies that the requesting device can obtain control of the bus at the end of the current bus cycle. When the BAM receives the BG from the processor it will issue the DBGn to the highest priority requesting device. When the next bus master observes the end of the current bus cycle, it should bring BGACK active and begin to transfer. As long as the BGACK is held active the user can continue bus cycles indefinitely. When the current user completes the transfer it should release the BGACK to allow others to use the bus. If there is another request pending, the MC68000 MPU will remain in the idle state and another device will be allowed to become bus master. When no devices have a pending request the BAM will remove the BR from the MPU and allow the processor to resume execution.

Global Bus Arbiter

Figure 1 shows a moderately coupled multiprocessor system utilizing the BAM circuit. The global BAM serves as the central bus controller of the shared global bus. This allows multiple local buses to share mass storage and the addition of the more local processors to increase system throughput.

Figure 5 shows the global interface of each local bus. Please note that this circuit is used as an example. It will only support local bus masters with arbitration at the end of every bus cycle. However, the BAM does not preclude global bus masters and will certainly support block transfers with the proper interface circuitry. The local bus generates the DBRn by detecting some global address on the address bus. As shown, the AS is used in the DBRn equation to eliminate any switching noise on the address decode signal. The local DTACK signal also enters the DBRn equation to remove the request before BGACK is released. In this configuration there is no MPU to be removed from control of the global bus. Therefore, the BR output is connected directly to the BG input of the BAM. This allows a short delay before the DBGn outputs are enabled to allow encoding/decoding to proceed without switching noise appearing on the outputs. The rest of the circuitry shown in Figure 4 is used to generate the output enable for address/data three-state drivers and the BGACK for this user. Since the DBGn signal is removed when BGACK becomes active the OEn is the logical OR of the DBGn and the BGACKn for each user. The BGACK is generated when the global bus generates the global DTACK (GDTACK).

This will bring the clear active on the flip-flop which brings BGACK low and removes the DBGn. After the local bus recognizes the DTACK it will finish the cycle by removing ASn. The rising edge of the AS clocks the flip-flop and removes the BGACK which initiates another arbitration cycle. By removing BGACK at the end of every cycle this circuit implements single cycle transfers. This is probably the most efficient way to operate if the MPU is performing the transfers. However, this circuit can support local bus masters other than the MPU. If a DMA is performing the transfer, the clock to the BGACK flop might be the END signal from the DMA controller. Certainly both modes could be supported easily by multiplexing these two clocks together using single cycle for program I/O cycles and block mode for DMA cycles.

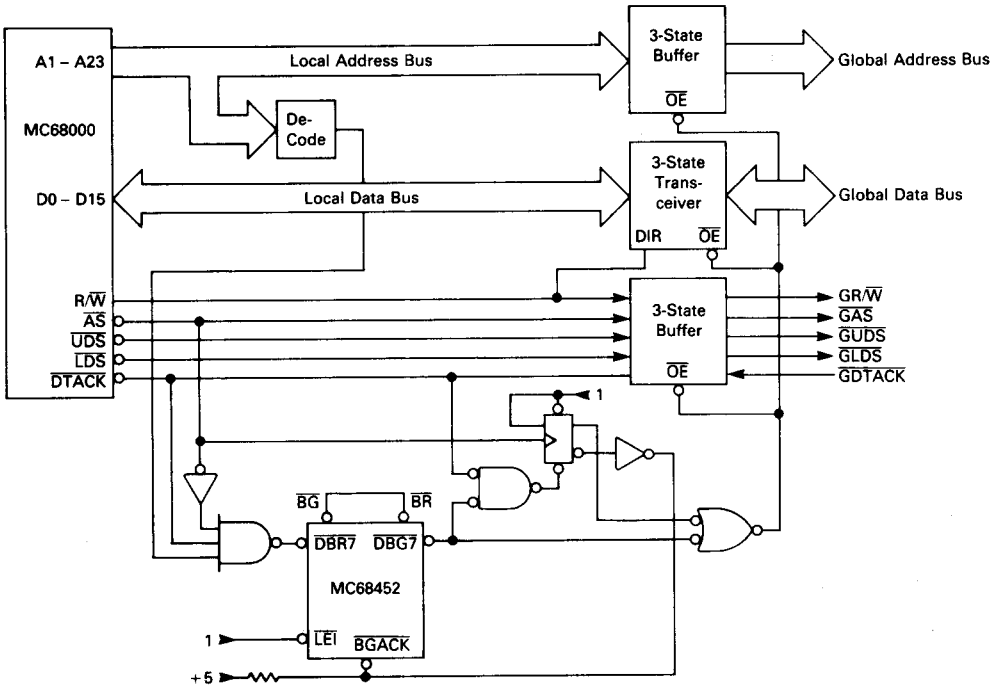

FIGURE 5 — GLOBAL BUS ARBITER CONFIGURATION

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Expanding the Arbiter

If a system requires more than eight bus masters the BAMs can be cascaded to any number of users required. Figure 6 shows a circuit that can support up to 64 bus masters. To support 64 users, nine BAMs are required. Eight parts supply the DBRn-DBGn request-grant pairs, and one part monitors status of the eight parts in parallel to supply the BCLR signal and handle the eight asynchronous BR outputs. As shown, the BR outputs of the parallel parts are connected to the DBRn inputs of the expansion BAM. This preserves the physical priority and handles the asynchronous expansion. By expanding in this way, the BAMs can operate correctly, however, the arbitration cycle will now require 80 ns max.

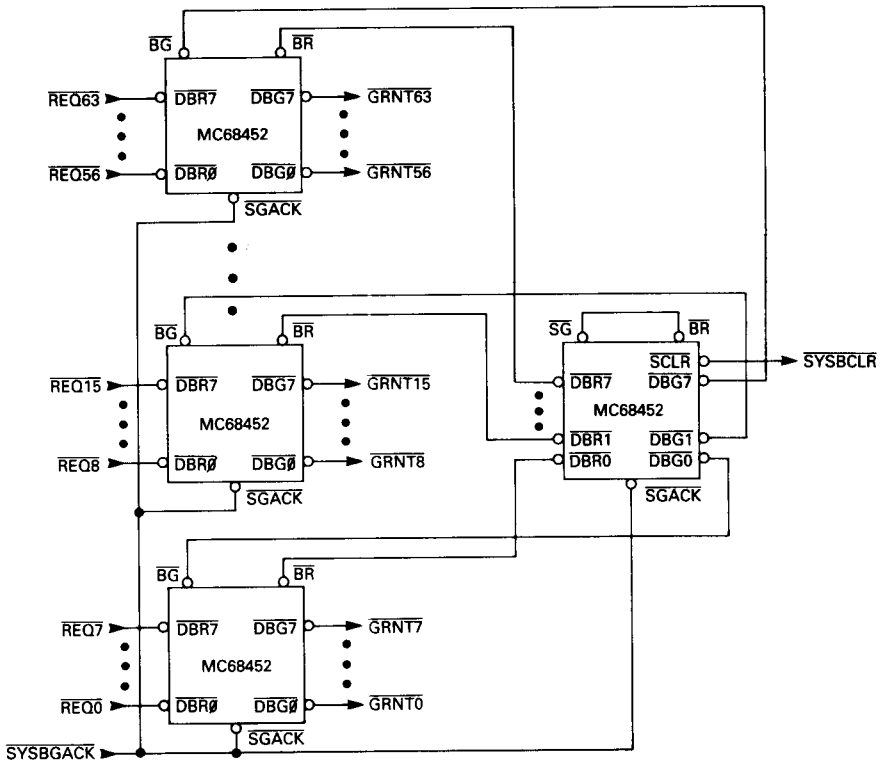
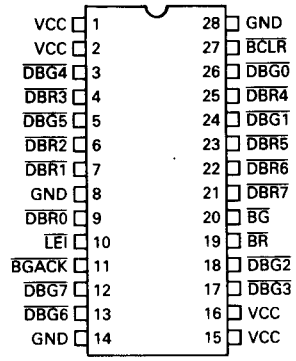


FIGURE 6 — EXPANDED BAM CONFIGURATION

BAM SIGNAL DIAGRAM



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