MOTOROLA

MCM10149*25

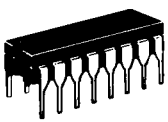
256 x 4-BIT PROGRAMMABLE READ-ONLY MEMORY

This device is a 256-word x 4-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

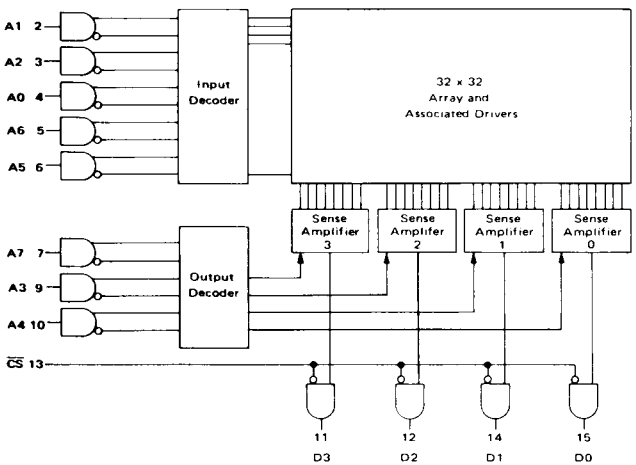
- Typical Address Access Time of 20 ns
- Typical Chip Select Access Time of 8.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (540 mW typ @ 25°C) Decreases with Increasing Temperature

MECL

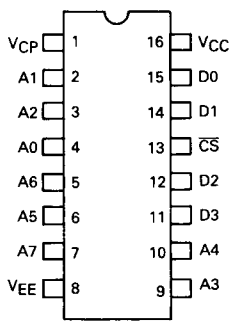
1024-BIT PROGRAMMABLE READ-ONLY MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620



PIN ASSIGNMENT



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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	0°C		+25°C		+75°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	155	–	150	–	145	mAdc
Input Current High	I_{inH}	–	265	–	265	–	265	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

Forcing Function	Parameter	0°C	25°C①	75°C①
V_{IHmax} =	V_{OHmax}	−0.840	−0.810	−0.720
	V_{OHmin}	−1.000	−0.960	−0.900
	V_{OHAmin}	−1.020	−0.980	−0.920
V_{IHAmin}		−1.130	−1.105	−1.045
V_{ILAmax}		−1.490	−1.475	−1.450
	V_{OLAmax}	−1.645	−1.630	−1.605
	V_{OLmax}	−1.665	−1.650	−1.625
V_{ILmin} =	V_{OLmin}	−1.870	−1.850	−1.830
V_{ILmin}	I_{NLmin}	0.5	0.5	0.3

NOTES: ① 0–75°C temperature range, 50Ω to −2.0V.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10149*25 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		Unit	Conditions
		Min	Max		
Read Mode				ns	Measured from 50% of input to 50% of output. See Note 1.
Chip Select Access Time	t_{ACS}	2.0	10		
Chip Select Recovery Time	t_{RCS}	2.0	10		
Address Access Time	t_{AA}	7.0	25		
Rise and Fall Time	t_r, t_f	1.5	7.0	ns	Measured between 20% and 80% points.
Capacitance				pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	5.0		
Output Capacitance	C_{out}	—	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10149;
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.
4. V_{CP} = V_{CC} = Gnd for normal operation.

*To be determined; contact your Motorola representative for up-to-date information.

PROGRAMMING THE MCM10149 †

During programming of the MCM 10149, input pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input pins 2, 3, 4, 5, and 6 are addressed with 0 V $\leq V_{IH} \leq$ + 0.25 V and $V_{EE} \leq V_{IL} \leq$ −3.0 V. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with V_{CP} = V_{CC} = 0 V and V_{EE} = − 5.2 V ± 5%, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to + 12 V ± 0.5 V (total voltage V_{CP} to V_{EE} is now 17.2 V, + 12 V − [− 5.2 V]). The rise time of this V_{CP} voltage pulse should be in the 1 − 10 μs range, while its pulse width (t_{W1}) should be greater than 100 μs but less than 1 ms. The V_{CP} supply current at + 12 V will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be

set on both of these supplies. The current limit on the V_{CP} supply should be set at 700 mA while the V_{CC} supply should be limited to 250 mA. It should be noted that the V_{EE} supply must be capable of sinking the combined current of the V_{CC} and V_{CP} supplies while maintaining a voltage of −5.2 V ± 5%.

Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresponding output pin to a voltage of +2.85 V ± 5%. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor to −2.0 V. Current into the selected output is 5.0 mA maximum.

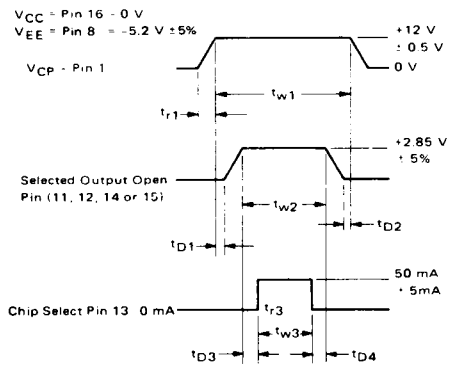
After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. Its pulse width should be greater than 100 μs. Pulse magnitude is 50 mA ± 5.0 mA. The voltage clamp on this current source is to be −6.0 V.

After the fusing current source has returned 0 mA, the bit select pulse is returned to its initial level, i.e., the output is returned through its load to −2.0 V. Thereafter, V_{CP} is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables. Noncompliance voids warranty.

PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149.



The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., V_{CP} = 0 V. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of ≤ 15% is to be observed.

Definitions and values of timing symbols are as follows.

Symbol	Definition	Value
t_{r1}	Rise Time, Programming Voltage	≥ 1 μs
t_{w1}	Pulse Width, Programming Voltage	≥ 100 μs < 1 ms
t_{D1}	Delay Time, Programming Voltage Pulse to Bit Select Pulse	≥ 0
t_{w2}	Pulse Width, Bit Select	≥ 100 μs
t_{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	≥ 0
t_{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	≥ 1 μs
t_{r3}	Rise Time, Programming Current Pulse	250 ns max
t_{w3}	Pulse Width, Programming Current Pulse	≥ 100 μs
t_{D4}	Delay Time, Programming Current Pulse to Bit Select Pulse	≥ 1 μs

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MANUAL PROGRAMMING CIRCUIT