MOTOROLA SEMICONDUCTOR I TECHNICAL DATA

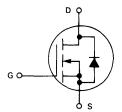
IRF710

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low rDS(on) to Minimize On-Losses. Specified at Elevated Temperature
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MAXIMUM RATINGS

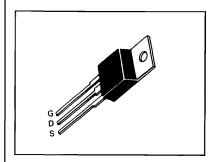
Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	400	Vdc
Drain-Gate Voltage (RGS = 1.0 M Ω)	VDGR	400	Vdc
Gate-Source Voltage	V _{GS}	± 20	Vdc
Drain Current Continuous Pulsed	I _D	1.5 6.0	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	20 0.16	Watts W/°C
Operating and Storage Temperature Range	TJ, T _{stg}	-55 to 150	°C

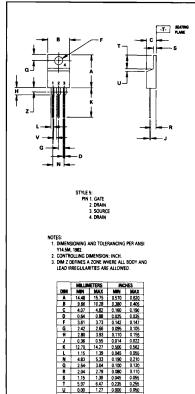
THERMAL CHARACTERISTICS

THE WINE OF MINOR ENGINEE			
Thermal Resistance			°C/W
Junction to Case	R _{€JC}	6.4	ĺ
Junction to Ambient	R ₀ JA	62.5	
Maximum Lead Temp, for	Tı	300	ů
Soldering Purposes, 1/8"			ĺ
from Case for 5 Seconds			,

Design curves of the MTP2N35 are applicable for this series of products. The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Part Number	VDSS	rDS(on)	lD
IRF710	400 V	3.6 Ω	1.5 A





CASE 221A-04

TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit	
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage $(V_{GS} = 0, I_D = 0.25 \text{ mA})$		V _{(BR)DSS}	400	-	Vdc	
Zero Gate Voltage Drain Current (VDS = Rated VDSS, VGS = 0) (VDS = 0.8 Rated VDSS, VGS = 0,	T _J = 125°C1	IDSS	_	0.25 1.00	mAdo	
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)		^I GSSF	_	500	nAdc	
Gate-Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)		^I GS\$R	-	500	nAdc	
ON CHARACTERISTICS*						
Gate Threshold Voltage (VDS = VGS, ID = 0.25 mA)		V _{GS(th)}	2.0	4.0	Vdc	
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 0.8 Adc)		「DS(on)		3.6	Ohm	
On-State Drain Current ($V_{GS} = 10 \text{ V}$) ($V_{DS} \ge 5.4 \text{ Vdc}$)		I _{D(on)}	1.5	_	Adc	
Forward Transconductance (V _{DS} ≥ 5.4 V, I _D = 0.8 A)		9FS	0.5		mhos	
DYNAMIC CHARACTERISTICS			· · · · · · ·			
Input Capacitance		Ciss		150	pF	
Output Capacitance	${V_{DS} = 25 \text{ V, V}_{GS} = 0, f = 1.0 \text{ MHz}}$	Coss	_	50		
Reverse Transfer Capacitance		C _{rss}	_	15		
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time		td(on)		10	ns	
Rise Time	$\{V_{DD} = 0.5 V_{DSS}, I_{D} = 0.8 Apk,$	tr		20		
Turn-Off Delay Time	R _{gen} = 50 Ohms)	td(off)		10		
Fall Time		tf		15		
Total Gate Charge		Qg	6.0 (Typ)	7.5	nC	
Gate-Source Charge	$(V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $V_{GS} = 10 \text{ Vdc}, I_{D} = 2.0 \text{ A})$	Qgs	3.0 (Typ)	-		
Gate-Drain Charge	VGS = 10 VdG, 10 2.0 74	a_{gd}	3.0 (Typ)			
SOURCE DRAIN DIODE CHARACTERIS	STICS*					
Forward On-Voltage	(Is ≈ 2.0 A,	V _{SD}	1.1 (Typ)	1.6	Vdc	
Forward Turn-On Time	$V_{GS} = 0$	ton	Limited by st	ray inducta	nce	
Reverse Recovery Time		t _{rr}	600 (Typ)	_	ns	
NTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw of (Measured from the drain lead 0.25		Ld	3.5 (Typ) 4.5 (Typ)	_	nH	
Internal Source Inductance	25" from package to source bond pad)	L _s	7.5 (Typ)	_		

^{*}Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%