SECTION 6
ELECTRICAL CHARACTERISTICS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock (CLKO pin) and possibly to one or more other signals.

6.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	- 0.3 to + 7.0	V
Input Voltage	V_{in}	- 0.3 to + 7.0	V
Operating Temperature Range MC68302 MC68302C	T_A	 0 to 70 - 40 to 85	°C
Storage Temperature Range	T_{stg}	- 55 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to his high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD})

6.2 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance for PGA	θ_{JA}	25	°C/W
	θ_{JC}	2	°C/W
Thermal Resistance for CQFP	θ_{JA}	40	°C/W
	θ_{JC}	15	°C/W
Thermal Resistance for PQFP	θ_{JA}	42	°C/W
	θ_{JC}	20	°C/W

$T_J = T_A + (P_D \cdot \theta_A)$
$P_D = (V_{DD} \cdot I_{DD}) + P_{I/O}$

where:
$P_{I/O}$ is the power dissipation on pins.
For T_A = 70°C and $P_{I/O}$ + 0 W, 16.67 MHz, 5.5 V, and CQFP package, the worst case value of T_J is:
T_J = 70°C + (5.5 V · 30 mA · 40°C/W) = 98.65C

6.3 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction to Ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{DD} \times V_{DD}$, Watts—Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins—User Determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected.

If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

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where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

6.4 POWER DISSIPATION

Characteristic	Symbol	Typ	Max	Unit
Power Dissipation at 25 MHz- Rev C.8μ (see Notes 1 & 2)	PD	85	130	mA
Power Dissipation at 25 MHz -Rev C.65μ (see Notes 1 & 2)	PD	65	90	mA
Power Dissipation at 20 MHz-Rev C.8μ (see Notes 1 & 2)	PD	65	100	mA
Power Dissipation at 20 MHz-Rev C.65μ (see Notes 1 & 2)	PD	50	80	mA
Power Dissipation at 16.67 MHz-Rev C.8μ (see Notes 1 & 2)	PD	54	85	mA
Power Dissipation at 16.67 MHz-Rev C.65μ (see Notes 1 & 2)	PD	44	70	mA
Power Dissipation at 4 MHz-Rev C.8μ (see Notes 1,2 & 3)	PD	40	-	mA
Power Dissipation at 4 MHz-Rev C.65μ (see Notes 1, 2 & 3)	PD	27	-	mA
Power Dissipation at 3.3V 20 MHz-Rev C.65μ (see Note 2)	PD	30	60	mA
Power Dissipation at 3.3V 16.67 MHz-Rev C.65μ (see Note 2)	PD	25	50	mA

NOTES:

1. Values measured with maximum loading of 130 pF on all output pins. Typical means 5.0 V at 25°C. Maximum means guaranteed maximum over maximum temperature (85°C) and voltage (5.5 V).
2. The IMP is tested with the M68000 core executing, all three baud rate generators enabled and clocking at a rate of 64 kHz, and the two general-purpose timers running with a prescaler of 256. Power measurements are not significantly impacted by baud rate generators or timers until their clocking frequency becomes a much more sizable fraction of the system frequency than in these test conditions.
3. The M68000 core will not operate at 4 MHz. This is only for low power mode.

6.5 DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input High Voltage (Except EXTAL)	V_{IH}	2.0	V_{DD}	V
Input Low Voltage (Except EXTAL)	V_{IL}	V_{SS} - 0.3	0.8	V
Input High Voltage (EXTAL)	V_{CIH}	4.0	VDD	V
Input Low Voltage (EXTAL)	V_{CIL}	V_{SS} - 0.3	0.6	V
Input Leakage Current	I_{IN}	—	20	µA
Input Capacitance All Pins	C_{IN}	—	15	pF
Three-State Leakage Current (2.4/0.5 V)	I_{TSI}	—	20	µA
Open Drain Leakage Current (2.4 V)	I_{OD}	—	20	µA
Output High Voltage (I_{OH} = 400 µA) (see Note)	V_{OH}	V_{DD}–1.0	—	V
Output Low Voltage	V_{OL}			
(I_{OL} = 3.2 mA) A1–A23, PB0–PB11, FC0–FC2, $\overline{CS0}$–$\overline{CS3}$		—	0.5	V
$\overline{IAC}$, $\overline{AVEC}$, $\overline{BG}$, RCLK1, RCLK2, RCLK3, TCLK1, TCLK2, TCLK3, $\overline{RTS1}$, $\overline{RTS2}$, $\overline{RTS3}$, SDS2, PA12, RXD2, RXD3, CTS2, CD2, CD3 $\overline{DREQ}$, BRG1				
(I_{OL} = 5.3 mA) $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$, $\overline{BERR}$		—	0.5	
$\overline{BGACK}$, $\overline{BCLR}$, $\overline{DTACK}$, $\overline{DACK}$, $\overline{RMC}$, D0–D15, $\overline{RESET}$				
(I_{OL} = 7.0 mA) TXD1, TXD2, TXD3		—	0.5	
(I_{OL} = 8.9 mA) $\overline{DONE}$, $\overline{HALT}$, $\overline{BR}$ (as output)		—	0.5	
(I_{OL} = 3.2 mA) CLKO		—	0.4	
Output Drive CLKO	O_{CLK}	—	50	pF
Output Drive ISDN I/F (GCI Mode)	O_{GCI}	—	150	pF
Output Drive All Other Pins	O_{ALL}	—	130	pF
Output Drive Derating Factor for CLKO of 0.030 ns/pF	O_{KF}	20	50	pF
Output Drive Derating Factor for CLKO of 0.035 ns/pF	O_{KF}	50	130	pF
Output Drive Derating Factor for All Other Pins 0.035 ns/pF	O_{KF}	20	130	pF
Output Drive Derating Factor for All Other Pins 0.055 ns/pF	O_{KF}	130	220	pF
Power	V_{DD}	4.5	5.5	V
Common	V_{SS}	0	0	V

NOTE: The maximum I_{OH} for a given pin is one-half the I_{OL} rating for that pin. For an I_{OH} between 400 µA and I_{OL}/2 mA, the minimum V_{OH} is calculated as: V_{DD} - (1 +.05 V/mA(I_{OH} -.400 mA)).

NOTE: All AC specs are assume an output load of 130pf (except for CLKO).

6.6 DC ELECTRICAL CHARACTERISTICS—NMSI1 IN IDL MODE

Characteristic	Symbol	Min	Max	Unit	Condition
Input Pin Characteristics: L1CLK, L1SY1, L1RXD, L1GR					
Input Low Level Voltage	V_{IL}	-10%	+ 20%	V	(% of V_{DD})
Input High Level Voltage	V_{IH}	V_{DD} - 20%	V_{DD} + 10%	V	
Input Low Level Current	II_L	—	± 10	µA	$V_{in} = V_{ss}$
Input High Level Current	II_H	—	± 10	µA	$V_{in} = V_{DD}$
Output Pin Characteristics: L1TXD, SDS1- SDS2, L1RQ					
Output Low Level Voltage	V_{OL}	0	1.0	V	I_{OL} = 5.0 mA
Output High Level Voltage	V_{OH}	V_{DD} - 1.0	V_{DD}	V	I_{OH} = 400 µA

6.7 AC ELECTRICAL SPECIFICATIONS—CLOCK TIMING

(see Figure 6-1, Figure 6-2, Figure 6-3, and Figure 6-4)

			16.67 MHz		20 MHz		25 MHz		
Num.	**Characteristic**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
	Frequency of Operation	f	8	16.67	8	20	8	25	MHz
1	Clock Period (EXTAL) (See note 3)	t_{cyc}	60	125	50	125	40	125	ns
2, 3	Clock Pulse Width (EXTAL)	t_{CL}, t_{CH}	25	62.5	21	62.5	16	62.5	ns
4, 5	Clock Rise and Fall Times (EXTAL)	t_{Cr}, t_{Cf}	—	5	—	4	—	4	ns
5a	EXTAL to CLKO Delay (See Notes 1 and 2)	t_{CD}	2	11	2	9	2	7	ns

NOTE:
1. CLKO loading is 50 pF max.
2. CLKO skew from the rising and falling edges of EXTAL will not differ from each other by more than 1 ns, if the EXTAL rise time equals the EXTAL fall time.
3. You may not stop the clock input at any time.

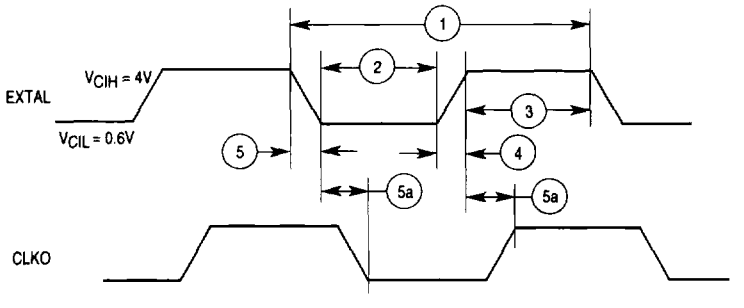


Figure 6-1. Clock Timing Diagram

6.8 AC ELECTRICAL SPECIFICATIONS—IMP BUS MASTER CYCLES

(see Figure 6-2, Figure 6-3, Figure 6-4, and Figure 6-5))

			16.67 MHz		20 MHz		25 MHz		
Num.	Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
6	Clock High to FC, Address Valid	$t_{CHFCADV}$	0	45	0	40	0	30	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	t_{CHADZ}	—	50	—	42	—	33	ns
8	Clock High to Address, FC Invalid (Minimum)	t_{CHAFI}	0	—	0	—	0	—	ns
9	Clock High to $\overline{AS}$, $\overline{DS}$ Asserted (see Note 1)	t_{CHSL}	3	30	3	25	3	20	ns
11	Address, FC Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read) $\overline{AS}$ Asserted Write (see Note 2)	t_{AFCVSL}	15	—	12	—	10	—	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated (see Note 1)	t_{CLSH}	—	30	—	25	—	20	ns
13	$\overline{AS}$, $\overline{DS}$ Negated to Address, FC Invalid (see Note 2)	t_{SHAFI}	15	—	12	—	10	—	ns
14	$\overline{AS}$ (and $\overline{DS}$ Read) Width Asserted (see Note 2)	t_{SL}	120	—	100	—	80	—	ns
14A	$\overline{DS}$ Width Asserted, Write (see Note 2)	t_{DSL}	60	—	50	—	40	—	ns
15	$\overline{AS}$, $\overline{DS}$ Width Negated (see Note 2)	t_{SH}	60	—	50	—	40	—	ns
16	Clock High to Control Bus High Impedance	t_{CHCZ}	—	50	—	42	—	33	ns
17	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid (see Note 2)	t_{SHRH}	15	—	12	—	10	—	ns
18	Clock High to R/$\overline{W}$ High (see Note 1)	t_{CHRH}	—	30	—	25	—	20	ns
20	Clock High to R/$\overline{W}$ Low (see Note 1)	t_{CHRL}	—	30	—	25	—	20	ns
20A	$\overline{AS}$ Asserted to R/$\overline{W}$ Low (Write) (see Notes 2 and 6)	t_{ASRV}	—	10	—	10	—	7	ns
21	Address FC Valid to R/$\overline{W}$ Low (Write) (see Note 2)	t_{AFCVRL}	15	—	12	—	10	—	ns
22	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write) (see Note 2)	t_{RLSL}	30	—	25	—	20	—	ns
23	Clock Low to Data-Out Valid	t_{CLDO}	—	30	—	25	—	20	ns
25	$\overline{AS}$, $\overline{DS}$, Negated to Data-Out Invalid (Write) (see Note 2)	t_{SHDOI}	15	—	12	—	10	—	ns
26	Data-Out Valid to $\overline{DS}$ Asserted (Write) (see Note 2)	t_{DOSL}	15	—	12	—	10	—	ns
27	Data-In Valid to Clock Low (Setup Time on Read) (see Note 5)	t_{DICL}	7	—	6	—	5	—	ns
28	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Asynchronous Hold) (see Note 2)	t_{SHDAH}	0	110	0	95	0	75	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	t_{SHDII}	0	—	0	—	0	—	ns
30	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{BERR}$ Negated	t_{SHBEH}	0	—	0	—	0	—	ns
31	$\overline{DTACK}$ Asserted to Data-In Valid (Setup Time) (see Notes 2 and 5)	t_{DALDI}	—	50	—	42	—	33	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	t_{RHr}, t_{RHf}	—	150	—	150	—	150	ns
33	Clock High to $\overline{BG}$ Asserted	t_{CHGL}	—	30	—	25	—	20	ns
34	Clock High to $\overline{BG}$ Negated	t_{CHGH}	—	30	—	25	—	20	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted (see Note 11)	t_{BRLGL}	2.5	4.5	2.5	4.5	2.5	4.5	clks
36	$\overline{BR}$ Negated to $\overline{BG}$ Negated (see Note 7)	t_{BRHGH}	1.5	2.5	1.5	2.5	1.5	2.5	clks

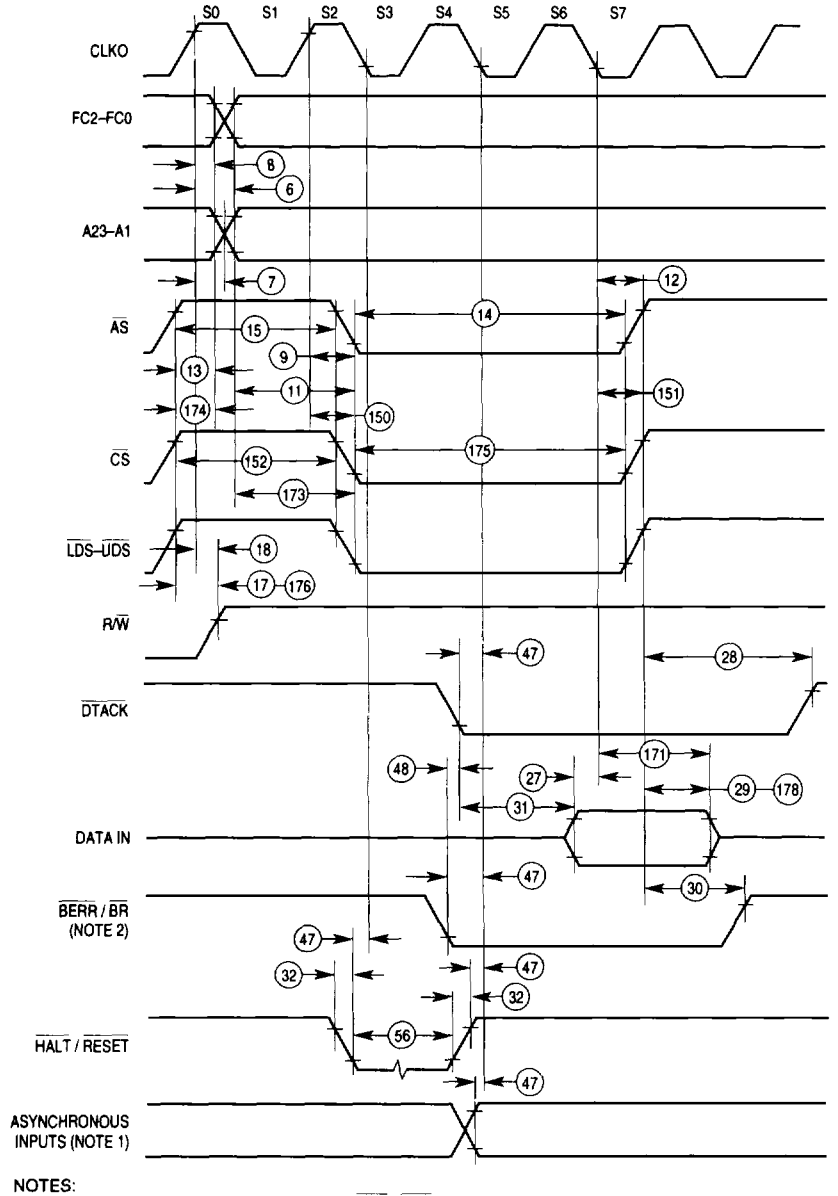
			16.67 MHz		20 MHz		25 MHz		
Num.	Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GALGH}	2.5	4.5	2.5	4.5	2.5	4.5	clks
37A	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated (see Note 8)	t_{GALBRH}	10	1.5	10	1.5	10	1.5	ns/ clks
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{AS}$ Negated)	t_{GLZ}	—	50	—	42	—	33	ns
39	$\overline{BG}$ Width Negated	t_{GH}	1.5	—	1.5	—	1.5	—	clks
40	$\overline{BGACK}$ Asserted to Address Valid	t_{GALAV}	15	—	15	—	15	—	ns
41	$\overline{BGACK}$ Asserted to $\overline{AS}$ Asserted	t_{GALASA}	30	—	30	—	20	—	ns
44	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{AVEC}$ Negated	t_{SHVPH}	0	50	0	42	0	33	ns
46	$\overline{BGACK}$ Width Low	t_{GAL}	1.5	—	1.5	—	1.5	—	clks
47	Asynchronous Input Setup Time (see Note 5)	t_{ASI}	10	—	10	—	7	—	ns
48	$\overline{BERR}$ Asserted to $\overline{DTACK}$ Asserted (see Notes 2 and 3)	t_{BELDAL}	10	—	10	—	7	—	ns
53	Data-Out Hold from Clock High	t_{CHDOI}	0	—	0	—	0	—	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RLDBD}	0	—	0	—	0	—	ns
56	$\overline{HALT}$/$\overline{RESET}$ Pulse Width (see Note 4)	t_{HRPW}	10	—	10	—	10	—	clks
57	$\overline{BGACK}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	t_{GASD}	1.5	—	1.5	—	1.5	—	clks
57A	$\overline{BGACK}$ Negated to FC	t_{GAFD}	1	—	1	—	1	—	clks
58	$\overline{BR}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven (see Note 7)	t_{RHSD}	1.5	—	1.5	—	1.5	—	clks
58A	$\overline{BR}$ Negated to FC (see Note 7)	t_{RHFD}	1	—	1	—	1	—	clks
60	Clock High to $\overline{BCLR}$ Asserted	t_{CHBCL}	—	30	—	25	—	20	ns
61	Clock High to $\overline{BCLR}$ High Impedance (See Note 10)	t_{CHBCH}	—	30	—	25	—	20	ns
62	Clock Low (S0 Falling Edge during read) to $\overline{RMC}$ Asserted	t_{CLRML}	—	30	—	25	—	20	ns
63	Clock High (during write) to $\overline{RMC}$ Negated	t_{CHRMH}	—	30	—	25	—	20	ns
64	$\overline{RMC}$ Negated to $\overline{BG}$ Asserted (see Note 9)	t_{RMHGL}	—	30	—	25	—	20	ns

NOTES:

1. For loading capacitance of less than or equal to 50 pF, subtract 4 ns from the value given in the maximum columns.
2. Actual value depends on clock period since signals are driven/latched on different CLKO edges. To calculate the actual spec for other clock frequencies, the user may derive the formula for each specification. First, derive the margin factor as:
   M = N(P/2) - Sa
   where N is the number of one-half CLKO periods between the two events as derived from the timing diagram, P is the rated clock period of the device for which the specs were derived (e.g., 60 ns with a 16.67-MHz device or 50 ns with a 20 MHz device), and Sa is the actual spec in the data sheet. Thus, for spec 14 at 16.67 MHz:
   M = 5(60 ns/2) - 120 ns = 30 ns.
   Once the margin (M) is calculated for a given spec, a new value of that spec (Sn) at another clock frequency with period (Pa) is calculated as:
   Sn = N(Pa/2) - M
   Thus for spec 14 at 12.5 MHz:
   Sn = 5(80 ns/2) - 30 ns = 170 ns.
   These two formulas assume a 50% duty cycle. Otherwise, if N is odd, the previous values N(P/2) and N(Pa/2) must be reduced by X, where X is the difference between the nominal pulse width and the minimum pulse width of the EXTAL input clock for that duty cycle.
3. If #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, #48 may be ignored. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is a

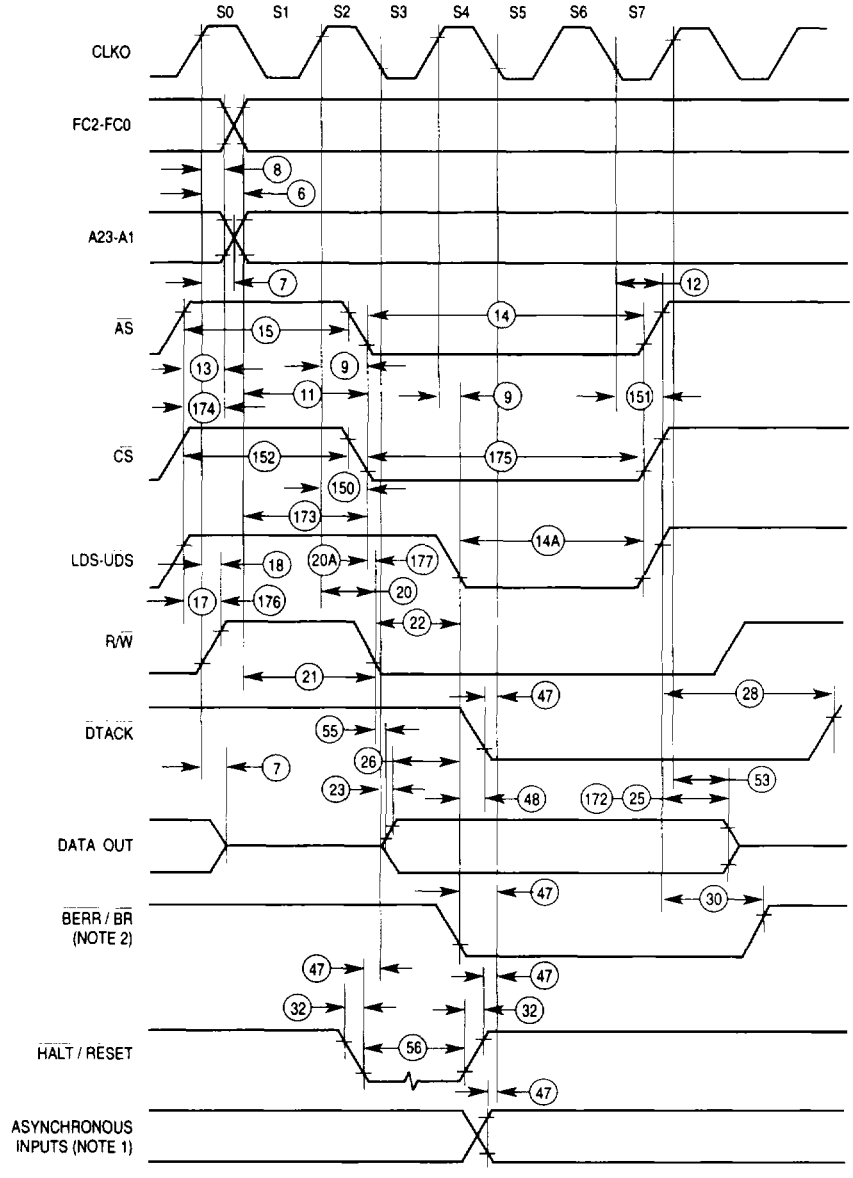
synchronous input using the asynchronous input setup time (#47).

4. For power-up, the MC68302 must be held in the reset state for 100 ms to allow stabilization of on-chip circuit. After the system is powered up #56 refers to the minimum pulse width required to reset the processor.
5. If the asynchronous input setup (#47) requirement is satisfied for $\overline{DTACK}$, the $\overline{DTACK}$ asserted to data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle.
6. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), subtract 5 ns from the values given in these columns.
7. The MC68302 will negate $\overline{BG}$ and begin driving the bus if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
8. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.
9. This specification is valid only when the RMCST bit is set in the SCR register.
10. Occurs on S0 of SDMA read/write access when the SDMA becomes bus master.
11. Specification may be exceeded during the TAS instruction if the RMCST bit in the SCR is set.



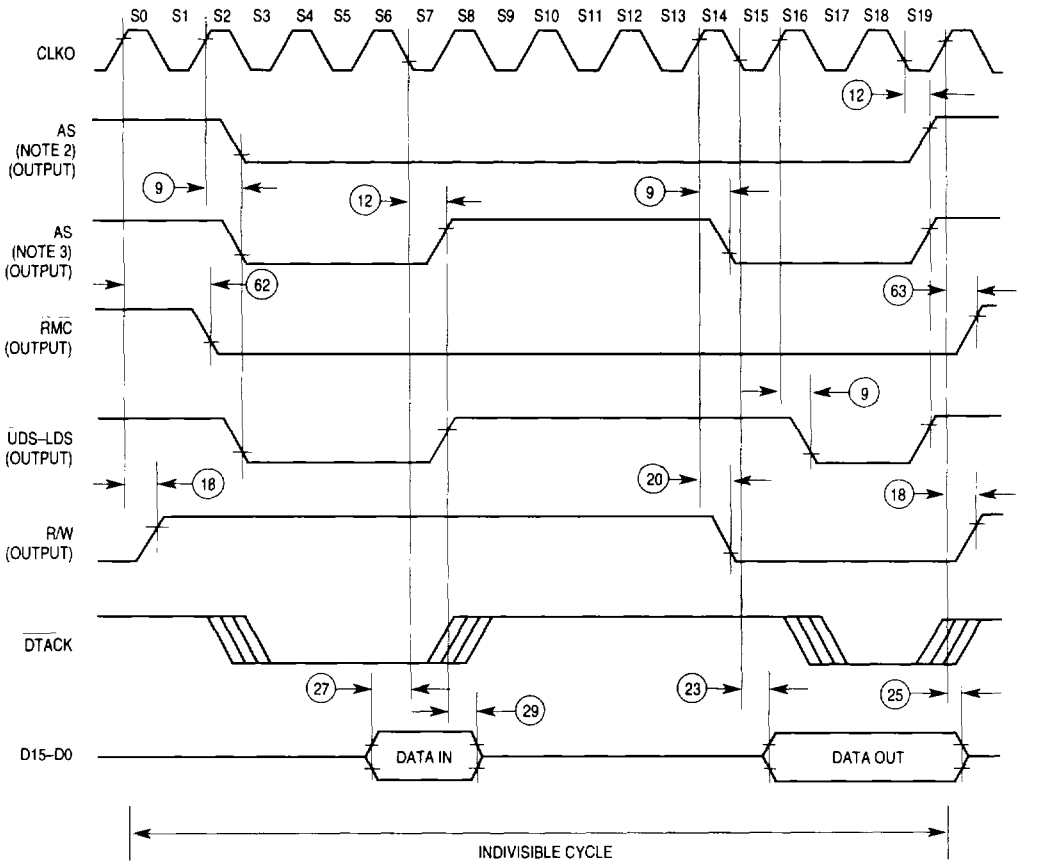
NOTES:
1. Setup time for the asynchronous inputs IPL2–IPL0 guarantees their recognition at the next falling edge of the clock.
2. BR need fall at this time only to insure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 volts and 2.0 volts.

Figure 6-2. Read Cycle Timing Diagram



NOTES:
1. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between between 0.8 volt and 2.0 volts.
2. Because of loading variations, R/W may be valid after AS even though both are initiated by the rising edge of S2 (specification #20A)
3. Each wait state is a full clock cycle inserted between S4 and S5.

Figure 6-3. Write Cycle Timing Diagram



NOTES:
1. For other timings than RMC, see Figures 6-2 and 6-3.
2. RMCST = 0 in the SCR.
3. RMCST = 1 in the SCR.
4. Wait states may be inserted between S4 and S5 during the write cycle and between S16 and S17 during the read cycle.
5. Read-modify-write cycle is generated only by the TAS instruction.

Figure 6-4. Read-Modify-Write Cycle Timing Diagram

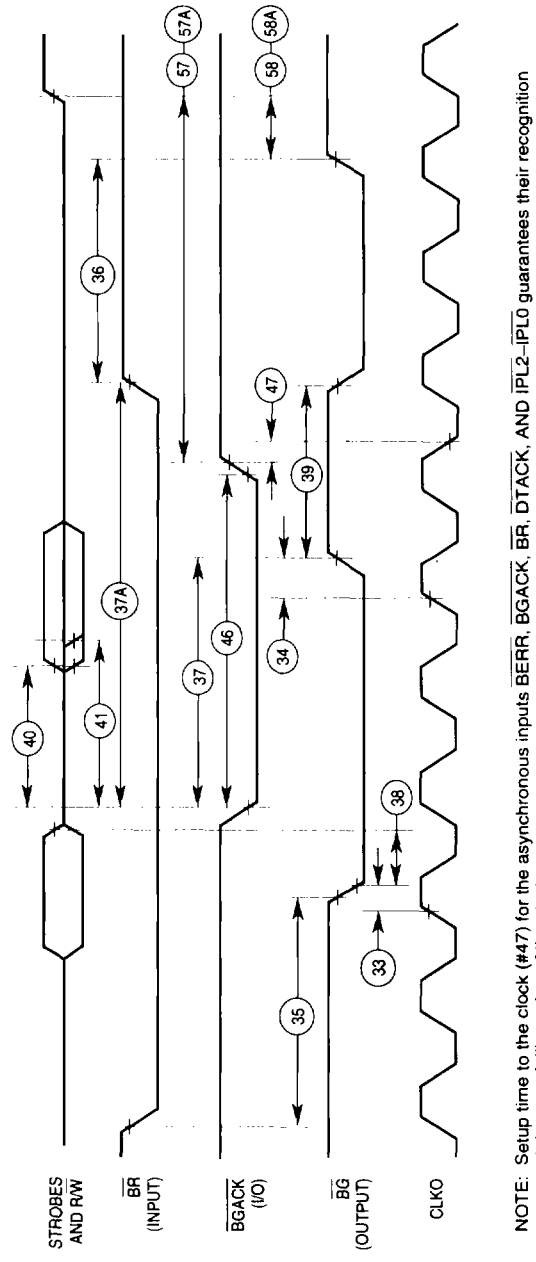
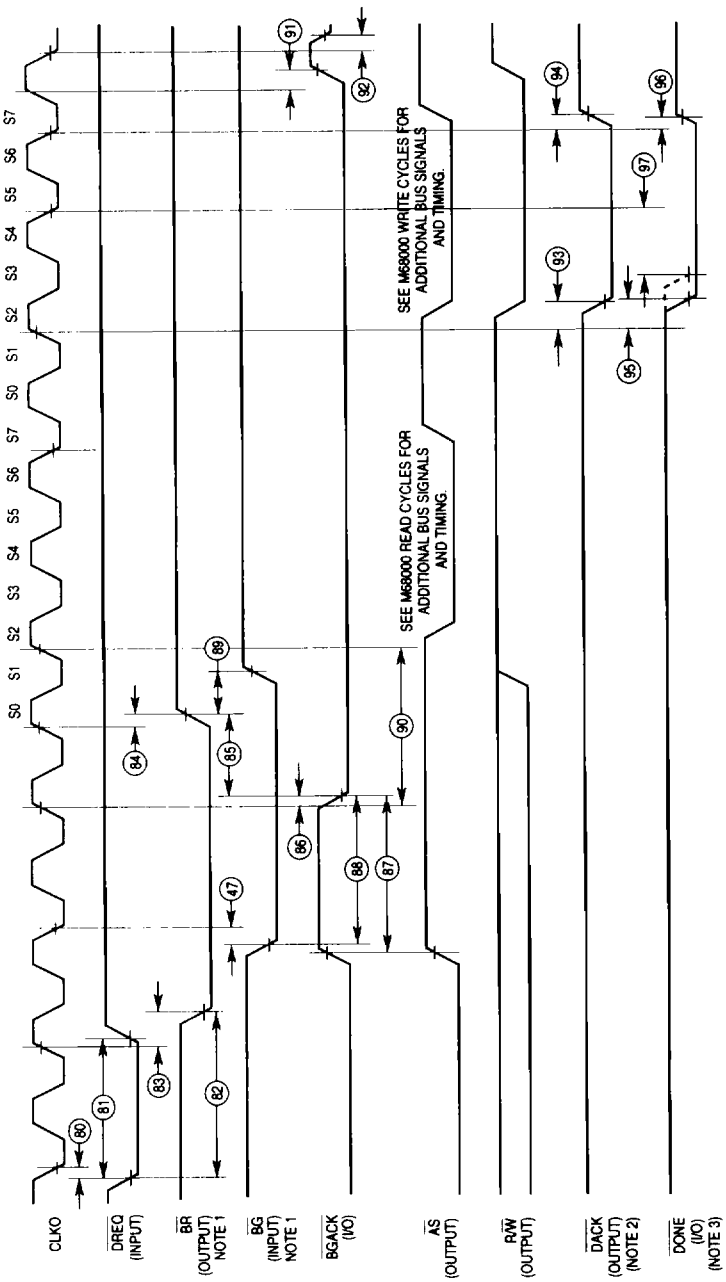


Figure 6-5. Bus Arbitration Timing Diagram

6.9 AC ELECTRICAL SPECIFICATIONS—DMA (see Figure 6-6 and Figure 6-7)

Num.	Characteristic	Symbol	16.67 MHz		20 MHz		25 MHz		Unit
			Min	Max	Min	Max	Min	Max	
80	$\overline{DREQ}$ Asynchronous Setup Time (see Note 1)	t_{REQASI}	15	—	15	—	10	—	ns
81	$\overline{DREQ}$ Width Low (see Note 2)	t_{REQL}	2	—	2	—	2	—	clks
82	$\overline{DREQ}$ Low to $\overline{BR}$ Low (see Notes 3 and 4)	$t_{REQLBRL}$	—	2	—	2	—	2	clks
83	Clock High to $\overline{BR}$ Low (see Notes 3 and 4)	t_{CHBRL}	—	30	—	25	—	20	ns
84	Clock High to $\overline{BR}$ High Impedance (see Notes 3 and 4)	t_{CHBRZ}	—	30	—	25	—	20	ns
85	$\overline{BGACK}$ Low to $\overline{BR}$ High Impedance (see Notes 3 and 4)	t_{BKLBRZ}	30	—	25	—	20	—	ns
86	Clock High to $\overline{BGACK}$ Low	t_{CHBKL}	—	30	—	25	—	20	ns
87	$\overline{AS}$ and $\overline{BGACK}$ High (the Latest One) to $\overline{BGACK}$ Low (when $\overline{BG}$ Is Asserted)	t_{ABHBKL}	1.5	2.5 +30	1.5	2.5 +25	1.5	2.5 +20	clks ns
88	$\overline{BG}$ Low to $\overline{BGACK}$ Low (No Other Bus Master) (see Notes 3 and 4)	t_{BGLBKL}	1.5	2.5 +30	1.5	2.5 +25	1.5	2.5 +20	clks ns
89	$\overline{BR}$ High Impedance to $\overline{BG}$ High (see Notes 3 and 4)	t_{BRHBGH}	0	—	0	—	0	—	ns
90	Clock on which $\overline{BGACK}$ Low to Clock on which $\overline{AS}$ Low	$t_{CLBKLAL}$	2	2	2	2	2	2	clks
91	Clock High to $\overline{BGACK}$ High	t_{CHBKH}	—	30	—	25	—	20	ns
92	Clock Low to $\overline{BGACK}$ High Impedance	t_{CLBKZ}	—	15	—	15	—	10	ns
93	Clock High to $\overline{DACK}$ Low	t_{CHACKL}	—	30	—	25	—	20	ns
94	Clock Low to $\overline{DACK}$ High	t_{CLACKH}	—	30	—	25	—	20	ns
95	Clock High to $\overline{DONE}$ Low (Output)	t_{CHDNL}	—	30	—	25	—	20	ns
96	Clock Low to $\overline{DONE}$ High Impedance	t_{CLDNZ}	—	30	—	25	—	20	ns
97	$\overline{DONE}$ Input Low to Clock Low (Asynchronous Setup)	t_{DNLTCH}	15	—	15	—	10	—	ns

NOTES:
1. $\overline{DREQ}$ is sampled on the falling edge of CLK in cycle steal and burst modes.
2. If #80 is satisfied for $\overline{DREQ}$, #81 may be ignored.
3. $\overline{BR}$ will not be asserted while $\overline{BG}$, $\overline{HALT}$, or $\overline{BERR}$ is asserted.
4. Specifications are for DISABLE CPU mode only.
5. $\overline{DREQ}$, $\overline{DACK}$, and $\overline{DONE}$ do not apply to the SDMA channels.
6. DMA and SDMA read and write cycle timing is the same as that for the M68000 core.



NOTES:
1. BR and BG shown above are only active in disable CPU mode; otherwise, they do not apply to the diagram.
2. Assumes the ECO bit in the CMR = 1.
3. For the case when DONE is an input, assumes ECO bit in the CMR = 1.

Figure 6-6. DMA Timing Diagram (IDMA)

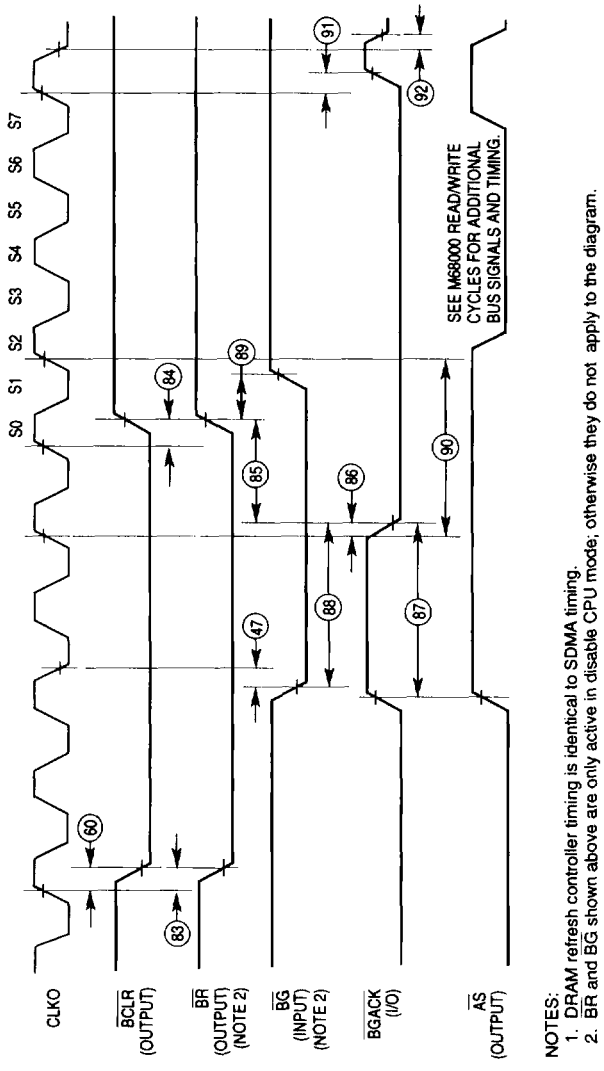


Figure 6-7. DMA Timing Diagram (SDMA)

6.10 AC ELECTRICAL SPECIFICATIONS—EXTERNAL MASTER INTERNAL ASYNCHRONOUS READ/WRITE CYCLES

(see Figure 6-8 and Figure 6-9)

			16.67 MHz		20 MHz		25 MHz		
Num.	Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
100	R/$\overline{W}$ Valid to $\overline{DS}$ Low	t_{RWVDSL}	0	—	0	—	0	—	ns
101	$\overline{DS}$ Low to Data-In Valid	t_{DSLDIV}	—	30	—	25	—	20	ns
102	$\overline{DTACK}$ Low to Data-In Hold Time	t_{DKLDH}	0	—	0	—	0	—	ns
103	$\overline{AS}$ Valid to $\overline{DS}$ Low	t_{ASVDSL}	0	—	0	—	0	—	ns
104	$\overline{DTACK}$ Low to $\overline{AS}$, $\overline{DS}$ High	t_{DKLDSH}	0	—	0	—	0	—	ns
105	$\overline{DS}$ High to $\overline{DTACK}$ High	t_{DSHDKH}	—	45	—	40	—	30	ns
106	$\overline{DS}$ Inactive to $\overline{AS}$ Inactive	t_{DSIASI}	0	—	0	—	0	—	ns
107	$\overline{DS}$ High to R/$\overline{W}$ High	t_{DSHRWH}	0	—	0	—	0	—	ns
108	$\overline{DS}$ High to Data High Impedance	t_{DSHDZ}	—	45	—	40	—	30	ns
108A	$\overline{DS}$ High to Data-Out Hold Time (see Note)	t_{DSHDH}	0	—	0	—	0	—	ns
109A	Data Out Valid to $\overline{DTACK}$ Low	t_{DOVDKL}	15	—	15	—	10	—	ns

NOTE: If $\overline{AS}$ is negated before $\overline{DS}$, the data bus could be three-stated (spec 126) before $\overline{DS}$ is negated.

6

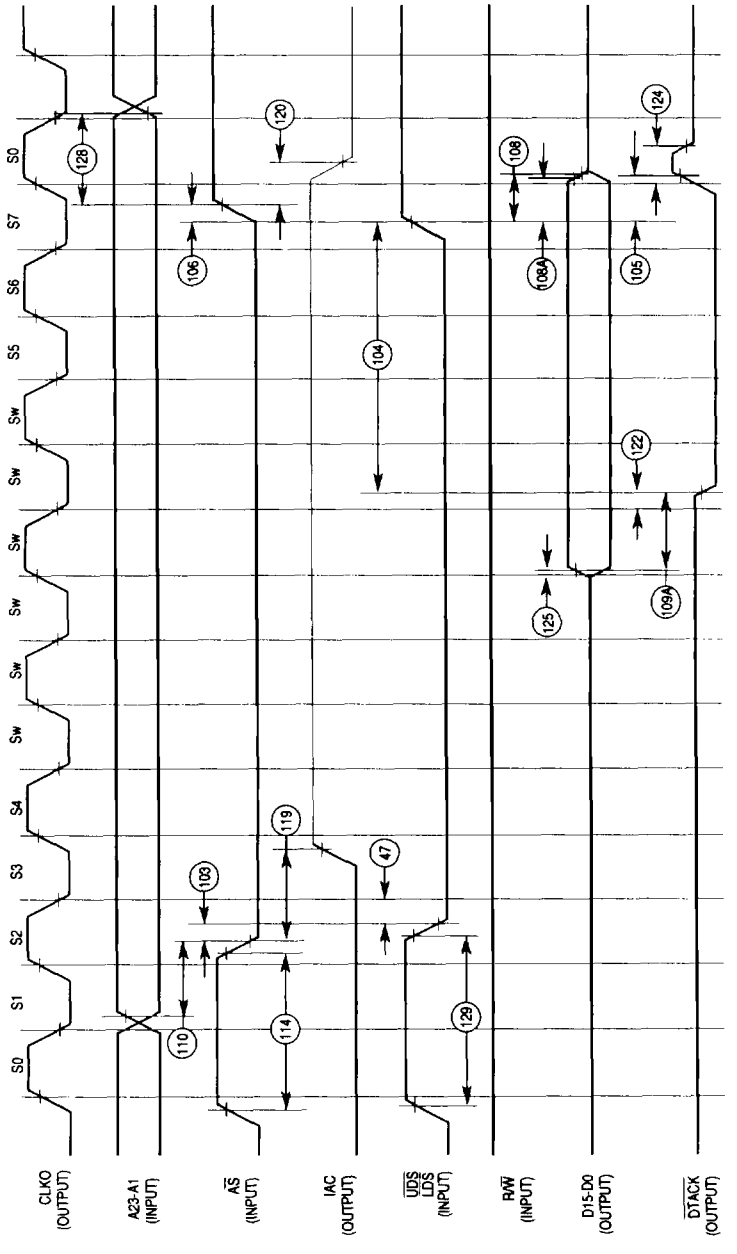


Figure 6-8. External Master Internal Asynchronous Read Cycle Timing Diagram

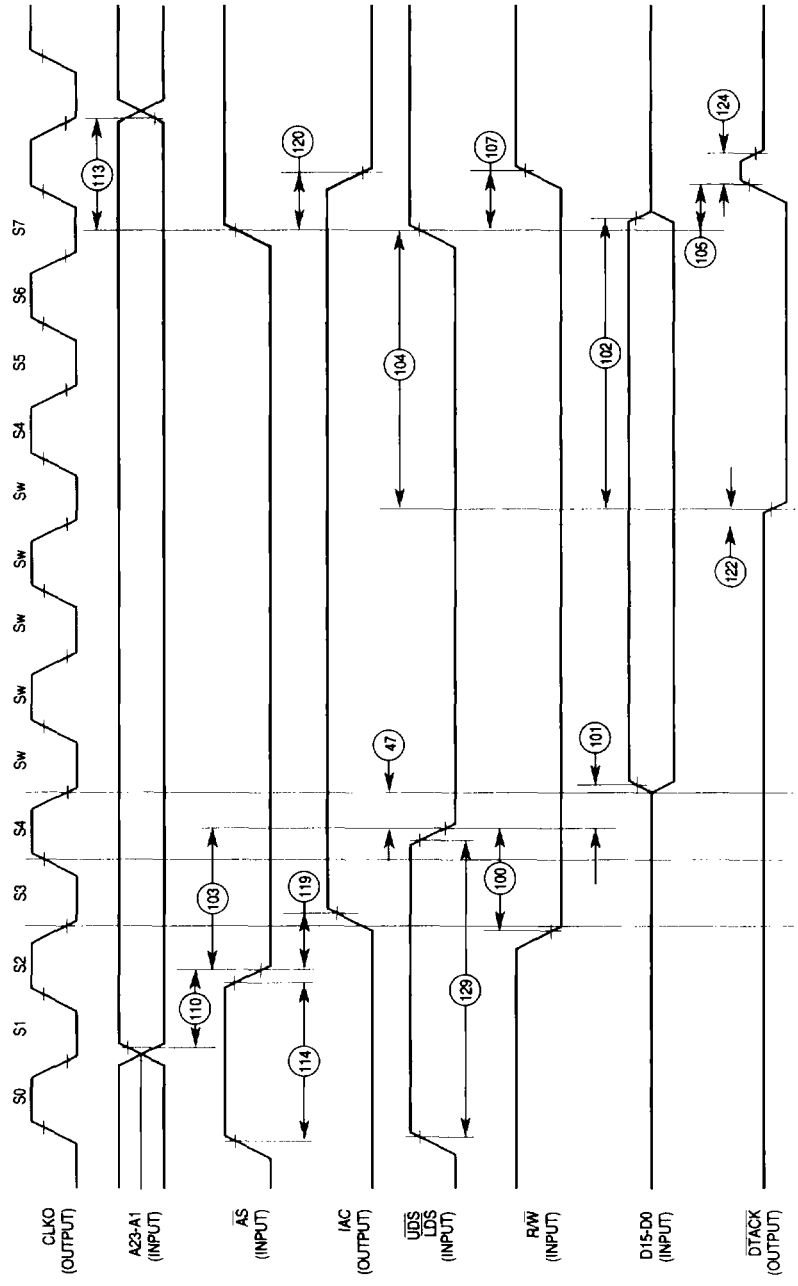


Figure 6-9. External Master Internal Asynchronous Write Cycle Timing Diagram

6.11 AC ELECTRICAL SPECIFICATIONS—EXTERNAL MASTER INTERNAL SYNCHRONOUS READ/WRITE CYCLES

(see Figure 6-10, Figure 6-11, and Figure 6-12)

			16.67 MHz		20 MHz		25 MHz		
Num.	Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
110	Address Valid to $\overline{AS}$ Low	t_{AVASL}	15	—	12	—	10	—	ns
111	$\overline{AS}$ Low to Clock High	t_{ASLCH}	30	—	25	—	20	—	ns
112	Clock Low to $\overline{AS}$ High	t_{CLASH}	—	45	—	40	—	30	ns
113	$\overline{AS}$ High to Address Hold Time on Write	t_{ASHAH}	0	—	0	—	0	—	ns
114	$\overline{AS}$ Inactive Time	t_{ASH}	1	—	1	—	1	—	clk
115	$\overline{UDS}/\overline{LDS}$ Low to Clock High (see Note 2)	t_{SLCH}	40	—	33	—	27	—	ns
116	Clock Low to $\overline{UDS}/\overline{LDS}$ High	t_{CLSH}	—	45	—	40	—	30	ns
117	R/$\overline{W}$ Valid to Clock High (see Note 2)	t_{RWVCH}	30	—	25	—	20	—	ns
118	Clock High to R/$\overline{W}$ High	t_{CHRWH}	—	45	—	40	—	30	ns
119	$\overline{AS}$ Low to IAC High	t_{ASLIAH}	—	40	—	35	—	27	ns
120	$\overline{AS}$ High to IAC Low	t_{ASHIAL}	—	40	—	35	—	27	ns
121	$\overline{AS}$ Low to $\overline{DTACK}$ Low (0 Wait State)	t_{ASLDTL}	—	45	—	40	—	30	ns
122	Clock Low to $\overline{DTACK}$ Low (1 Wait State)	t_{CLDTL}	—	30	—	25	—	20	ns
123	$\overline{AS}$ High to $\overline{DTACK}$ High	t_{ASHDTH}	—	45	—	40	—	30	ns
124	$\overline{DTACK}$ High to $\overline{DTACK}$ High Impedance	t_{DTHDTZ}	—	15	—	15	—	10	ns
125	Clock High to Data-Out Valid	t_{CHDOV}	—	30	—	25	—	20	ns
126	$\overline{AS}$ High to Data High Impedance	t_{ASHDZ}	—	45	—	40	—	30	ns
127	$\overline{AS}$ High to Data-Out Hold Time	t_{ASHDOI}	0	—	0	—	0	—	ns
128	$\overline{AS}$ High to Address Hold Time on Read	t_{ASHAI}	0	—	0	—	0	—	ns
129	$\overline{UDS}/\overline{LDS}$ Inactive Time	t_{SH}	1	—	1	—	1	—	clk
130	Data-In Valid to Clock Low	t_{CLDIV}	30	—	25	—	20	—	ns
131	Clock Low to Data-In Hold Time	t_{CLDIH}	15	—	12	—	10	—	ns

NOTES:
1. Synchronous specifications above are valid only when SAM = 1 in the SCR.
2. It is required that this signal not be asserted prior to the previous rising CLKO edge (i.e., in the previous clock cycle). It must be recognized by the IMP no sooner than the rising CLKO edge shown in the diagram.

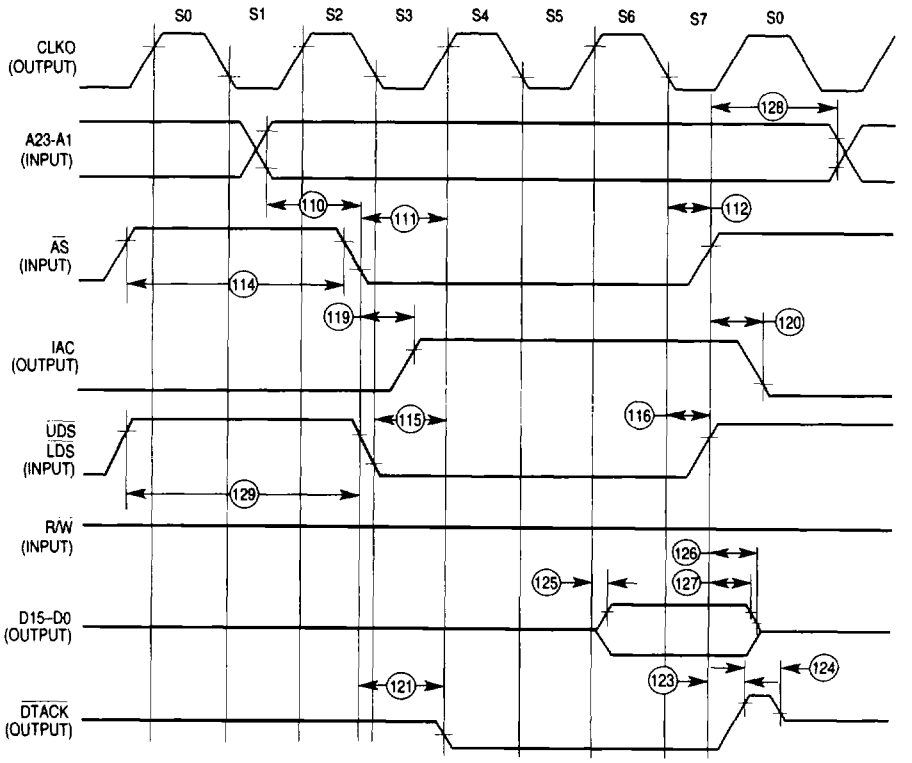


Figure 6-10. External Master Internal Synchronous Read Cycle Timing Diagram

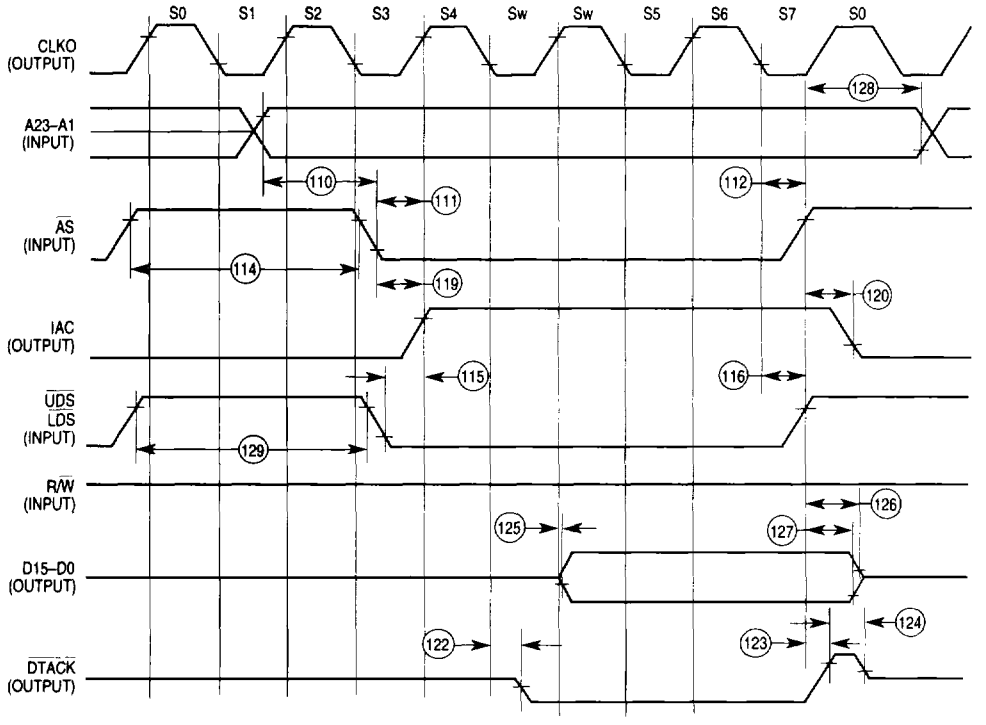


Figure 6-11. External Master Internal Synchronous Read Cycle Timing Diagram (One Wait State)

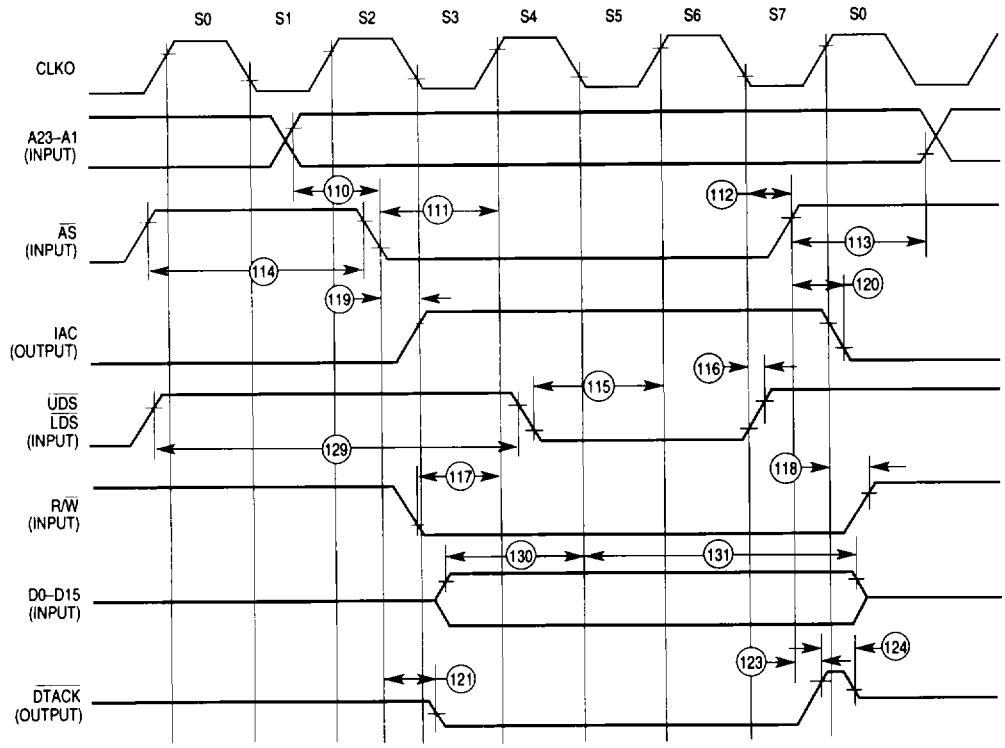


Figure 6-12. External Master Internal Synchronous Write Cycle Timing Diagram

6.12 AC ELECTRICAL SPECIFICATIONS—INTERNAL MASTER INTERNAL READ/WRITE CYCLES (see Figure 6-13)

			16.67 MHz		20 MHz		25 MHz		
Num.	**Characteristic**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
140	Clock High to IAC High	t_{CHIAH}	—	40	—	35	—	27	ns
141	Clock Low to IAC Low	t_{CLIAL}	—	40	—	35	—	27	ns
142	Clock High to $\overline{DTACK}$ Low	t_{CHDTL}	—	45	—	40	—	30	ns
143	Clock Low to $\overline{DTACK}$ High	t_{CLDTH}	—	40	—	35	—	27	ns
144	Clock High to Data-Out Valid	t_{CHDOV}	—	30	—	25	—	20	ns
145	$\overline{AS}$ High to Data-Out Hold Time	t_{ASHDOH}	0	—	0	—	0	—	ns

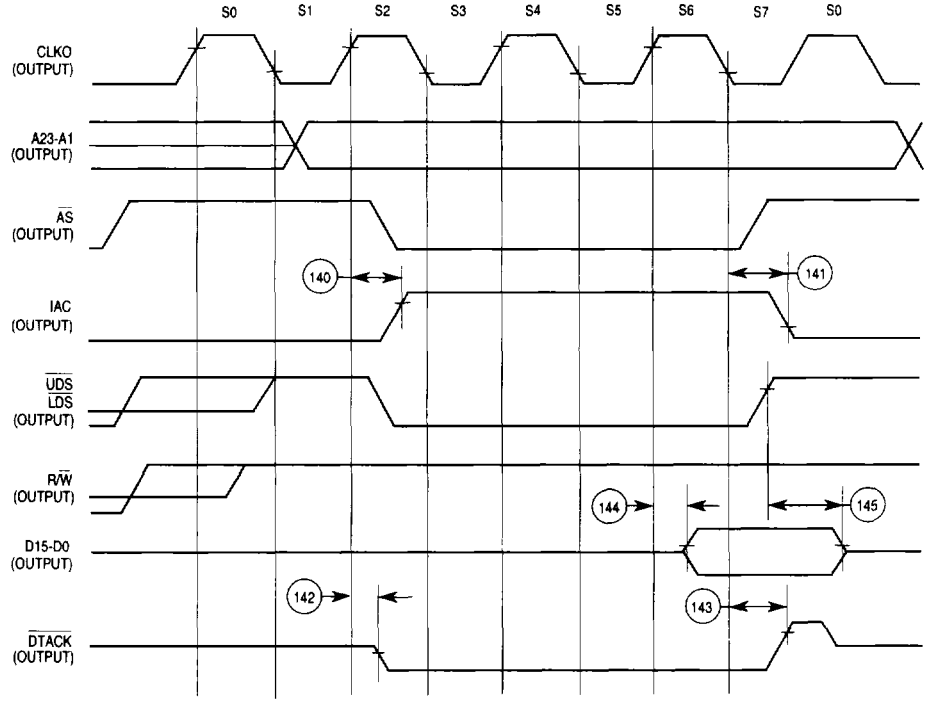


Figure 6-13. Internal Master Internal Read/Write Cycle Timing Diagram

6.13 AC ELECTRICAL SPECIFICATIONS—CHIP-SELECT TIMING INTERNAL MASTER (see Figure 6-14)

			16.67 MHz		20 MHz		25 MHz		
Num.	Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
150	Clock High to $\overline{CS}$, $\overline{IACK}$ Low (see Note 2)	$t_{CHCSIAKL}$	0	40	0	35	0	27	ns
151	Clock Low to $\overline{CS}$, $\overline{IACK}$ High (see Note 2)	$t_{CLCSIAKH}$	0	40	0	35	0	27	ns
152	$\overline{CS}$ Width Negated	t_{CSH}	60	—	50	—	40	—	ns
153	Clock High to $\overline{DTACK}$ Low (0 Wait State)	t_{CHDTKL}	—	45	—	40	—	30	ns
154	Clock Low to $\overline{DTACK}$ Low (1–6 Wait States)	t_{CLDTKL}	—	30	—	25	—	20	ns
155	Clock Low to $\overline{DTACK}$ High	t_{CLDTKH}	—	40	—	35	—	27	ns
156	Clock High to $\overline{BERR}$ Low (see Note 1)	t_{CHBERL}	—	40	—	35	—	27	ns
157	Clock Low to $\overline{BERR}$ High Impedance (see Note 1)	t_{CLBERH}	—	40	—	35	—	27	ns
158	$\overline{DTACK}$ High to $\overline{DTACK}$ High Impedance	$t_{DTKHDTKZ}$	—	15	—	15	—	10	ns
171	Input Data Hold Time from S6 Low	t_{IDHCL}	5	—	5	—	5	—	ns
172	$\overline{CS}$ Negated to Data-Out Invalid (Write)	t_{CSNDOI}	10	—	10	—	7	—	ns
173	Address, FC Valid to $\overline{CS}$ Asserted	t_{AFVCSA}	15	—	15	—	15	—	ns
174	$\overline{CS}$ Negated to Address, FC Invalid	t_{CSNAFI}	15	—	15	—	12	—	ns
175	$\overline{CS}$ Low Time (0 Wait States)	t_{CSLT}	120	—	100	—	80	—	ns
176	$\overline{CS}$ Negated to R/$\overline{W}$ Invalid	t_{CSNRWI}	10	—	10	—	7	—	ns
177	$\overline{CS}$ Asserted to R/$\overline{W}$ Low (Write)	t_{CSARWL}	—	10	—	10	—	8	ns
178	$\overline{CS}$ Negated to Data-In Invalid (Hold Time on Read)	t_{CSNDII}	0	—	0	—	0	—	ns

NOTE:

1. This specification is valid only when the ADCE or WPVE bits in the SCR are set.
2. For loading capacitance less than or equal to 50 pF, subtract 4 ns from the maximum value given.
3. Since $\overline{AS}$ and $\overline{CS}$ are asserted/negated on the same CLKO edges, no $\overline{AS}$ to $\overline{CS}$ relative timings can be specified. However, $\overline{CS}$ timings are given relative to a number of other signals, in the same manner as $\overline{AS}$. See Figure 6-2 and Figure 6-3 for diagrams.

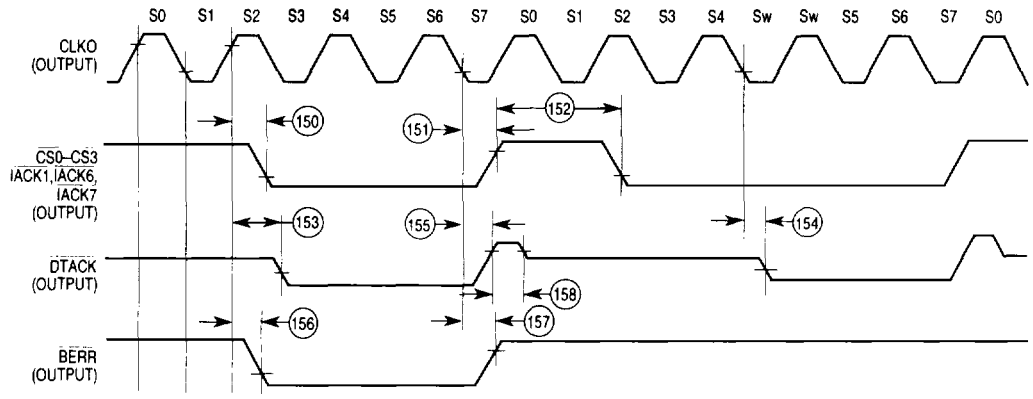


Figure 6-14. Internal Master Chip-Select Timing Diagram

6.14 AC ELECTRICAL SPECIFICATIONS—CHIP-SELECT TIMING EXTERNAL MASTER (see Figure 6-15)

			16.67 MHz		20 MHz		25 MHz		
Num.	**Characteristic**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
154	Clock Low to $\overline{DTACK}$ Low (1-6 Wait States)	t_{CLDTKL}	—	30	—	25	—	20	ns
160	$\overline{AS}$ Low to $\overline{CS}$ Low	t_{ASLCSL}	—	30	—	25	—	20	ns
161	$\overline{AS}$ High to $\overline{CS}$ High	t_{ASHCSH}	—	30	—	25	—	20	ns
162	Address Valid to $\overline{AS}$ Low	t_{AVASL}	15	—	12	—	10	—	ns
163	R/$\overline{W}$ Valid to $\overline{AS}$ Low (see Note 1)	t_{RWVASL}	15	—	12	—	10	—	ns
164	$\overline{AS}$ Negated to Address Hold Time	t_{ASHAI}	0	—	0	—	0	—	ns
165	$\overline{AS}$ Low to $\overline{DTACK}$ Low (0 Wait State)	$t_{ASLDTKL}$	—	45	—	40	—	30	ns
167	$\overline{AS}$ High to $\overline{DTACK}$ High	$t_{ASHDTKH}$	—	30	—	25	—	20	ns
168	$\overline{AS}$ Low to $\overline{BERR}$ Low (see Note 2)	$t_{ASLBERL}$	—	30	—	25	—	20	ns
169	$\overline{AS}$ High to $\overline{BERR}$ High Impedance (see Notes 2 and 3)	$t_{ASHBERH}$	—	30	—	25	—	20	ns

NOTES:
1. The minimum value must be met to guarantee write protection operation.
2. This specification is valid when the ADCE or WPVE bits in the SCR are set.
3. Also applies after a timeout of the hardware watchdog.

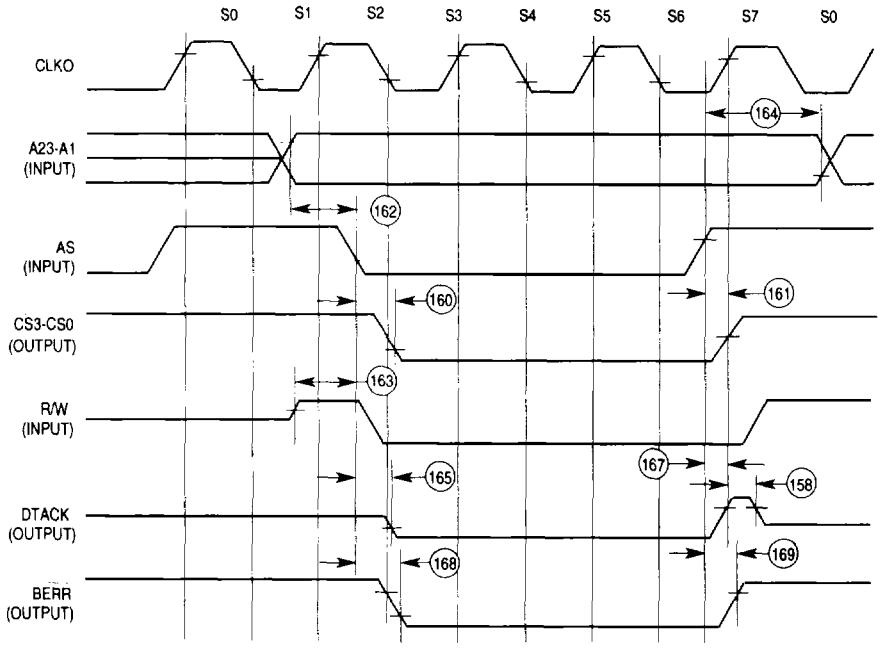


Figure 6-15. External Master Chip-Select Timing Diagram

6.15 AC ELECTRICAL SPECIFICATIONS—PARALLEL I/O

(see Figure 6-16)

			16.67 MHz		20 MHz		25 MHz		
Num.	**Characteristic**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
180	Input Data Setup Time (to Clock Low)	t_{DSU}	20	—	20	—	14	—	ns
181	Input Data Hold Time (from Clock Low)	t_{DH}	10	—	10	—	19	—	ns
182	Clock High to Data-out Valid (CPU Writes Data, Control, or Direction)	t_{CHDOV}	—	35	—	30	—	24	ns

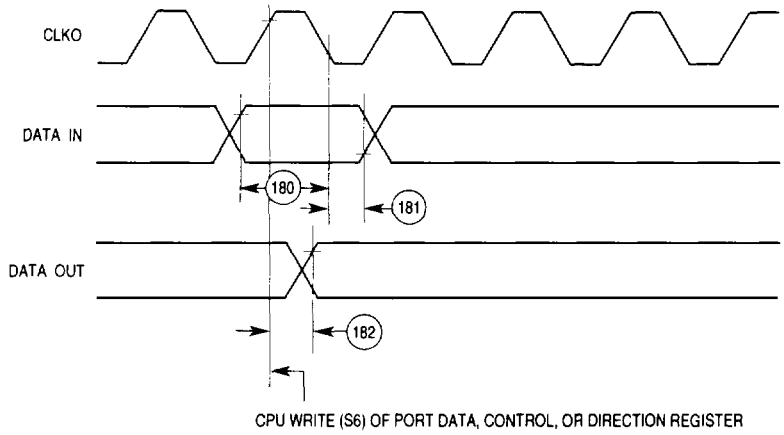


Figure 6-16. Parallel I/O Data-In/Data-Out Timing Diagram

6.16 AC ELECTRICAL SPECIFICATIONS—INTERRUPTS

(see Figure 6-17)

			16.67 MHz		20 MHz		25 MHz		
Num.	**Characteristic**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
190	Interrupt Pulse Width Low $\overline{IRQ}$ (Edge Triggered Mode) or PB8-11	t_{PW}	50	—	42	—	34	—	ns
191	Minimum Time Between Active Edges	t_{AEMT}	3	—	3	—	3	—	clk

NOTE: Setup time for the asynchronous inputs $\overline{IPL2}$–$\overline{IPL0}$ and $\overline{AVEC}$ guarantees their recognition at the next falling edge of the clock.

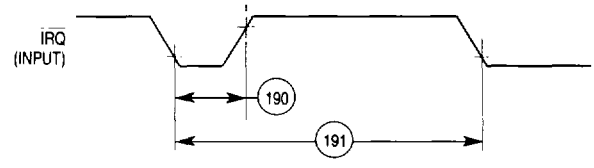


Figure 6-17. Interrupts Timing Diagram

6.17 AC ELECTRICAL SPECIFICATIONS—TIMERS

(see Figure 6-18)

			16.67 MHz		20 MHz		25 MHz		
Num.	**Characteristic**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
200	Timer Input Capture Pulse Width	t_{TPW}	50	—	42	—	34	—	ns
201	TIN Clock Low Pulse Width	t_{TICLT}	50	—	42	—	34	—	ns
202	TIN Clock High Pulse Width and Input Capture High Pulse Width	t_{TICHT}	2	—	2	—	2	—	clk
203	TIN Clock Cycle Time	t_{cyc}	3	—	3	—	3	—	clk
204	Clock High to TOUT Valid	t_{CHTOV}	—	35	—	30	—	24	ns
205	$\overline{FRZ}$ Input Setup Time (to Clock High) (see Note 1)	t_{FRZSU}	20	—	20	—	14	—	ns
206	$\overline{FRZ}$ Input Hold Time (from Clock High)	t_{FRZHT}	10	—	10	—	7	—	ns

NOTES:
1. $\overline{FRZ}$ should be negated during total system reset.
2. The TIN specs above do not apply to the use of TIN1 as a baud rate generator input clock. In such a case, specifications 1–3 may be used.

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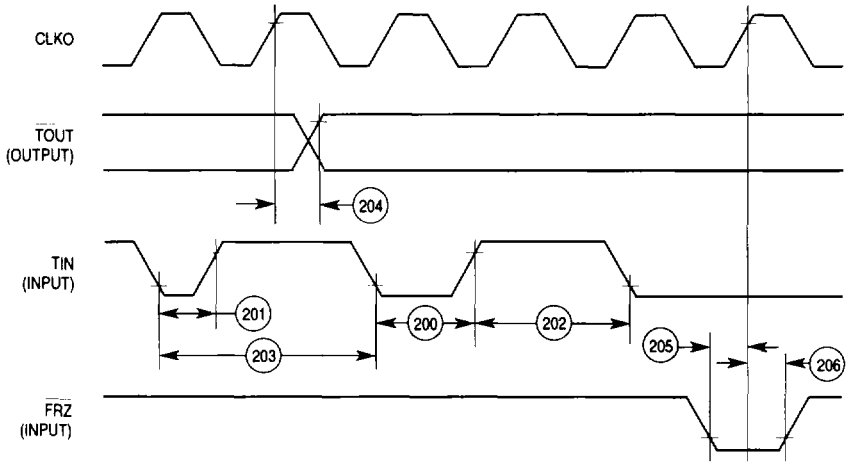


Figure 6-18. Timers Timing Diagram

6.18 AC ELECTRICAL SPECIFICATIONS—SERIAL COMMUNICATIONS PORT (see Figure 6-19).

		16.67 MHz		20 MHz		25 MHz		
Num.	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
250	SPCLK Clock Output Period	4	64	4	64	4	64	clks
251	SPCLK Clock Output Rise/Fall Time	0	15	0	10	0	8	ns
252	Delay from SPCLK to Transmit (see Note 1)	0	40	0	30	0	24	ns
253	SCP Receive Setup Time (see Note 1)	40	—	30	—	24	—	ns
254	SCP Receive Hold Time (see Note 1)	10	—	8	—	7	—	ns

NOTES:
1. This also applies when SPCLK is inverted by CI in the SPMODE register.
2. The enable signals for the slaves may be implemented by the parallel I/O pins.

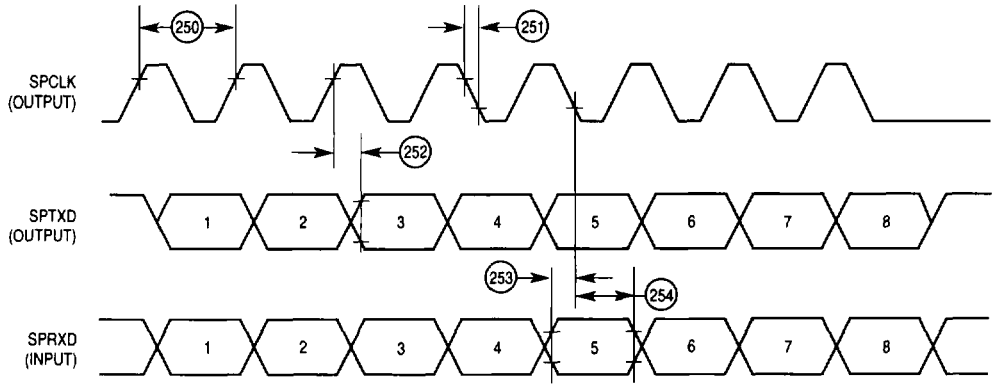


Figure 6-19. Serial Communication Port Timing Diagram

6.19 AC ELECTRICAL SPECIFICATIONS—IDL TIMING (All timing measurements, unless otherwise specified, are referenced to the L1CLK at 50% point of V_{DD}) (see Figure 6-20).

		16.67 MHz		20 MHz		25 MHz		
Num.	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
260	L1CLK (IDL Clock) Frequency (see Note 1)	—	6.66	—	8	—	10	MHz
261	L1CLK Width Low	55	—	45	—	37	—	ns
262	L1CLK Width High (see Note 3)	P+10	—	P+10	—	P+10	—	ns
263	L1TXD, L1RQ, SDS1–SDS2 Rising/Falling Time	—	20	—	17	—	14	ns
264	L1SY1 (sync) Setup Time (to L1CLK Falling Edge)	30	—	25	—	20	—	ns
265	L1SY1 (sync) Hold Time (from L1CLK Falling Edge)	50	—	40	—	34	—	ns
266	L1SY1 (sync) Inactive Before 4th L1CLK	0	—	0	—	0	—	ns
267	L1TxD Active Delay (from L1CLK Rising Edge)	0	75	0	65	0	50	ns
268	L1TxD to High Impedance (from L1CLK Rising Edge) (see Note 2)	0	50	0	42	0	34	ns
269	L1RxD Setup Time (to L1CLK Falling Edge)	50	—	42	—	34	—	ns
270	L1RxD Hold Time (from L1CLK Falling Edge)	50	—	42	—	34	—	ns
271	Time Between Successive IDL syncs	20	—	20	—	20	—	L1CLK
272	L1RQ Valid before Falling Edge of L1SY1	1	—	1	—	1	—	L1CLK
273	L1GR Setup Time (to L1SY1 Falling Edge)	50	—	42	—	34	—	ns
274	L1GR Hold Time (from L1SY1 Falling Edge)	50	—	42	—	34	—	ns
275	SDS1–SDS2 Active Delay from L1CLK Rising Edge	10	75	10	65	7	50	ns
276	SDS1–SDS2 Inactive Delay from L1CLK Falling Edge	10	75	10	65	7	50	ns

NOTES:

1. The ratio CLKO/L1CLK must be greater than 2.5/1.
2. High impedance is measured at the 30% and 70% of V_{DD} points, with the line at $V_{DD}/2$ through 10K in parallel with130 pF.
3. Where P = 1/CLKO. Thus, for a 16.67-MHz CLKO rate, P = 60 ns.

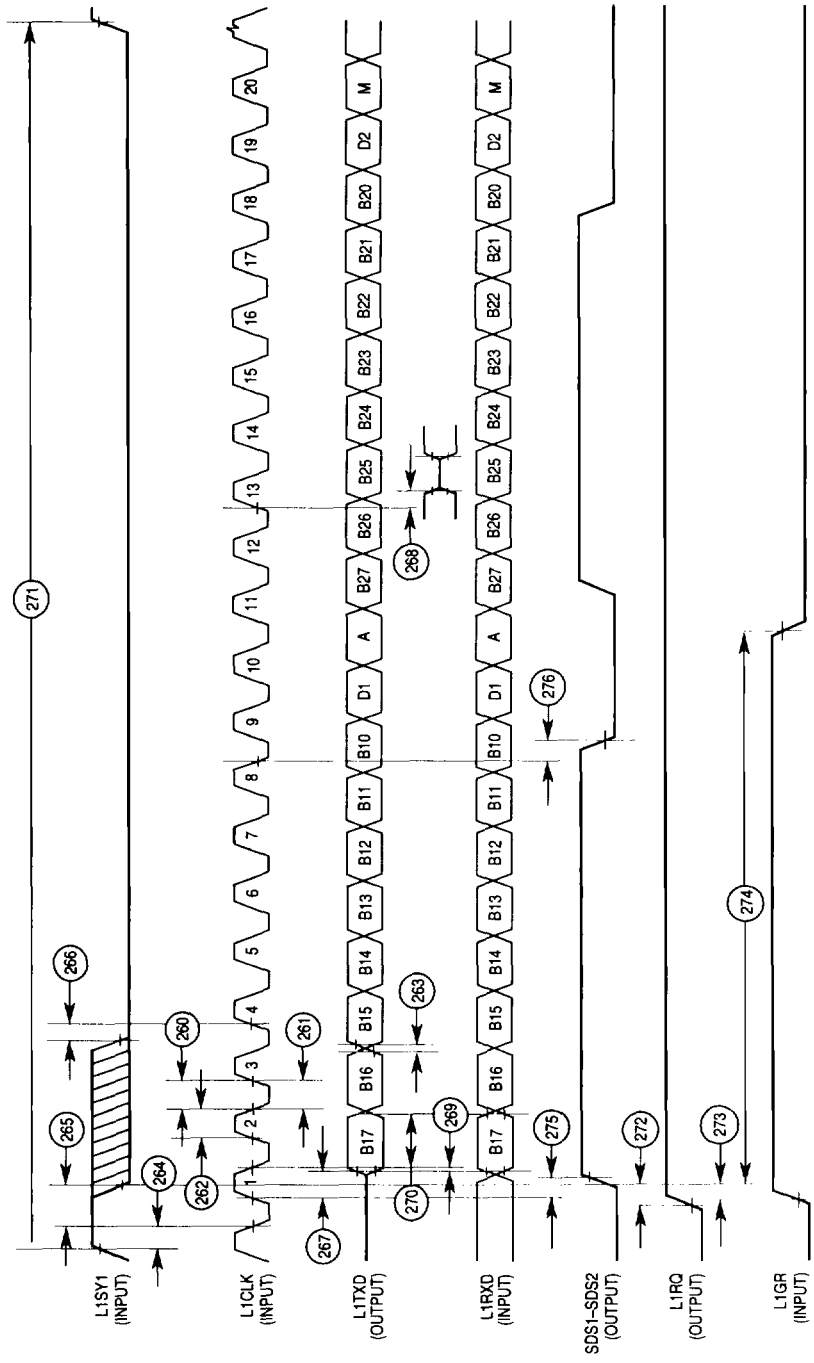


Figure 6-20. IDL Timing Diagram

6.20 AC ELECTRICAL SPECIFICATIONS—GCI TIMING

GCI supports the NORMAL mode and the GCI channel 0 (GCN0) in MUX mode. Normal mode uses 512 kHz clock rate (256K bit rate). MUX mode uses 256 x n - 3088 kbs (clock rate is data rate x 2). The ratio CLKO/L1CLK must be greater than 2.5/1 (see Figure 6-21).

		16.67 MHz		20 MHz		25 MHz		
Num.	Characteristic	Min	Max	Min	Max	Min	Max	Unit
	L1CLK GCI Clock Frequency (Normal Mode) (see Note 1)	—	512	—	512	—	512	kHz
280	L1CLK Clock Period Normal Mode (see Note 1)	1800	2100	1800	2100	1800	2100	ns
281	L1CLK Width Low/High Normal Mode	840	1450	840	1450	840	1450	ns
282	L1CLK Rise/Fall Time Normal Mode (see Note 4)	—	—	—	—	—	—	ns
	L1CLK (GCI Clock) Frequency (MUX Mode) (see Note 1)	—	6.668	—	6.668	—	6.668	MHz
280	L1CLK Clock Period MUX Mode (see Note 1)	150	—	150	—	150	—	ns
281	L1CLK Width Low MUX Mode	55	—	55	—	55	—	ns
281A	L1CLK Width High MUX Mode (see Note 5)	P+10	—	P+10	—	P+10	—	ns
282	L1CLK Rise/Fall Time MUX Mode (see Note 4)	—	—	—	—	—	—	ns
283	L1SY1 Sync Setup Time to L1CLK Falling Edge	30	—	25	—	20	—	ns
284	L1SY1 Sync Hold Time from L1CLK Falling Edge	50	—	42	—	34	—	ns
285	L1TxD Active Delay (from L1CLK Rising Edge) (see Note 2)	0	100	0	85	0	70	ns
286	L1TxD Active Delay (from L1SY1 Rising Edge) (see Note 2)	0	100	0	85	0	70	ns
287	L1RxD Setup Time to L1CLK Rising Edge	20	—	17	—	14	—	ns
288	L1RxD Hold Time from L1CLK Rising Edge	50	—	42	—	34	—	ns
289	Time Between Successive L1SY1in Normal SCIT Mode	64 192	— —	64 192	— —	64 192	— —	L1CLK L1CLK
290	SDS1–SDS2 Active Delay from L1CLK Rising Edge (see Note 3)	10	90	10	75	7	60	ns
291	SDS1–SDS2 Active Delay from L1SY1 Rising Edge (see Note 3)	10	90	10	75	7	60	ns
292	SDS1–SDS2 Inactive Delay from L1CLK Falling Edge	10	90	10	75	7	60	ns
293	GCIDCL (GCI Data Clock) Active Delay	0	50	0	42	0	34	ns

NOTES:

1. The ratio CLKO/L1CLK must be greater than 2.5/1.
2. Condition C_L = 150 pF. L1TD becomes valid after the L1CLK rising edge or L1SY1, whichever is later.
3. SDS1–SDS2 become valid after the L1CLK rising edge or L1SY1, whichever is later.
4. Schmitt trigger used on input buffer.
5. Where P = 1/CLKO. Thus, for a 16.67-MHz CLKO rate, P = 60 ns.

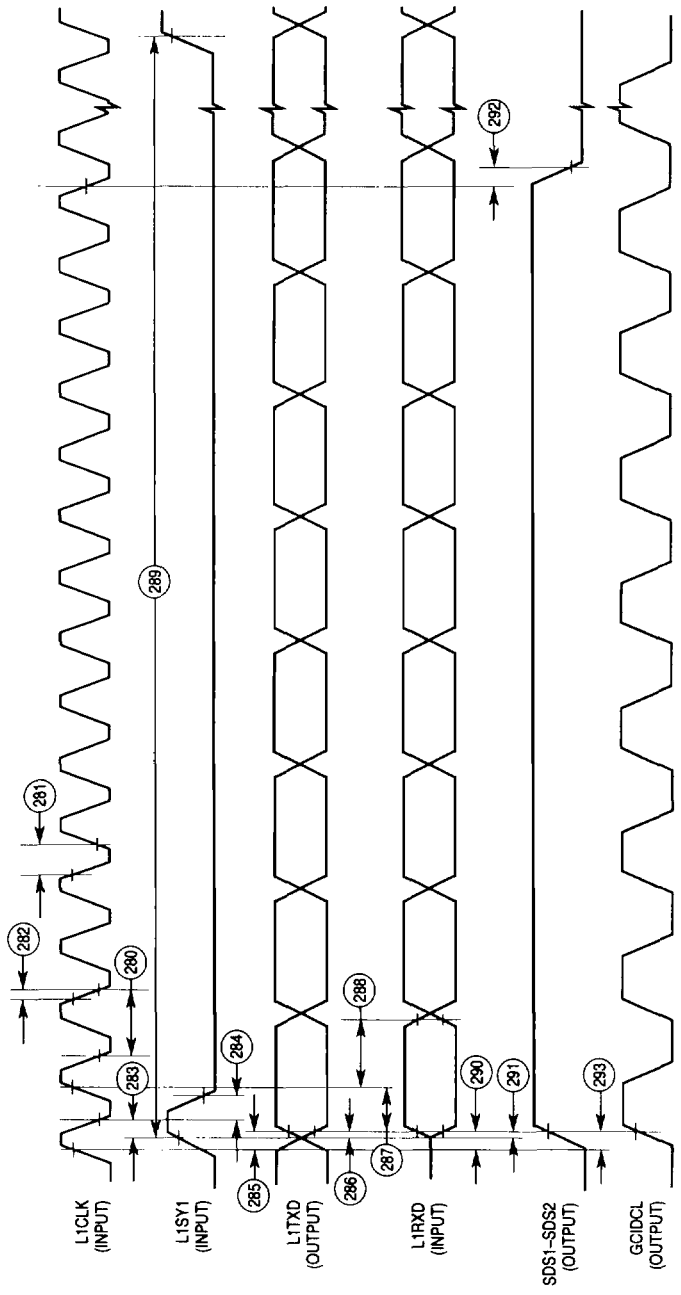


Figure 6-21. GCI Timing Diagram

6.21 AC ELECTRICAL SPECIFICATIONS—PCM TIMING

There are two sync types:

Short Frame—Sync signals are one clock cycle prior to the data
Long Frame—Sync signals are N-bits that envelope the data, N > 0; see Figure 6-22 and Figure 6-23).

		16.67 MHz		20 MHz		25 MHz		
Num.	Characteristic	Min	Max	Min	Max	Min	Max	Unit
300	L1CLK (PCM Clock) Frequency (see Note 1)	—	6.66	—	8.0	—	10.0	MHz
301	L1CLK Width Low	55	—	45	—	37	—	ns
301A	L1CLK Width High (see Note 4)	P+10	—	P+10	—	P+10	—	ns
302	L1SY0–L1SY1 Setup Time to L1CLK Rising Edge	0	—	0	—	0	—	ns
303	L1SY0–L1SY1 Hold Time from L1CLK Falling Edge	40	—	33	—	27	—	ns
304	L1SY0–L1SY1 Width Low	1	—	1	—	1	—	L1CLK
305	Time Between Successive Sync Signals (Short Frame)	8	—	8	—	8	—	L1CLK
306	L1TxD Data Valid after L1CLK Rising Edge (see Note 2)	0	70	0	60	0	47	ns
307	L1TxD to High Impedance (from L1CLK Rising Edge)	0	50	0	42	0	34	ns
308	L1RxD Setup Time (to L1CLK Falling Edge) (see Note 3)	20	—	17	—	14	—	ns
309	L1RxD Hold Time (from L1CLK Falling Edge) (see Note 3)	50	—	42	—	34	—	ns

NOTES:
1. The ratio CLK/L1CLK must be greater than 2.5/1.
2. L1TxD becomes valid after the L1CLK rising edge or the sync enable, whichever is later, if long frames are used. This note should only be used if the user can guarantee that only one sync pin (L1SY0 and L1SY1) is changed simultaneously in the selection and de-selection of the desired PCM channel time slot. A safe example of this is using only PCM CH-1. Another example is using CH-1 and CH-2 only, where CH-1 and CH-2 are not contiguous on the PCM highway.
3. Specification valid for both sync methods.
4. Where P = 1/CLKO. Thus, for a 16.67-MHz CLKO rate, P = 60 ns.

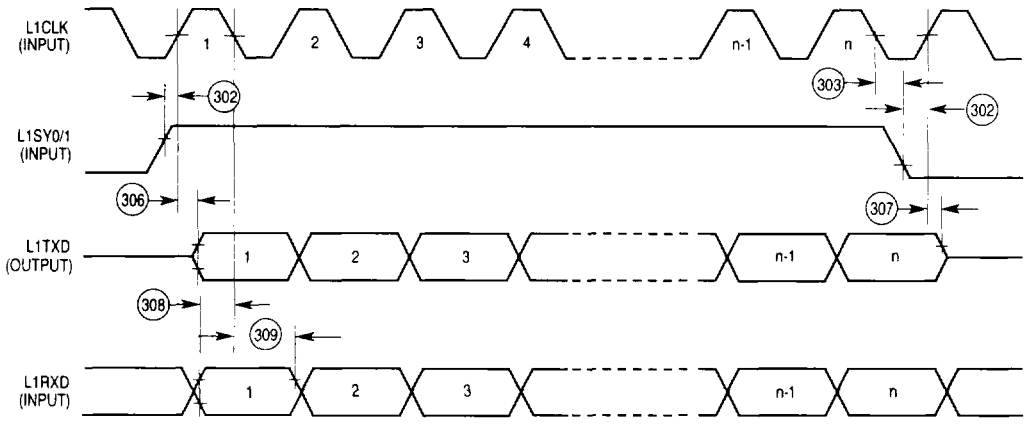
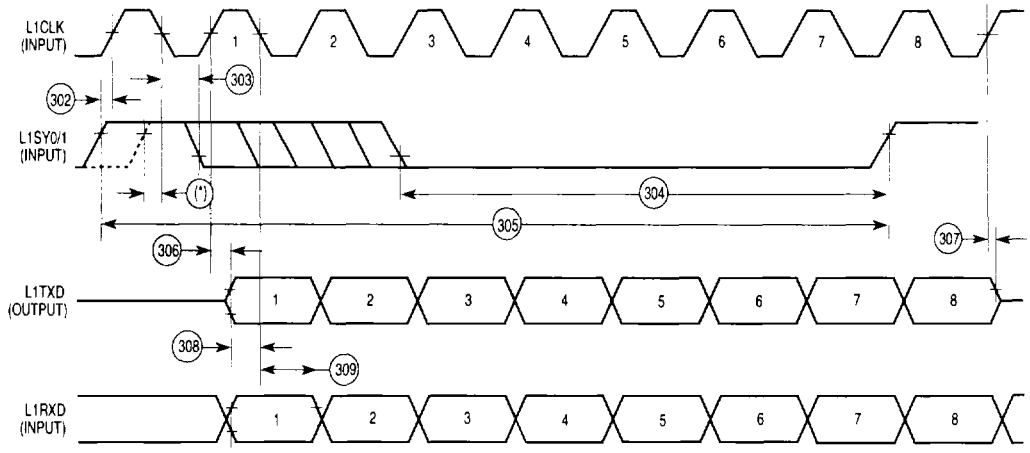


Figure 6-22. PCM Timing Diagram (SYNC Envelopes Data)



NOTE: (*) If L1SYn is guaranteed to make a smooth low to high transition (no spikes) while the clock is high, setup time can be defined as shown (min 20 ns).

Figure 6-23. PCM Timing Diagram (SYNC Prior to 8-Bit Data)

6.22 AC ELECTRICAL SPECIFICATIONS—NMSI TIMING

The NMSI mode uses two clocks, one for receive and one for transmit. Both clocks can be internal or external. When t he clock is internal, it is generated by the internal baud rate generator and it is output on TCLK or RCLK. All the timing is related to the external clock pin. The timing is specified for NMSI1. It is also valid for NMSI2 and NMSI3 (see Figure 6-24).

		16.67 MHz		16.67 MHz		20 MHz		20 MHz		25 MHz		25 MHz		
Num.	Characteristic	Internal Clock		External Clock		Internal Clock		External Clock		Internal Clock		External Clock		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
315	RCLK1 and TCLK1 Frequency (see Note 1)	—	5.55	—	6.668	—	6.66	—	8	—	8.33	—	10	MHz
316	RCLK1 and TCLK1 Low (see Note 4)	65	—	P+10	—	55	—	P+10	—	45	—	P+10	—	ns
316a	RCLK1 and TCLK1 High	65	—	55	—	55	—	45	—	45	—	35	—	ns
317	RCLK1 and TCLK1 Rise/Fall Time (see Note 3)	—	20	—	—	—	17	—	—	—	14	—	—	ns
318	TXD1 Active Delay from TCLK1 Falling Edge	0	40	0	70	0	30	0	50	0	25	0	40	ns
319	$\overline{\text{RTS1}}$ Active/Inactive Delay from TCLK1 Falling Edge	0	40	0	100	0	30	0	80	0	25	0	65	ns
320	$\overline{\text{CTS1}}$ Setup Time to TCLK1 Rising Edge	50	—	10	—	40	—	7	—	35	—	7	—	ns
321	RXD1 Setup Time to RCLK1 Rising Edge	50	—	10	—	40	—	7	—	35	—	7	—	ns
322	RXD1 Hold Time from RCLK1 Rising Edge (see Note 2)	10	—	50	—	7	—	40	—	7	—	35	—	ns
323	$\overline{\text{CD1}}$ Setup Time to RCLK1 Rising Edge	50	—	10	—	40	—	7	—	35	—	7	—	ns

NOTES:

1. The ratio CLKO/TCLK1 and CLKO/RCLK1 must be greater than or equal to 2.5/1 for external clock. The input clock to the baud rate generator may be either an internal clock or TIN1, and may be as fast as EXTAL. However, the output of the baud rate generator must provide a CLKO/TCLK1 and CLKO/RCLK1 ratio greater than or equal to 3/1. In asynchronous mode (UART), the bit rate is 1/16 of the TCLK1/RCLK1 clock rate.
2. Also applies to $\overline{\text{CD}}$ hold time when $\overline{\text{CD}}$ is used as an external sync in BISYNC or totally transparent mode.
3. Schmitt triggers used on input buffers.
4. Where P = 1/CLKO. Thus, for a 16.67-MHz CLKO rate, P = 60 ns.

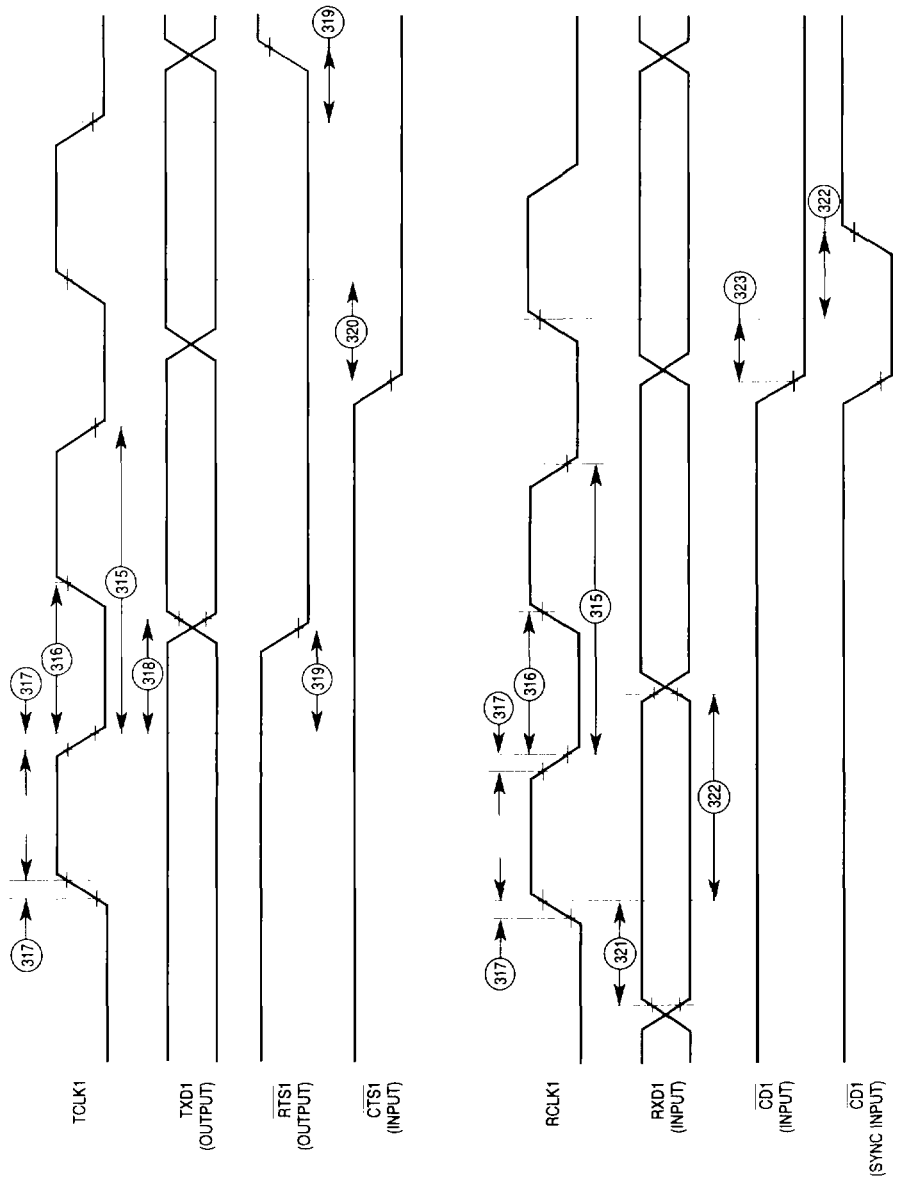


Figure 6-24. NMSI Timing Diagram