



HR1210

Multi-Mode PFC and Current Mode LLC Digital Combo Controller Configurable through UART Interface

DESCRIPTION

The HR1210 is a multi-mode PFC and current mode LLC combo controller that is configurable through a UART interface. This power-saving device achieves optimal power supply efficiency over a wide operating range.

The device uses a PFC controller with a patented digital average current control scheme to achieve hybrid CCM and DCM operation. DCM operation reduces the switching frequency under light loads to improve efficiency. Higher power factor (PF) is achieved under light loads with a digital input capacitor and current compensation method. Under heavy loads, CCM operation reduces the peak current in MOSFETs, so the controller can be implemented across a wide load range.

The HR1210 implements current control mode in the LLC stage to easily achieve stability and fast response. In addition, three operation modes are implemented based on the load conditions: steady state mode, skip mode, and burst mode. This optimizes efficiency in different load conditions independently. The key zero-voltage switching (ZVS) feature of the LLC converter greatly benefits the efficiency performance; this feature is guaranteed by the adaptive dead time of the high-side and low-side gate drivers. Any capacitive operation is effectively prevented in the HR1210.

The device uses a high-voltage current source within the IC for start-up. The traditional start-up resistor or external circuit can be removed. The high-voltage current source is also implemented as an X-capacitor (also called a Class X capacitor) discharger when the AC input is in dropout mode, so the resistor for the X-capacitor discharger can be removed.

Protection features include over-temperature protection (OTP), PFC open-loop protection (OLP), over-voltage protection (OVP), over-current limit (OCL), LLC over-current protection (OCP), SO pin protection, and over-power protection (OPP). The HR1210 is available in SOIC-20 and TSSOP-20 packages.

FEATURES

General System Features

- HV Current Source for Start-Up
- Smart X-Capacitor Discharges during AC Dropout, Approved by IEC62368 and IEC60950
- UART Interface to Configure Parameters
- User-Friendly GUI

PFC Controller

- CCM/DCM Multi Mode PFC Control with High Efficiency from Light-Load to Full Load
- Operate up to 250kHz
- High PF from Input Capacitor Current Compensation
- Configurable Frequency Jittering
- Configurable Soft Start
- Configurable AC input Brown-In/Out
- Cycle-by-Cycle Current Limit
- OLP, OVP Protection

LLC Controller

- 600V High-Side Gate Driver with Integrated Bootstrap Diode and High dV/dt Immunity
- Current Mode Control
- Operate up to 500kHz in Steady State Mode
- Adaptive Dead Time Adjustment with Minimum and Maximum Limit
- Burst/Skip Mode Switching at Light Load
- Configurable Soft Start
- Configurable DC Input Brown-In/Out
- Capacitive Mode Protection
- OCP, OPP Protection with Auto-Restart or Latch
- Configurable Protection on SO Pin

APPLICATIONS

- Desktop PCs and ATX Power Supplies
- All-in-One Gaming Power Supplies
- Notebook Adapters
- LCD TV and Plasma TV Power Supplies
- Power Tool Power Supplies
- LED Drivers

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TYPICAL APPLICATION CIRCUIT

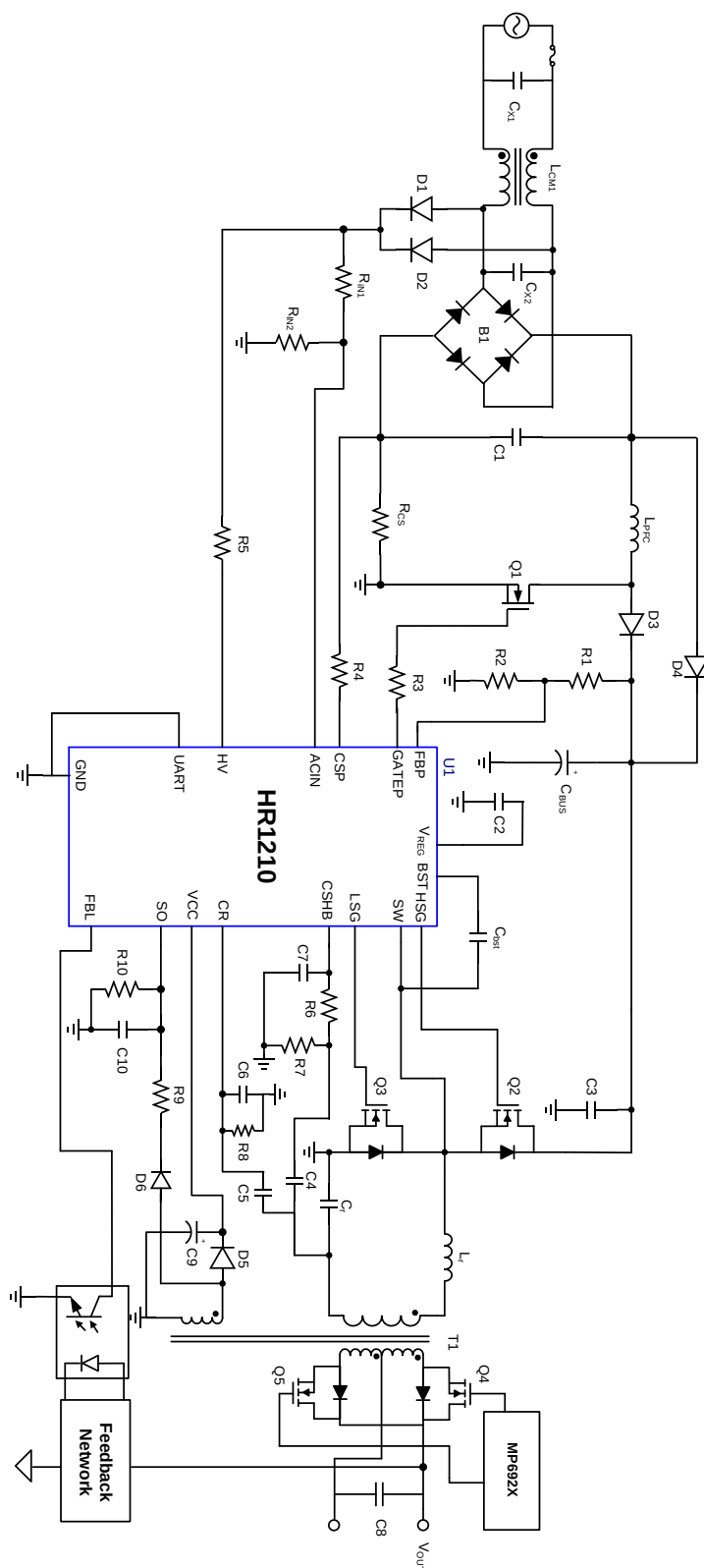


Figure 1: Typical Application Circuit

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
HR1210GY-xxxx**	SOIC-20	See Below	3
HR1210GY-0000	SOIC-20		

* For Tape & Reel, add suffix –Z (e.g. HR1210GY-XXXX–Z).

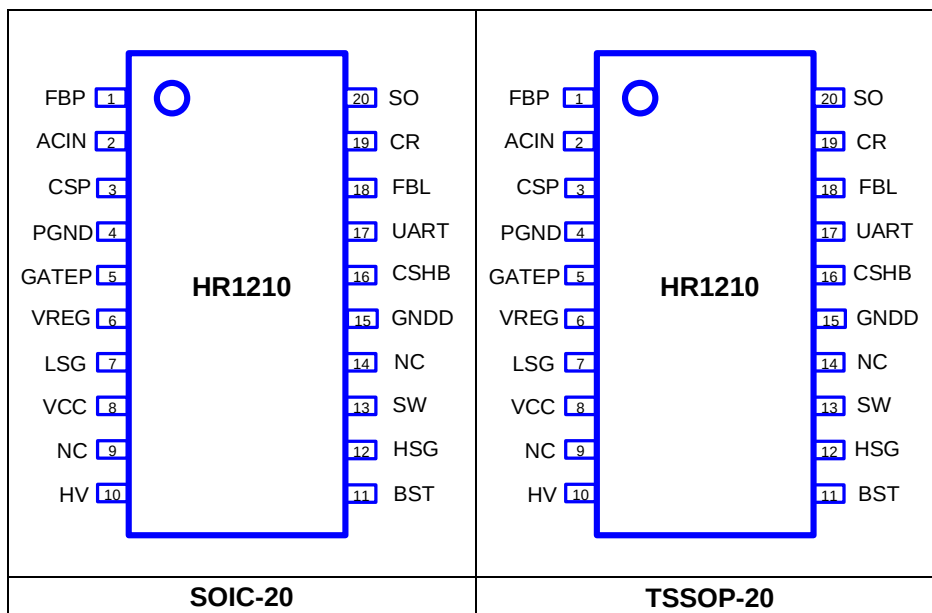
** “xxxx” is the configuration code identifier for the register setting stored in the MTP. The default number is “0000”. Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0000” code. HR1210GY-0000 is the default version.

TOP MARKING (HR1210GY)

MPSYYWW
HR1210
LLLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
HR1210: Part number
LLLLLLLLLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	FBP	Senses PFC output voltage to perform PFC switch on-time calculation, over-voltage protection (OVP) and overload protection (OLP). FBP calculates the digital current reference ($I_{REF(n)}$) which decide the PFC switching frequency. A 3.3M Ω pull-down resistor is connected internally. For noise immunity, connect a capacitor (around 4.7nF) to FBP.
2	ACIN	AC input voltage sense. This pin performs PFC switch-on time calculation, brown-in/out protection, and calculates digital current reference $I_{REF(n)}$ which decide the PFC switching frequency. It is recommended to connect a capacitor (around 2.2nF) for noise immunity.
3	CSP	PFC switching current sense. This pin defines the PFC switch on time, switching frequency, and cycle-by-cycle current-limiting protection. Connect a 500 Ω resistor in series between the current-sense resistor and CSP pin to prevent overstress during AC plug-in or surge conditions. CSP offers an internal ESD clamping capability, or an external clamping component can be used.
4	PGND	Ground reference of PFC and LLC low-side gate.
5	GATEP	PFC gate driver output.
6	VREG	Voltage regulator for PFC and LLC gate drivers and internal circuits.
7	LSG	LLC low-side gate driver output.
8	VCC	IC supply power. VCC can be charged by an internal current source through HV or by external power supply.
9	NC	No connection.
10	HV	High-voltage supply input. HV is the internal start-up source and X-capacitor discharger when the AC input voltage drops out.
11	BST	Bootstrap voltage. An internal bootstrap diode is connected from VCC to BST. Externally connect a capacitor to SW to drive the high-side MOSFET of the HB LLC.
12	HSG	LLC high-side gate driver output.
13	SW	High-side switch source. Current return for the high-side gate-drive current. Requires careful layout to avoid large spikes below ground.
14	NC	No connection.
15	GNDD	Ground reference for digital core of PFC.
16	CSHB	Half-bridge current sense. Uses a sense resistor or a capacitive divider to sense the primary current. Thid pin has multiple functions: 1. Over-current protection: If the current continues to build up, when $V_{CSHB} > V_{CS-OC}$, OCP is triggered and brings the IC into a configurable protection (auto-restart or latch). 2. Capacitive mode protection: V_{CSHB} is compared with the V_{CSNR} and V_{CSPR} threshold to define if the LLC current is in positive or negative polarity. The IC terminates the high-side gate driver (HSG) when the current goes into negative polarity ($V_{CSHB} < V_{CSPR}$), or it terminates the low-side gate driver (LSG) when the current goes into positive polarity ($V_{CSHB} > V_{CSNR}$).
17	UART	Universal asynchronous receiver-transmitter. UART provides a half-duplex communication IO interface. Connect this pin to GNDD when the IC is operating. Real-time communication is not recommended. UART should never be pulled high when V_{CC} is below V_{CCUV1} .
18	FBL	LLC output voltage feedback input. Pulled up by a voltage source with an internal resistor. Defines the LLC switching frequency according to the load condition. Activate LLC skip mode, burst mode, and over-power protection (OPP) according to the voltage level on this pin.
19	CR	LLC capacitor voltage sense input. Senses the divided resonant capacitor voltage to determine the LLC switching frequency.
20	SO	If V_{SO} exceeds V_{SO-OVP} , over-voltage protection (OVP) is triggered and the IC is forced into a configurable protection (auto-restart or latch). If over-temperature protection (OTP) is triggered, an external NTC can be connected on this pin (see Figure 39). The external resistor between SO and GNDD should be no less than 10k Ω .

ABSOLUTE MAXIMUM RATINGS ⁽²⁾

HV to PGND	-0.3V to +700V
BST to PGND	-0.3V to +618V
SW to PGND.....	-3V ⁽⁵⁾ to +618V
HSG to PGND.....	618V
LSG to PGND	-0.3V to +14V
SW to PGND maximum slew rate.....	50V/ns
VCC to PGND	-0.3V to +38V
VREG to PGND	-0.3V to +14V
GATEP to PGND	-0.3V to +14V
CR, CSHB to GNDD	-3.3V ⁽⁵⁾ to +3.6V
CSP to GNDD.....	-5V to +3.6V
PGND to GNDD	-0.3V to +0.3V
All other pins to GNDD.....	-0.3V to +3.6V
VREG supply current	40mA

CSP input current limit at negative voltage
overstress (clamped by internal ESD device) ⁽⁵⁾

2ms single pulse	-0.15A
100µs single pulse	-0.17A
20µs single pulse	-0.20A

Continuous power dissipation ($T_A = 25^\circ\text{C}$) ⁽³⁾

SOIC-20	1.92W
TSSOP-20	1.38W

Storage temperature	-55°C to +150°C
Junction temperature	-40°C to +150°C
Lead temperature	260°C

ESD Ratings ⁽²⁾

Human-body model (HBM).....	2000V
Charged-device model (CDM).....	1500V

Recommended Operating Conditions ⁽¹⁾

Supply voltage (V_{CC})	12V to 35V
Operating junction temp (T_J).....	-40°C to +125°C

Thermal Resistance ⁽⁴⁾ θ_{JA} θ_{JC}

SOIC-20.....	65	30... °C/W
TSSOP-20	90	40... °C/W

Notes:

- 1) The device is not guaranteed to function outside of its operating conditions.
- 2) Exceeding these ratings may damage the device.
- 3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) Measured on JESD51-7, 4-layer PCB.
- 5) Guaranteed by characterization.

ELECTRICAL CHARACTERISTICS

$V_{CC} = 25V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, min and max values are guaranteed by characterization, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
High-Voltage Start-Up Current Source (HV Pin)						
Breakdown voltage	V_{HVBR}	$T_J = 25^{\circ}C$	700			V
Normal charge current	I_{HVNOR}	$V_{CCSCP} < V_{CC} < 15V$, $T_J = 25^{\circ}C$	5.9	7	9	mA
Extra charge current from VCC pin	I_{VCCON_OUT}	$V_{CC} = V_{CCON(HV)} - 0.1V$, $T_J = 25^{\circ}C$	2			mA
Supply current when fault occurs	$I_{HVLIMIT}$	$V_{CC} < V_{CCSCP}$	1.5	2.2	3	mA
Leakage current during shutdown	I_{HVOFF}	$V_{HV} = 400V$, $V_{CC} = 24V$		4.5	10	μA
IC Power Supply (VCC Pin)						
IC turn-on threshold	$V_{CCON(HV)}$		20	21.5	23	V
UV protection threshold 1	V_{CCUVP1}		10	10.8	11.5	V
UV protection threshold 2	V_{CCUVP2}		13.5	14.4	15.2	V
IC release threshold	V_{CCRST}		8	8.8	9.3	V
X-capacitor discharger regulation voltage ⁽⁶⁾	V_{CCXCD}			17		V
Short-circuit protection	V_{CCSCP}		0.76	0.94	1.4	V
Normal operating current	$I_{CC(nor)}$	$C_{GATEP} = 1nF$, $f_{PFC} = 100kHz$, $C_{HSG} = 1nF$, $C_{LSG} = 1nF$, $f_{LLC} = 200kHz$		15		mA
		No switch, $T_J = 25^{\circ}C$		8	10	
Start-up current	$I_{CC-start1}$	$V_{CC} = 20V$		2.1	3.5	mA
Burst mode current	$I_{CC-Burst}$	When burst off, $T_J = 25^{\circ}C$		2.2	2.7	mA
X-capacitor Discharger (HV Pin)						
Discharge current	I_{HVXCD}	$T_J = 25^{\circ}C$	5.9	7	9	mA
Discharge clock time	t_{X-d}		0.8	1.6	2.6	ms
PFC Gate Driver (GATEP Pin)						
Minimum high-voltage gate	V_{OH}	$C_{GATEP} = 1nF$, sourcing 20mA, $V_{REG} = 11.5V$	11.3			V
Maximum low-voltage gate	V_{OL}	$C_{GATEP} = 1nF$, sinking 20mA, $V_{REG} = 11.5V$			0.1	V
Gate on resistor	$R_{ON(H)}$	Sourcing 20mA		4.5	7.5	Ω
	$R_{ON(L)}$	Sinking 20mA		2.5	5	Ω
Voltage fall time	t_F	$C_{GATE} = 1nF$		20	40	ns
Voltage rise time	t_R	$C_{GATE} = 1nF$		20	40	ns
Sourcing capacity	I_{GATE_SR}	$C_{GATE} = 1nF$		650		mA
Sinking capacity	I_{GATE_SK}	$C_{GATE} = 1nF$		800		mA

ELECTRICAL CHARACTERISTICS (continued)

$V_{CC} = 25V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, min and max values are guaranteed by characterization, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Regulated Power Supply (VREG Pin)						
Regulated output voltage	V _{REG}	I _{REG} = 0mA	11	12	13	V
		I _{REG} = 20mA	10.8	11.9	12.8	V
Turn-on threshold	V _{REGON}		9	10	10.9	V
UVP	V _{REGUVP}		6.5	7.3	8.1	V
System Clock						
Clock frequency	f _{OSC1_NOR}	At normal, T _J = 25°C	180	200	223	MHz
	f _{OSC2_NOR}	At normal, T _J = 25°C	16.6	17.5	18.7	
	f _{OSC_NOPWM} ⁽⁵⁾	At burst off		1		
AC Input Sensing (ACIN Pin)						
Voltage range			0		1.6	V
PFC Feedback (FBP Pin)						
Voltage range			0		1.6	V
Internal resistance	R _{FBP_internal}			3.3		MΩ
Current Sense (CSP Pin)						
Voltage range			-1.4		0	V
Internal bias voltage	V _{BIAS_CSP}	V _{CSP} = 0V	0.19	0.2	0.21	V
ADC for CSP						
ADC voltage reference			1.585	1.6	1.61	V
		T _J = 25°C	1.595	1.6	1.605	V
ADC resolution ⁽⁷⁾				12		bits
Acquisition time ⁽⁶⁾				300		ns
Offset error ⁽⁷⁾				±0.5		LSB
Gain error ⁽⁷⁾				±1.5		LSB
ADC for ACIN, FBP, FBL						
ADC voltage reference			1.585	1.6	1.61	V
		T _J = 25°C	1.595	1.6	1.605	V
ADC resolution ⁽⁷⁾				10		bits
Acquisition time ⁽⁶⁾				300		ns
Offset error ⁽⁷⁾				±0.5		LSB
Gain error ⁽⁷⁾				±1.5		LSB

ELECTRICAL CHARACTERISTICS (continued)

$V_{CC} = 25V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, min and max values are guaranteed by characterization, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
DAC for OVP OCL, BI/BO of PFC, OPP, ADOFF of LLC						
DAC voltage reference			1.585	1.6	1.61	V
		$T_J = 25^{\circ}C$	1.595	1.6	1.605	V
PFC BI/BO DAC output				0.4		V
Resolution ⁽⁷⁾				8		bits
Offset error ⁽⁷⁾				± 0.2		LSB
Gain error ⁽⁷⁾				± 1.5		LSB
DAC for Set Signal of PFC						
DAC voltage reference			1.585	1.6	1.61	V
		$T_J = 25^{\circ}C$	1.595	1.6	1.605	V
Resolution ⁽⁷⁾				10		bits
Offset error ⁽⁷⁾				± 0.5		LSB
Gain error ⁽⁷⁾				± 1.5		LSB
DAC for Set Signal of LLC						
DAC voltage reference			1.77	1.8	1.825	V
		$T_J = 25^{\circ}C$	1.788	1.8	1.812	V
Resolution ⁽⁷⁾				10		bits
Offset error ⁽⁷⁾				± 0.5		LSB
Gain error ⁽⁷⁾				± 1.5		LSB
High-Side Floating Gate-Driver Supply (BST and SW Pins)						
BST pin leakage current	I_{LKBST}	$V_{BST} = 600V$			10	μA
SW pin leakage current	I_{LKSW}	$V_{SW} = 582V$			10	μA
Half-Bridge Current Sense (CSHB Pin)						
OCP threshold	V_{CS-OC}		1.475	1.5	1.52	V
Current polarity comparator reference when HSG is on	V_{CSPR}			80		mV
Current polarity comparator reference when LSG is on	V_{CSNR}			-80		mV
Output Voltage Sense (SO Pin)						
Over-voltage protection on SO	V_{SO-OVP}		1.475	1.5	1.52	V
ADTA (SW Pin)						
Minimum detectable voltage slew rate ⁽⁶⁾	dV_{MIN}/dt			85		V/ μs
Turn-on delay ⁽⁶⁾	t_D	Slope finish to turn-on delay		150		ns

ELECTRICAL CHARACTERISTICS (continued)

$V_{CC} = 25V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, min and max values are guaranteed by characterization, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback Section (FBL Pin)						
Internal pull-up resistor on FBL	R_{FBL_LOW}	$T_J = 25^{\circ}C$	7	8	9.6	k Ω
Internal pull-up resistor on FBL in power-saving mode	R_{FBL_HIGH}		38	47	56	k Ω
Internal voltage reference	V_{FBL_SOURCE}	$T_J = 25^{\circ}C$	2.35	2.41	2.5	V
V_{COMP} offset voltage from FBL voltage	V_{FBL_OFFSET}		0.995	1	1.005	V
Current Sense Input Section (CR Pin)						
Slope compensation amplitude per LSB ⁽⁶⁾	dV_{CR_Slope}/dt	$T_J = 25^{\circ}C$	5.0	6.64	8.2	mV/ μ s
Zero detection threshold	V_{CR_ZERO}		15	20	25	mV
On-time comparator delay to HSG driver shutdown ⁽⁶⁾	t_{d_CR}			150		ns
Current sense input leakage current	$I_{CR_leakage}$	$V_{CR} = 2V$			± 1	μ A
Leading-edge blanking ⁽⁶⁾	t_{LEB}			300		ns
Low-Side Gate Driver (LSG Pin)						
Peak source current ⁽⁶⁾	$I_{SOURCEPK}$			0.75		A
Peak sink current ⁽⁶⁾	I_{SINKPK}			0.87		A
Sourcing resistor	R_{SOURCE}			5	8	Ω
Sinking resistor	R_{SINK}			2.5	5	Ω
Fall time	t_F			20	40	ns
Rise time	t_R			20	40	ns
High-Side Gate Driver (HSG Pin, Referenced to SW Pin)						
Peak source current ⁽⁶⁾	$I_{SOURCEPK}$			0.74		A
Peak sink current ⁽⁶⁾	I_{SINKPK}			0.87		A
Sourcing resistor	R_{SOURCE}			5	8	Ω
Sinking resistor	R_{SINK}			2.5	5	Ω
Fall time	t_F			20	40	ns
Rise time	t_R			20	40	ns
Over-Temperature Protection						
Over-temperature protection threshold ⁽⁶⁾				145		$^{\circ}C$
Over-temperature protection recovery threshold ⁽⁶⁾				120		$^{\circ}C$

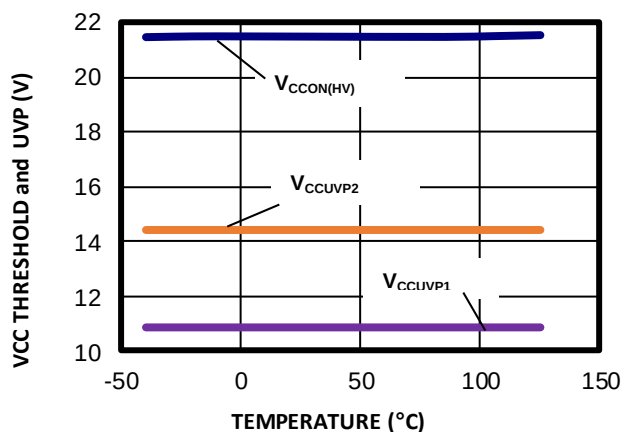
Notes:

6) Guaranteed by design.

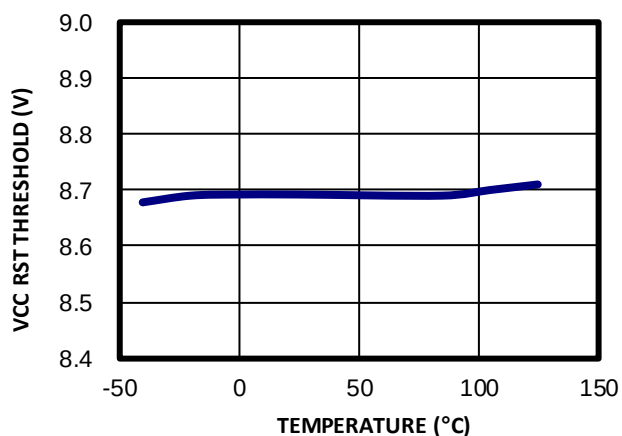
7) Guaranteed by characterization.

TYPICAL CHARACTERISTICS

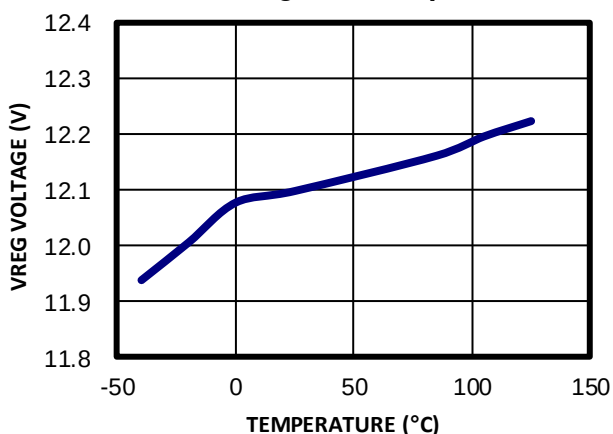
VCC On and Under-Voltage Protection (UVP) vs. Temperature



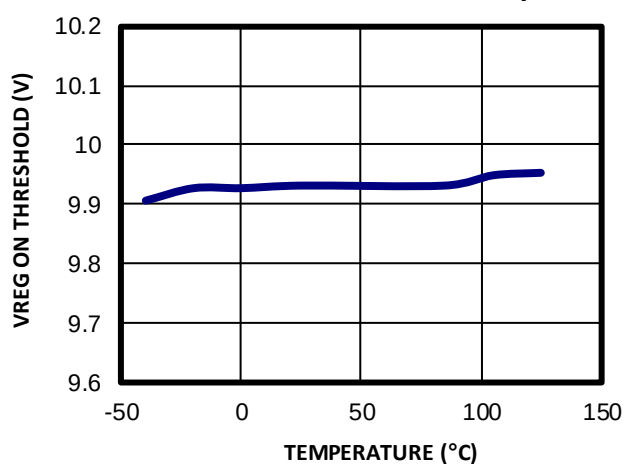
VCC RST Threshold vs. Temperature



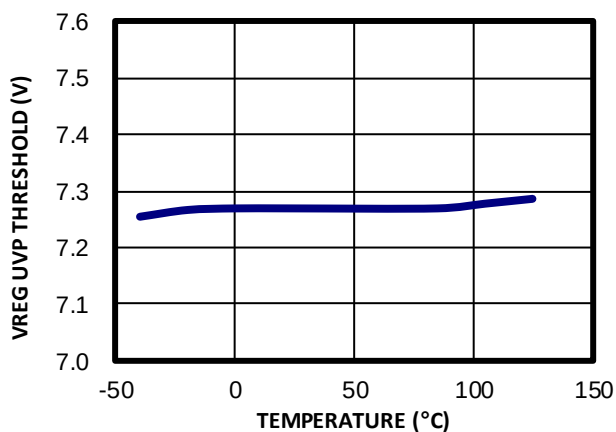
VREG Voltage vs. Temperature



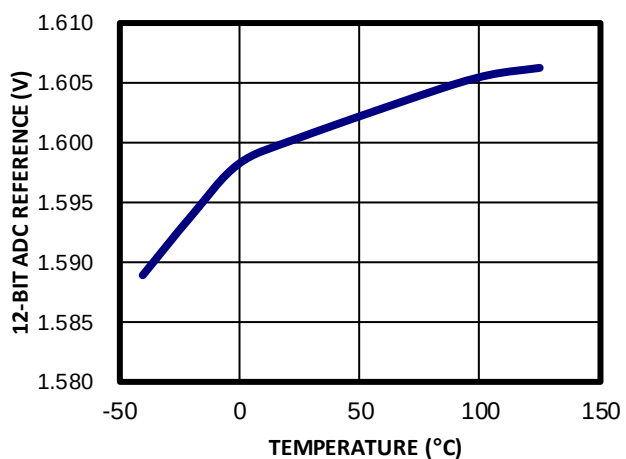
VREG On Threshold vs. Temperature



VREG Under-Voltage Protection (UVP) Threshold vs. Temperature

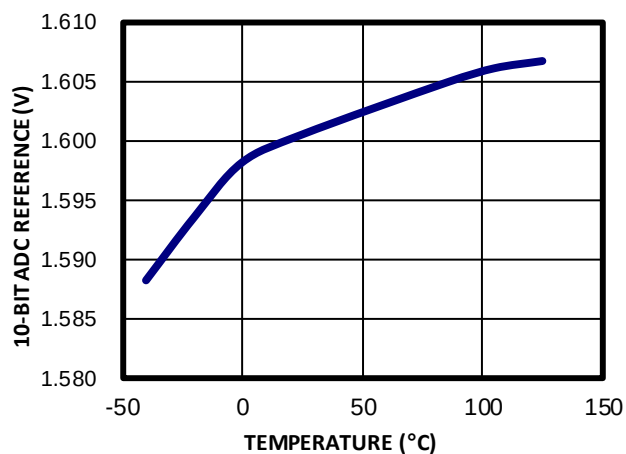


12-Bit ADC Reference vs. Temperature

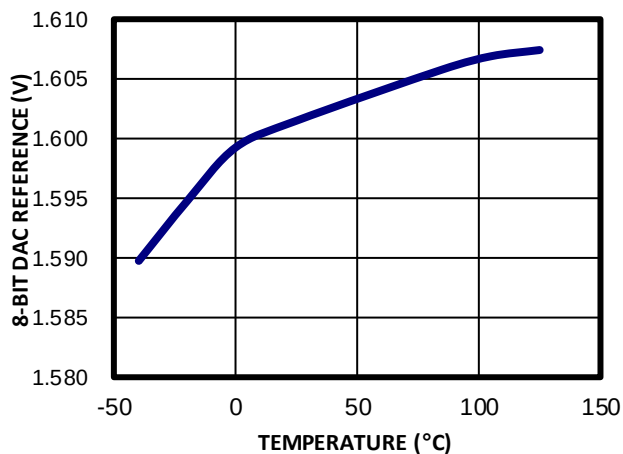


TYPICAL CHARACTERISTICS *(continued)*

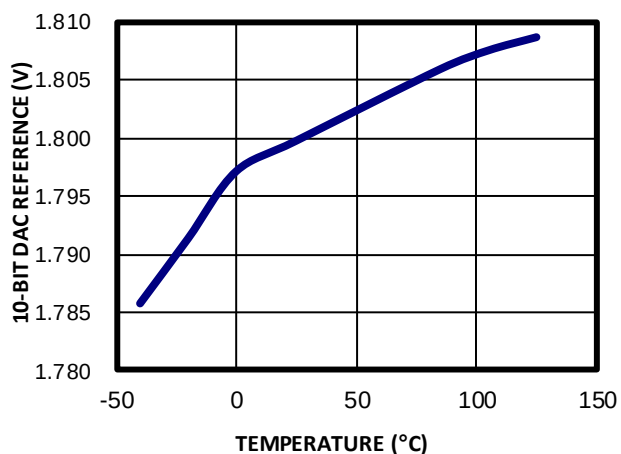
10-Bit ADC Reference vs. Temperature



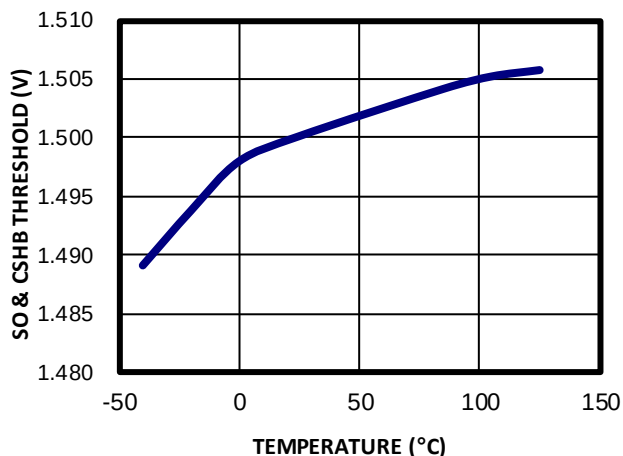
8-Bit DAC Reference vs. Temperature



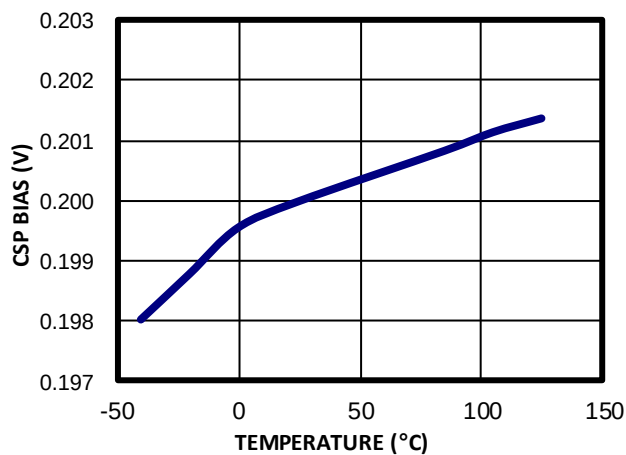
10-Bit DAC Reference vs. Temperature



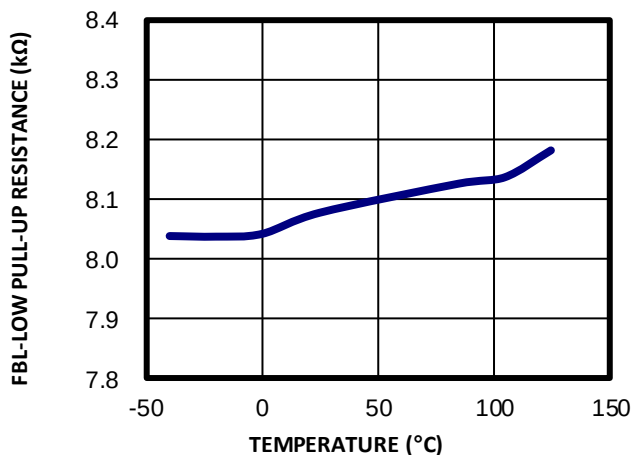
SO and CSHB Threshold vs. Temperature



CSP Bias vs. Temperature

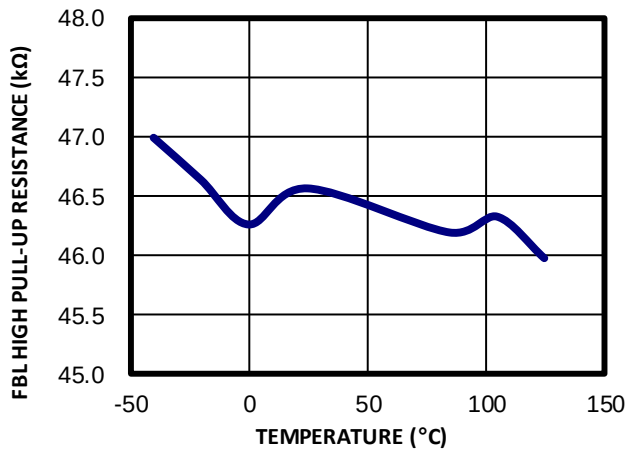


FBL Low Pull-Up Resistance vs. Temperature

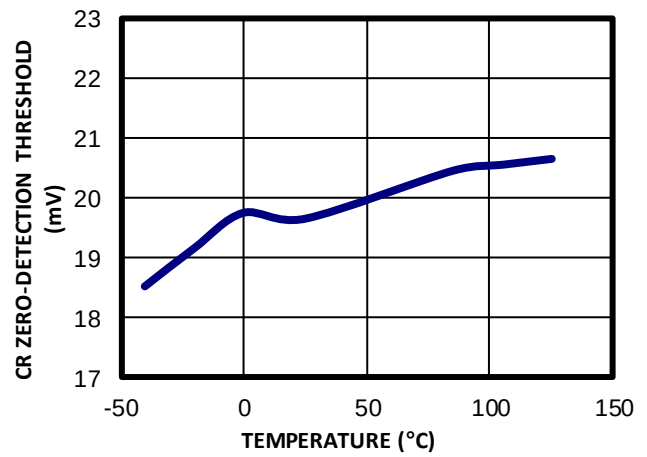


TYPICAL CHARACTERISTICS *(continued)*

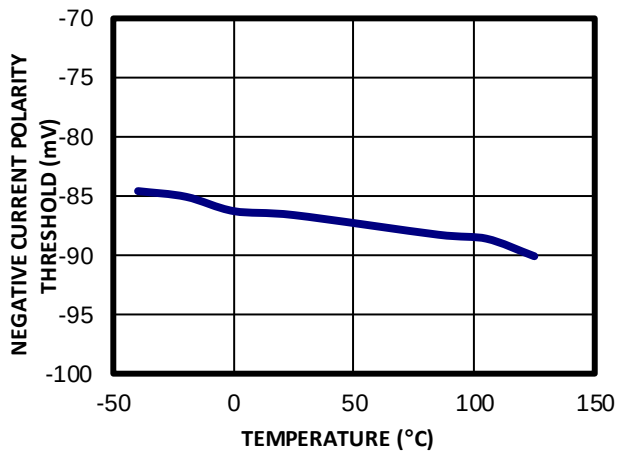
FBL High Pull-Up Resistance vs. Temperature



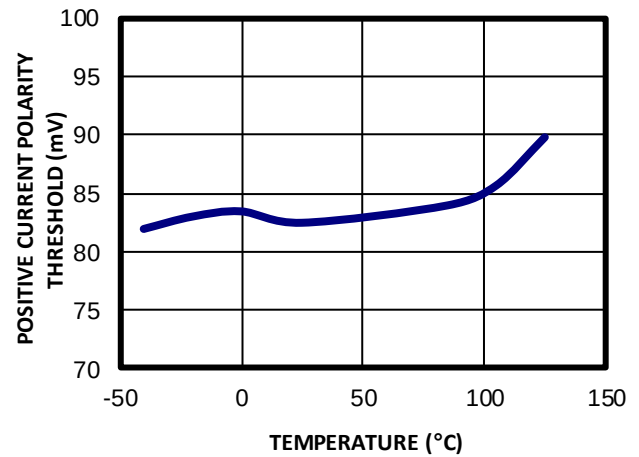
CR Zero-Detection Threshold vs. Temperature



Negative Current Polarity Threshold vs. Temperature



Positive Current Polarity Threshold vs. Temperature

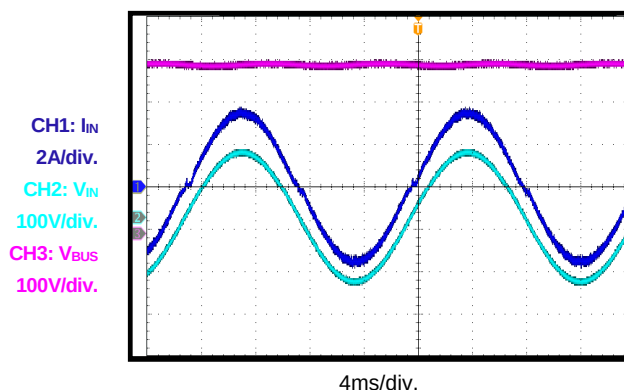


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 85V AC to 265V AC, V_{OUT} = 12V, I_{OUT} = 20A, T_A = 25°C, unless otherwise noted.

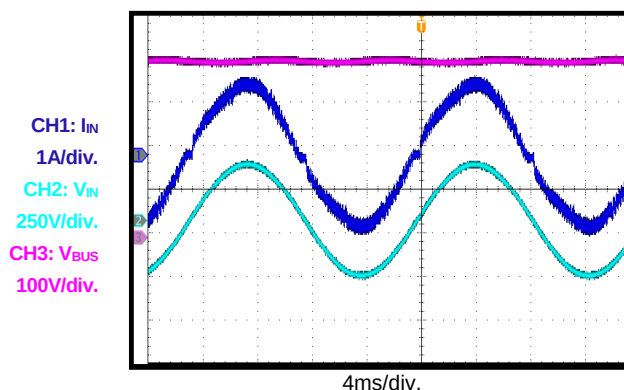
Steady State at Input

V_{IN} = 110V AC at P_{OUT} = 240W



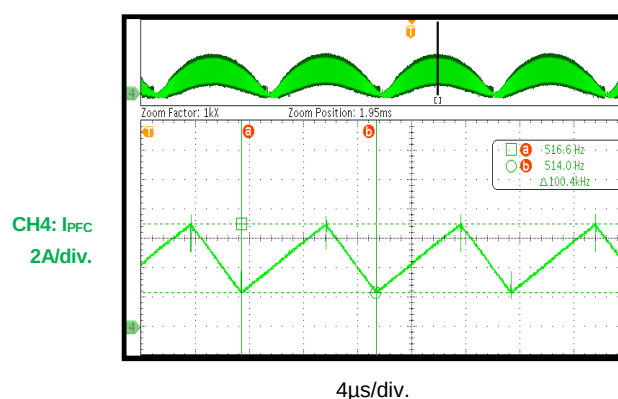
Steady State at Input

V_{IN} = 230V AC at P_{OUT} = 240W



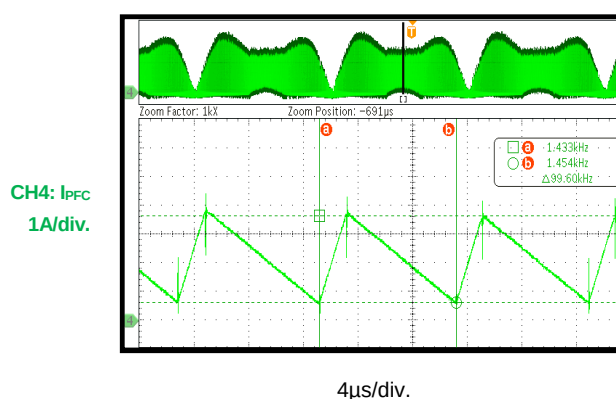
Steady State at PFC choke

V_{IN} = 110V AC at P_{OUT} = 240W



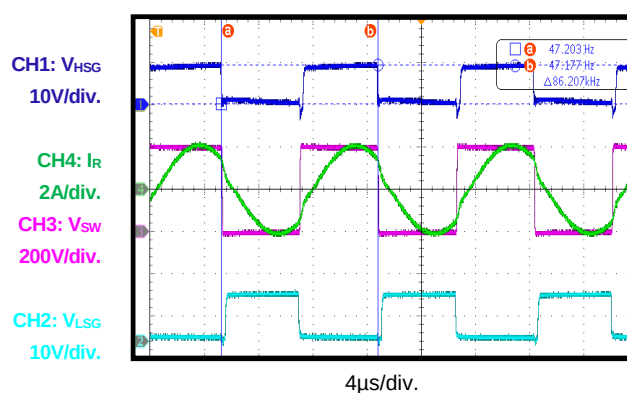
Steady State at PFC choke

V_{IN} = 230V AC at P_{OUT} = 240W



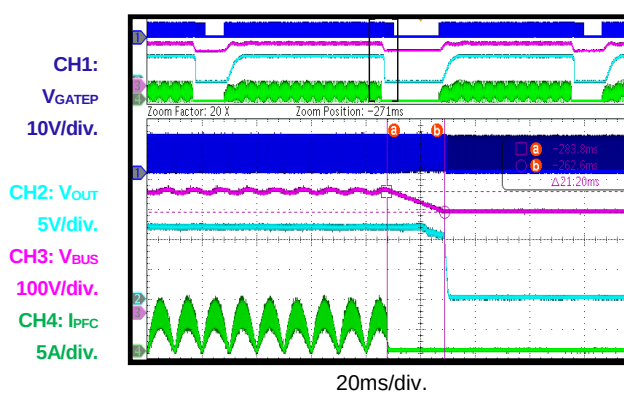
Steady State at LLC

P_{OUT} = 240W



Input Start-Up/Shutdown at PFC

V_{IN} = 110V AC, P_{OUT} = 240W

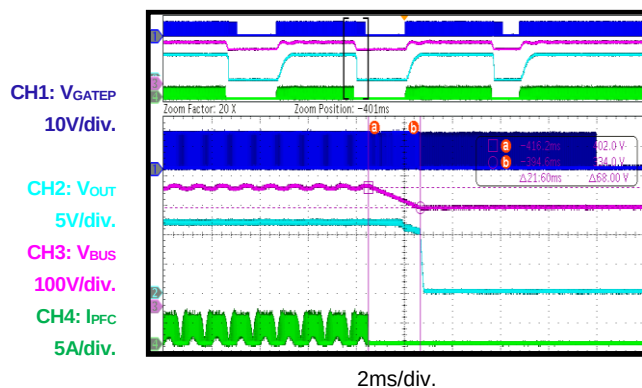


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 85V AC to 265V AC, V_{OUT} = 12V, I_{OUT} = 20A, T_A = 25°C, unless otherwise noted.

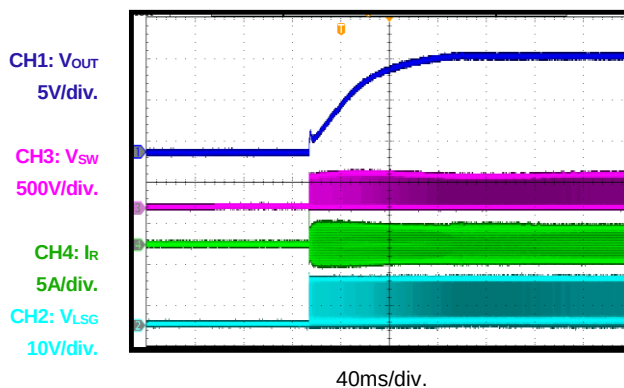
Input Start-Up/Shutdown at PFC

V_{IN} = 230V AC, P_{OUT} = 240W



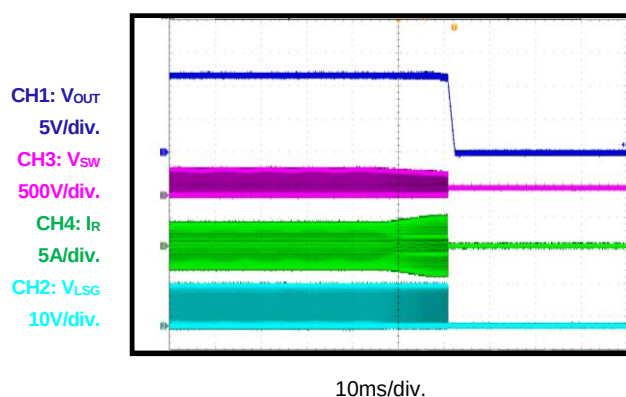
Input Start-Up at LLC

P_{OUT} = 240W



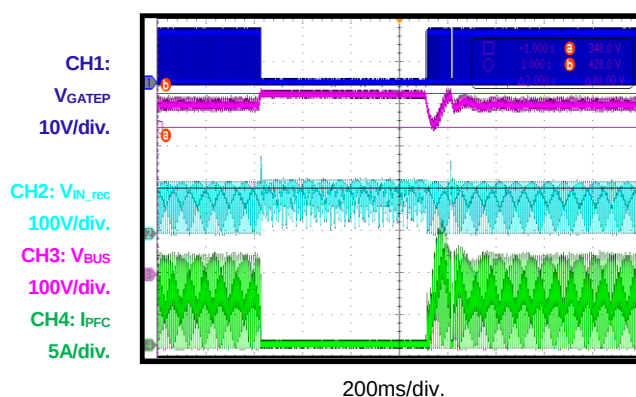
Input Shutdown at LLC

P_{OUT} = 240W



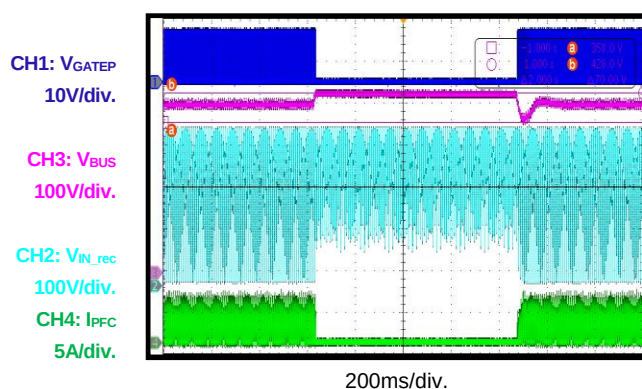
Load Dynamic at PFC

V_{IN} = 85V AC, P_{OUT} = 0W to 240W, 1A/μs



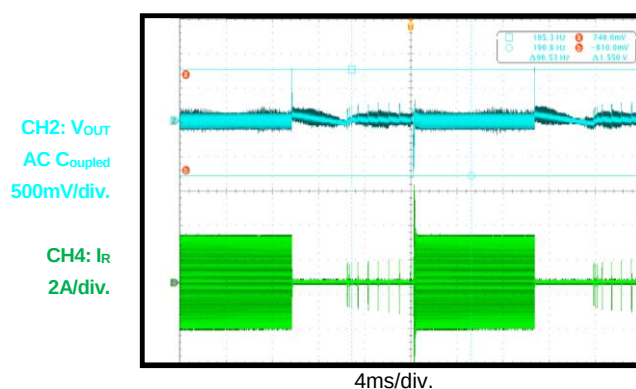
Load Dynamic at PFC

V_{IN} = 265V AC, P_{OUT} = 0W to 240W, 1A/μs



Load Dynamic at LLC

P_{OUT} = 0W to 240W, 6A/μs



FUNCTIONAL BLOCK DIAGRAM

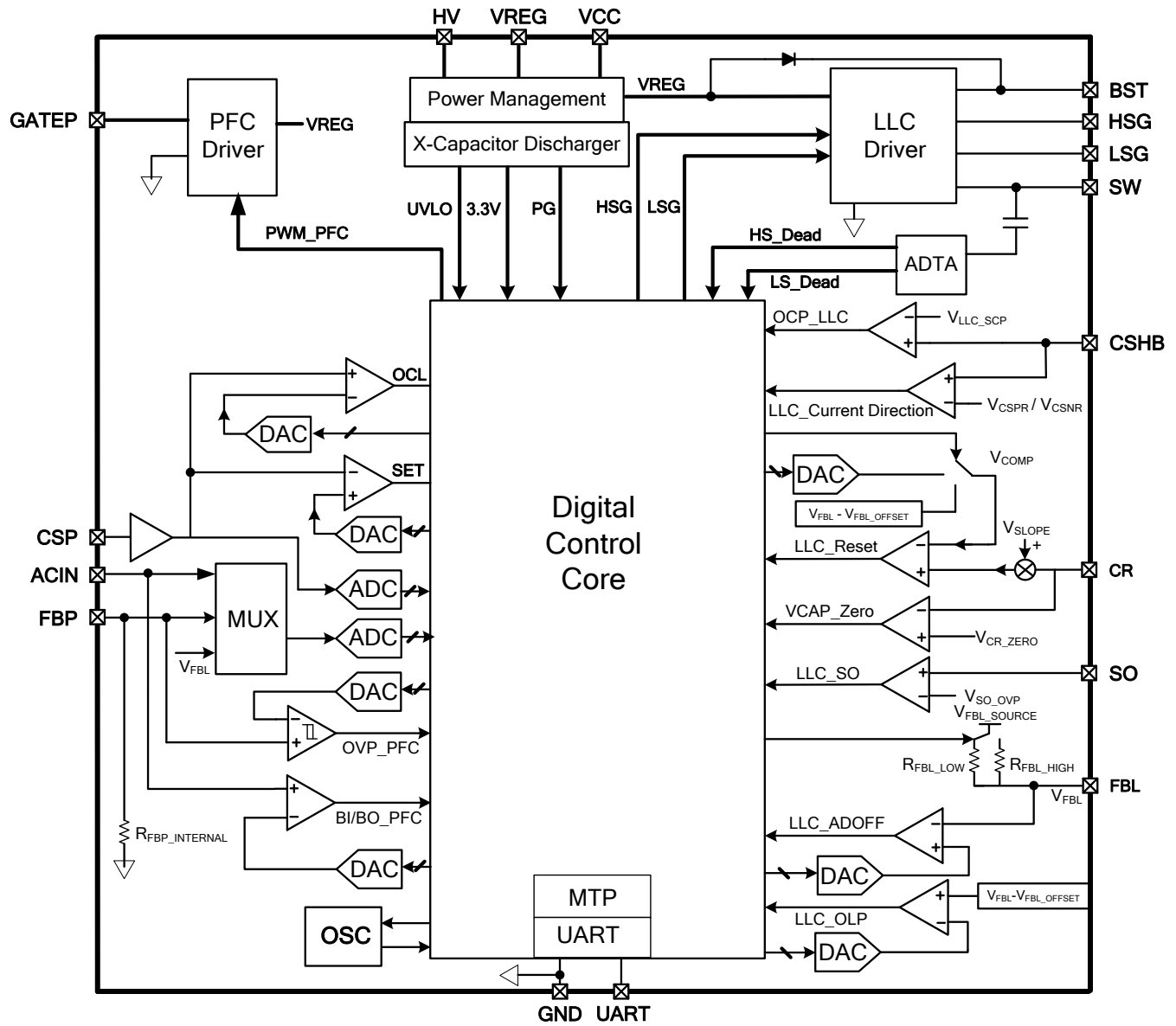


Figure 2: Functional Block Diagram

IC Supply Input (VCC)

VCC provides a power supply for all of the internal circuits, including VREG and the internal V3.3 supply.

VCC can be powered either by the auxiliary winding of the HB transformer or an external power supply.

If V_{CC} drops below the under-voltage protection (UVP) threshold, the following actions occur:

1. The IC stops operating, and the PFC driver stops switching immediately. The HB LLC continues to operate until the low-side MOSFET (LS-FET) turns on.
2. The VREG LDO is disabled.

There are two VCC UVP thresholds. If the LLC does not start switching, the UVP level is V_{CCUVP2} . If the LLC starts switching, the UVP level is V_{CCUVP1} .

If the IC enters latch mode, the latch status remains until V_{CC} falls below V_{CCRST} .

Regulated Output (VREG)

An internal LDO stabilizes VREG to:

- Supply the internal PFC driver
- Supply the internal low-side driver of the HB LLC
- Charge the bootstrap capacitor, which provides a power supply for the internal high-side driver of the HB LLC
- Use as a voltage reference for external circuits.

When V_{CC} rises to $V_{CCON(HV)}$, the internal LDO is enabled to charge the VREG capacitor. When VREG is built up and there is no fault condition, the IC starts operating. The LDO is enabled only when V_{CC} exceeds $V_{CCON(HV)}$. This ensures that any optional external circuitry connected to VREG does not dissipate any extra current before the IC starts up.

The IC starts working only when the regulated output voltage (V_{REG}) exceeds V_{REGON} . If V_{REG} drops below V_{REGUVP} , the IC stops, and the PFC controller stops switching immediately. The HB LLC controller continues operating until the low-side gate becomes active.

V3.3 for Digital Logic

V3.3 is an internal, stabilized 3.3V power supply for the digital circuit. It is derived from VCC by an internal LDO. When V_{CC} exceeds V_{CCRST} with a hysteresis, the V3.3 LDO is enabled. It is only disabled when V_{CC} drops below V_{CCRST} .

V3.3 serves as the input of an internal 1.8V LDO, which supplies power to the digital core.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is an internal enable signal for both the PFC and LLC digital controller. When V_{CC} exceeds V_{CCUVP1} and V_{REG} exceeds V_{REGON} , UVLO goes high. The UVLO signal is pulled low when V_{REG} falls below V_{REGUVP} .

Internal Power Good (PG) Indicator

The internal PG signal indicates to the digital core that the power supply (VCC) voltage is regulated. When UVLO goes high, the PG signal is pulled high after a 200 μ s delay ($t_{PG-DELAY}$).

System Functions

X-Capacitor Discharger

X-capacitors are critical components placed at the input terminals of power supplies to filter out differential EMI noise. If the AC line is removed, the energy stored in the X-capacitor could be dangerous. Safety standards require the voltage be discharged to a safe level within a certain time frame.

Resistors can be placed in parallel with the X-capacitor across the AC line to provide a discharge path. However, extra resistors require continuous power consumption while the AC input is connected, which is a significant contributor to the power consumption during no-load or standby conditions.

The HV current source in the HR1210 acts as an X-capacitor discharger when the AC input is removed, so the traditional discharge resistors are not required. Figure 6 shows the operating waveforms of the X-capacitor discharger when the AC input is removed.

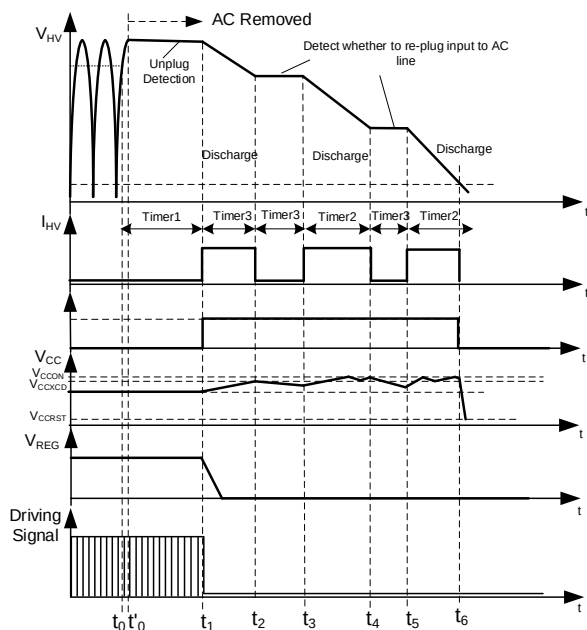


Figure 6: Operating Waveform of X-Capacitor Discharger when AC is Removed

In normal operation with the presence of the AC line, the HR1210 HV current source turns off. The HV leakage current is very small, so the power consumption is reduced significantly.

When the AC line is disconnected after the Timer 1 detection time ($60 \times t_{X-d}$), the IC controls the internal current source (I_{HV-NOR}) to discharge energy from the X-capacitor to VCC within the Timer 3 ($30 \times t_{X-d}$) period. The IC stops for an additional Timer 3 period to detect the AC. If no AC is reapplied during this time period, the IC continues discharging during the next Timer 2 ($90 \times t_{X-d}$) period until V_{HV} drops below 35V. Once V_{HV} drops below 35V, the internal current source discharges VCC until it drops below V_{CCRST} , which releases the latch of the IC when it is in latch-protection mode.

If the AC recovers in HV again during the Timer 3 period, a new start-up procedure begins (see Figure 7).

When the X-capacitor discharge function is activated, VCC is regulated between $V_{CCON(HV)}$ and V_{CCXCD} to avoid over-stressing VCC.

The X-capacitor discharge function allows users to choose any X-capacitor value that optimizes differential mode EMI filtering. This eliminates negative side effects from the required bleed resistors on the standby power budget and system no-load.

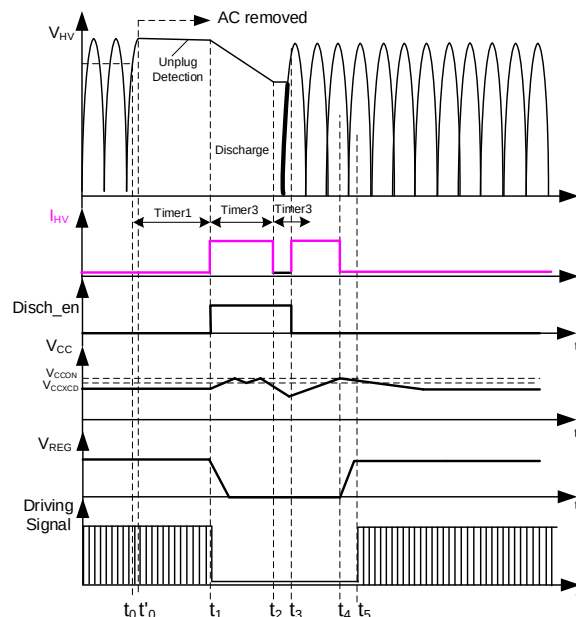


Figure 7: Operating Waveform of X-Capacitor Discharger during AC Recovery

Over-Temperature Protection (OTP)

If the internal thermal sensor senses that the IC temperature exceeds the over-temperature protection (OTP) threshold, the IC stops switching immediately. In OTP, the high-voltage current source is disabled so that the VCC cannot charge, and both the internal LDO for VREG and V3.3 are disabled. If the IC temperature drops below the OTP recovery threshold and VCC drops below V_{CCRST} , the IC starts up again when VCC is charged to above $V_{CCON(HV)}$.

IC Enable/Disable Control

The IC (either PFC operation or LLC operation) can be enabled and disabled by programming the MTP with the GUI.

Digital PFC Controller

The HR1210's state-of-the-art CCM/DCM control scheme reduces the RMS current drawn from the AC mains by ensuring good input current shaping in both CCM and DCM. The control scheme reduces the switching frequency when the load is decreased, therefore achieving higher efficiency and higher power factors at light loads.

Timing Sequence of Digital PFC

Figure 8 shows the timing sequence of the digital PFC block.

Timing Sequence of the Internal Power Supply

Once V_{CC} rises above V_{CCRST} with a hysteresis, the V3.3 LDO is enabled and an internal LDO downstream produces a stable 1.8V power supply for the internal digital core and system clocks. The RST signal is set high when both 3.3V and 1.8V are stable. When UVLO is validated, the IC enables OSC, ADC, DAC, and the relative comparators. The enable signal is set high after a 20 μ s delay, which indicates that the digital core is ready to begin operation.

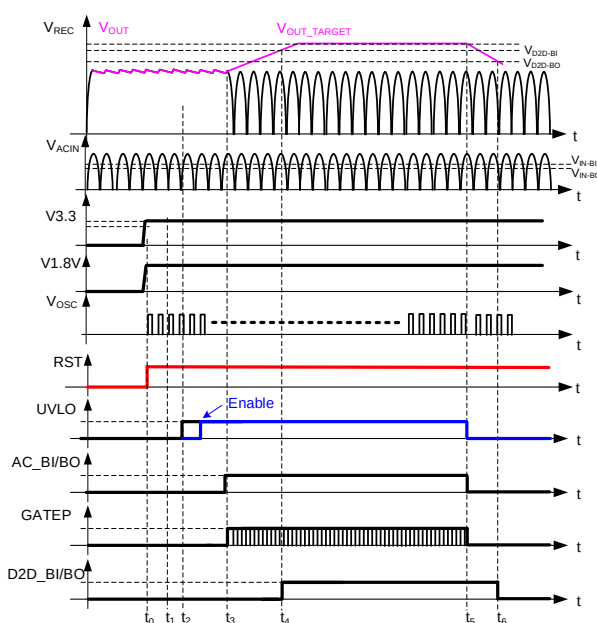


Figure 8: Power Supply Sequence of the Digital PFC

Timing of Digital Core

When the RST signal and enable signal (UVLO) are high, the digital system monitors the PG signal (from analog) for a 150 μ s detection time window, which determines whether or not the PFC and LLC start switching with a soft start. If no PG signal is detected, a soft start of the switching is applied. Otherwise, no soft start is applied on PFC and LLC switching.

After this PG detection time window, the digital system starts operating. First, ADC starts sampling V_{ACIN} and V_{FBP} . If the AC brown-in condition is met and there is no open-loop fault on the FBP pin, the AC_BI/BO signal is set to high and the PFC starts switching until the output

reaches the target value. The LLC starts switching when the PFC output voltage ramps up to the LLC brown-in threshold.

Oscillator

The system clock frequency for the PFC is f_{OSC1_NOR} , and the system clock frequency for LLC is f_{OSC2_NOR} . When the system is in ultra-low power mode (both the PFC and LLC are burst off), the PFC and LLC clock frequencies decrease to f_{OSC_NOPWM} , and the PWM clock frequency decreases to f_{OSC2_NOR} to reduce the IC power consumption.

ADC Sampling

The HR1210 has two independent ADCs that sample the AC input voltage, PFC output voltage, LLC feedback voltage, and PFC switching peak current. The digital PFC controller gets the information of the PFC inductor peak current on CSP via a 12-bit ADC.

A 3-channel, high-speed analog switch is used to switch between the AC input, V_{OUT} (PFC), and FB (LLC) signals for another 10-bit ADC sampling window.

Figure 9 shows the ADC module block diagram.

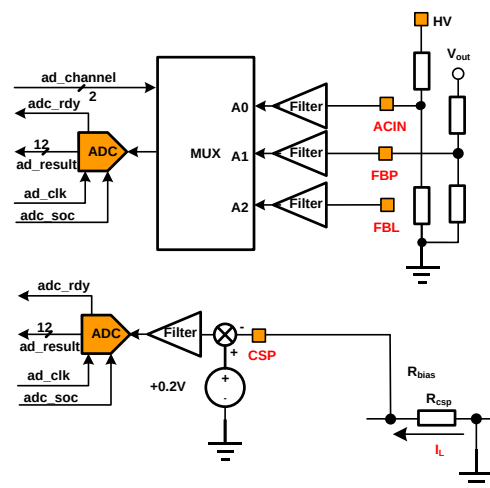


Figure 9: ADC Block Diagram

The ADC samples the ACIN, FBL, and FBP pins with a fixed frequency that can be adjusted by setting the idle time using the GUI. The LLC feedback voltage (V_{FBL}) is sampled every sampling period. The AC input voltage (V_{ACIN}) is sampled 3 times across every 4 sampling periods. The PFC output voltage (FBP) is sampled 1 time across every 4 sampling periods. Figure 10 shows the sampling sequence of the 10-bit ADC.



Figure 10: ADC Sampling Sequence

Input Voltage Sensing

The input voltage is rectified and attenuated by a resistor divider with a fixed ratio (0.0032) before being provided to the ACIN input. Then, the ADC samples the voltage on ACIN to get the instantaneous value, the peak value, and the frequency of the input voltage. The data is used for on-time calculations, AC brown-in/out protection, and input capacitor current compensation.

Figure 11 shows the input voltage level that is defined for different functions. All parameters can be programmed using the GUI.

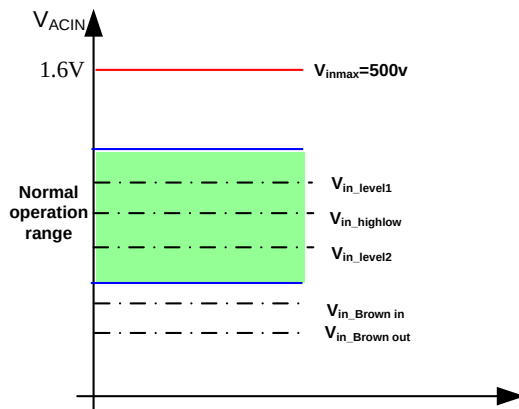


Figure 11: Input Voltage Levels

Input Brown-In/Brown-Out

When the peak voltage on ACIN (V_{ACIN}) exceeds the brown-in threshold (V_{IN-BI}) and lasts for the brown-in time set by BI_Timer, the PFC starts switching. If V_{ACIN} is below the brown-out threshold (V_{IN-BO}) for the brown-out time set by BO_Timer, then the PFC stops switching. Figure 12 shows the operating waveforms for brown-in/out control.

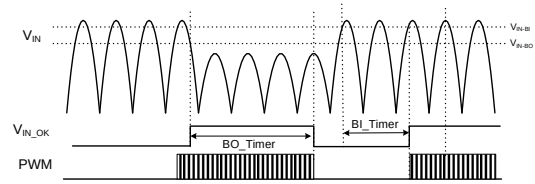


Figure 12: AC Brown-In and Brown-Out Control

High-Line/Low-Line

The system defines the input as the low-line condition when the input voltage is below $V_{IN_HIGH/LOW}$. The high-line input condition is determined when the input voltage exceeds $V_{IN_HIGH/LOW}$ with a hysteresis.

Both the soft-start time and resonant time for the PFC valley turn-on are implemented independently, according to the high-line or low-line input condition. To optimize PFC stage efficiency, the PFC output voltage and OVP can be regulated at different levels according to the high-line or low-line input condition.

There are another two configurable thresholds for the input voltage: V_{IN_LEVEL1} and V_{IN_LEVEL2} . With $V_{IN_HIGH/LOW}$, these thresholds divide the input voltage into four ranges. The input capacitor current compensation values can be set at different input voltage ranges to improve the power factor.

The three thresholds are 8-bit data in the MTP and can be configured using the GUI.

Output Voltage Sensing

Similar to input voltage sensing, the output voltage is also sampled through a resistor divider with a fixed ratio (0.0032) on FBP. The voltage on FBP is sampled by the 10 bits ADC, and the results are used for on-time calculations and several protection functions.

The internal pull-down resistor should be considered when designing the external resistor divider. Make the total divided ratio equal to 0.0032, calculated with Equation (1):

$$\frac{R_{FBP-L} // R_{FBP-int\,ernal}}{R_{FBP-H} + R_{FBP-L} // R_{FBP-int\,ernal}} = 0.0032 \quad (1)$$

Where R_{FBP-H} is the external divider resistor connected on the high side, and R_{FBP-L} is the external divider resistor connect on the low side.

Figure 13 shows the output voltage level that is defined for different functions.

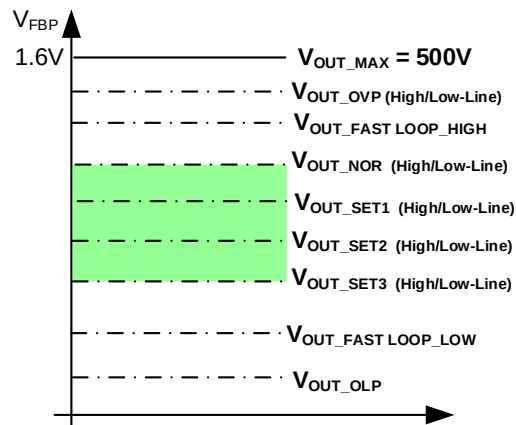


Figure 13: Output Voltage Levels

Output Regulation

To optimize efficiency, the output voltage can be auto-regulated according to the input voltage and output power. The output voltage can be set to two different options based on $V_{IN_HIGH/LOW}$, and from there four different options according to the power levels. In total, there are eight options for PFC output regulation that can be configured using the GUI.

Output Over-Voltage Protection (OVP)

The over-voltage protection (OVP) threshold (V_{OUT_OVP}) is set in the MTP register using the GUI. The digital value is converted to an analog signal by DAC and compared with the FBP pin voltage. If the output voltage exceeds V_{OUT_OVP} , PFC switching stops. If the output voltage returns to the regulated target, the PFC resumes switching. Figure 14 shows the internal OVP block.

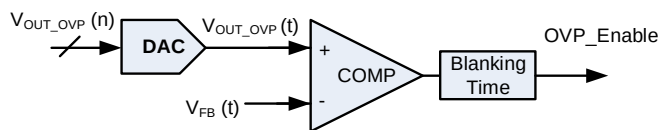


Figure 14: PFC OVP Circuit

A blanking time is inserted into OVP to keep the IC immune to switching noise interference (see Figure 15). This blanking time is configurable in the GUI.

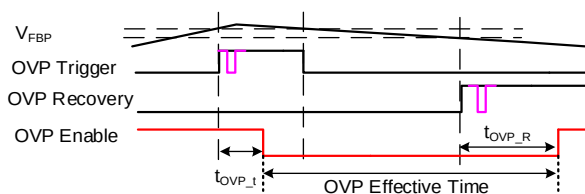


Figure 15: Output OVP

Fast Loop

In a dynamic load event, the PFC output voltage may drop or rise due to the low bandwidth of the PFC control loop; this can lead to the output voltage being out of spec. Fast loop can be enabled to improve the PFC dynamic performance. Fast loop is activated when the output voltage drops below $V_{OUT_FAST_LOOP_LOW}$ or rises above $V_{OUT_FAST_LOOP_HIGH}$, based on whether the fast loop low level or fast loop high level is enabled, respectively. When fast loop is activated, K_I and K_P switch to their fast loop settings. The fast loop functions are enabled/disabled using the GUI, which also allows for configuration of the fast loop's parameters.

Open-Loop Protection

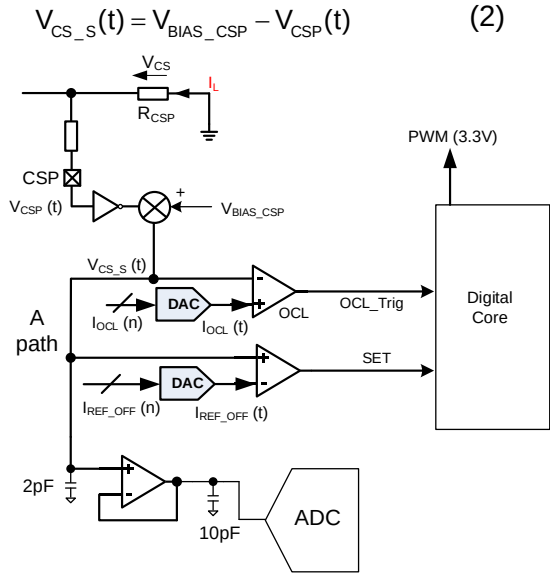
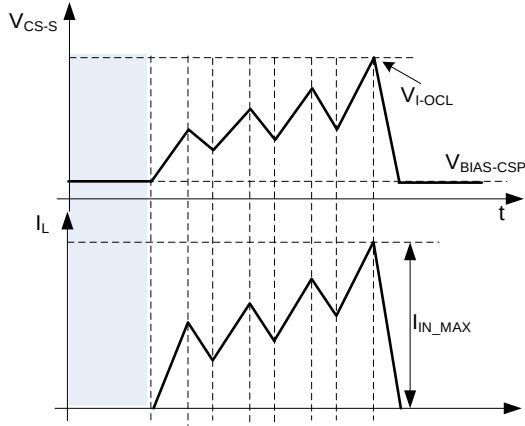
When the FBP voltage (V_{FBP}) falls below V_{OUT_OLP} for longer than configured, an open-loop condition occurs. The IC enters latch mode or auto-restart protection mode (selectable in the GUI) when this condition occurs.

If the IC is in latch protection mode and V_{CC} drops below V_{CCRST} , the switching is latched off, and can only restart when V_{CC} is charged above $V_{CCON(HV)}$.

If the IC is in auto-restart protection mode, the switching is suspended for the duration of the auto-restart timer (set via the GUI). Switching restarts after the timer runs out. If the user sets "self-power mode" in the GUI (which uses aux winding to power VCC), the IC must wait for VCC be charged above $V_{CCON(HV)}$ to restart.

Peak Current Sensing

The PFC inductor current is sensed by R_{CSP} and produces a negative voltage (V_{CSP}). It is internally converted into a positive voltage with a bias (V_{CS_S}) (see Figure 16 and Figure 17). The ADC samples V_{CS_S} when the PFC gate turns off, which can be calculated with Equation (2):

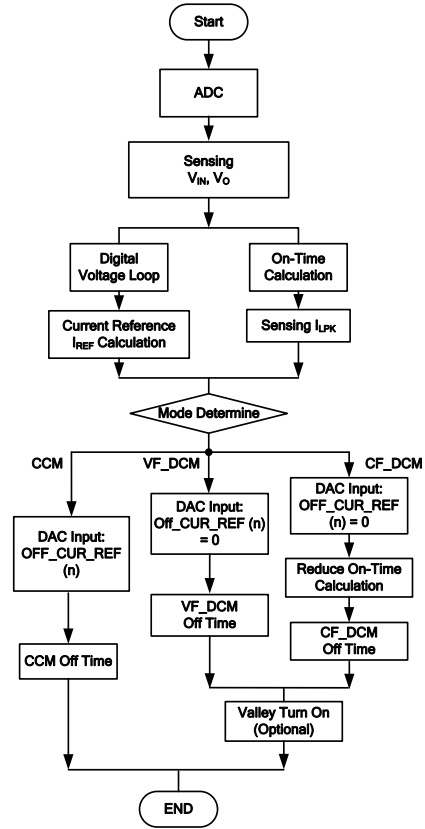

Figure 16: Current-Sense Circuit in the CSP Pin

Figure 17: V_{CS_S} Voltage Waveform

Over-Current Limit (OCL)

The HR1210 adopts a cycle-by-cycle over-current limit (OCL) to protect the PFC MOSFET from overstress. This over-current limit is implemented by comparing V_{CS_S} with an internal OCL threshold. The OCL threshold is an analog signal output of an 8-bits DAC. The internal OCL threshold can also be calculated similarly to Equation (3). An LEB1 ($t_{OCL_BLANKING}$) is inserted to avoid switching noise. R_{CSP} and the OCL current must be input into the GUI.

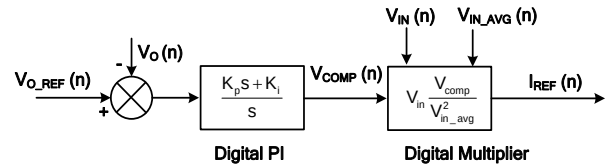
Digital PFC Control Scheme

Figure 18 shows the flowchart of the digital control.


Figure 18: Flowchart of the PFC Control Scheme

Digital Current Reference

The HR1210 adopts a digital PI compensation for the voltage control loop. Its output $V_{COMP}(n)$, is sent to the multiplier for the current reference calculation (see Figure 19).


Figure 19: Current reference

The digital current reference can be calculated with Equation (3):

$$I_{REF}(n) = V_{IN}(n) \times \frac{V_{COMP}(n)}{(0.5 \times V_{IN_PK}(n))^2} \quad (3)$$

On-Time Calculation

The on time can be estimated with Equation (4):

$$t_{ON}(n) = \frac{V_{O_REF} - V_{IN}(n)}{V_{O_REF}} \times t_s \quad (4)$$

Where t_s is the switching period that is configurable using the GUI.

PFC Operating Mode Selection

The HR1210 has three operation modes for PFC: continuous conduction mode (CCM), variable-frequency discontinuous conduction mode (VF-DCM), and constant-frequency discontinuous conduction mode (CF-DCM). The peak value of the inductor current in CCM should satisfy the following relationship, estimated with Equation (5):

$$I_{PK}(n) < 2I_{REF}(n) \quad (5)$$

The peak value of the inductor current in VF-DCM should satisfy the following relationship, calculated with Equation (6):

$$2I_{REF}(n) < I_{PK}(n) < 2I_{REF}(n) \cdot \frac{t_{S_MAX}}{t_s} \quad (6)$$

The peak value of the inductor current in CF-DCM can be estimated with Equation (7):

$$I_{PK}(n) > 2I_{REF}(n) \cdot \frac{t_{S_MAX}}{t_s} \quad (7)$$

Where t_{S_MAX} is the maximum switching period configurable via the GUI.

CCM Operation

When the converter operates in CCM, the $OFF_CUR_REF(n)$ is calculated and sent to DAC after a digital filter with configurable cross-frequency. The DAC then outputs an analog signal ($OFF_CUR_REF(t)$), which is compared with $V_{CS}(t)$. If $V_{CS}(t)$ is below $OFF_CUR_REF(t)$, then the signal is set high, and the PWM is also set high (see Figure 20).

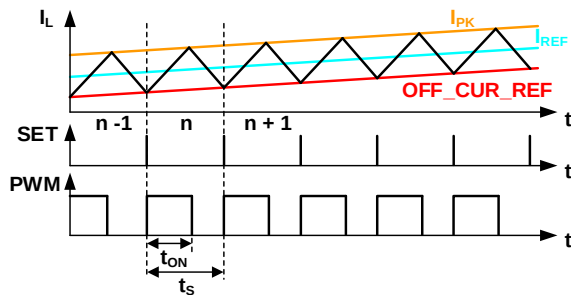


Figure 20: CCM Control Signals

The off current reference in CCM can be calculated with Equation (8):

$$OFF_CUR_REF(n) = 2I_{REF}(n) - I_{PK}(n) \quad (8)$$

VF-DCM Operation

When the converter operates in VF-DCM, the off current reference is set to 0A. In this case, the set signal represents the boundary of DCM (see Figure 21).

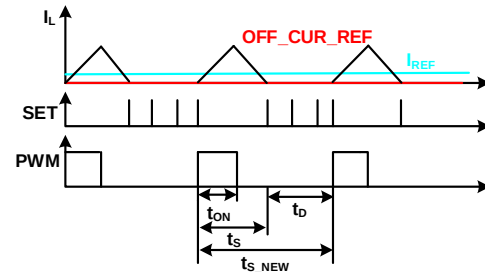


Figure 21: VF-DCM Control Signals

The new switching period can be calculated with Equation (9):

$$t_{S_NEW}(n) = \frac{I_{PK}(n)}{2I_{REF}(n)} t_s \quad (9)$$

The delay time can be calculated with Equation (10):

$$t_D(n) = t_{S_NEW}(n) - t_s = \left(\frac{I_{PK}(n)}{2I_{REF}(n)} - 1 \right) \times t_s \quad (10)$$

The calculated delay time has a digital filter with configurable cross frequency.

CF-DCM Operation

When the converter operates in CF-DCM, the off current reference is also set to 0A (see Figure 22).

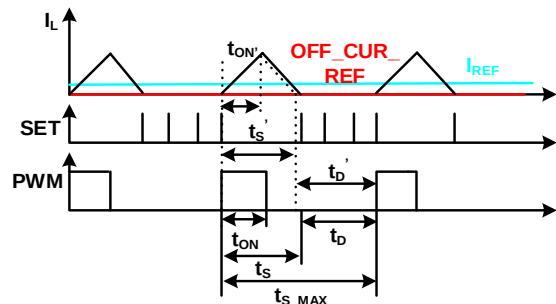


Figure 22: CF-DCM Control Signals

In this mode, the switching frequency is limited to the minimum switching frequency that can be set via the GUI. The PWM duty is modulated to achieve average current control. The new switching period can be calculated with Equation (11):

$$\frac{1}{2} I_{PK}'(n) \cdot t_S'(n) = I_{REF}(n) \times t_{S_MAX} \quad (11)$$

As t_{ON} changes, the peak value of inductor current can be seen as unchanged, which is estimated with Equation (12):

$$I_{PK}'(t) = I_{PK}(t) \quad (12)$$

The peak inductor current can be used to find the switching period, estimated with Equation (13):

$$t_S'(n) = \frac{2I_{REF}(n)}{I_{PK}(n)} \times t_{S_MAX} \quad (13)$$

The new turn-on time can be calculated with Equation (14):

$$t_{ON}'(n) = \frac{V_{O_REF} - V_{IN}(n)}{V_{O_REF}} \times t_S'(n) \quad (14)$$

The delay time can be calculated with Equation (15):

$$t_D'(n) = t_{S_MAX} - t_S'(n) = \left(1 - \frac{2I_{REF}(n)}{I_{PK}(n)}\right) \times t_{S_MAX} \quad (15)$$

The calculated delay time also has a digital filter with a configurable cross-frequency.

Soft Start

When the AC brown-in is triggered, the V_{IN_OK} signal goes high and the HR1210 initiates a soft start (see Figure 23).

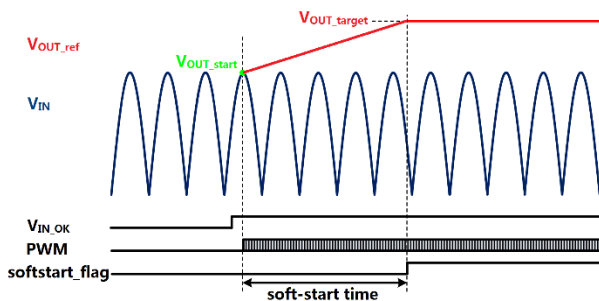


Figure 23: Soft-Start Sequence

During soft start, the internal voltage reference slowly ramps up to the regulation target. The ramp slew rate is determined by the soft-start time-set by the high and low lines, respectively,

which are configurable with the GUI. When the voltage reference on FBP rises to the regulation target value, $SOFT_START_FLAG$ is set high, and soft start completes. Generally, the output voltage cannot be built up during soft start, and is regulated afterwards.

The slew rate is different at high-line and low line, which can be configured with the GUI.

Burst Mode

At light loads, the IC is designed to run in burst mode to improve efficiency and lower no-load power consumption. Once the output load drops below the threshold (a percentage of the rated load), the PFC enters burst mode. The threshold can be programmed via the GUI for both high-line and low-line conditions.

In burst mode, the switching duty is calculated based on the set threshold, and the output is regulated to V_{O_TARGET} with a hysteresis. The PFC stops switching when the output voltage reaches $V_{O_TARGET} + 5V$, and resumes switching when the output voltage drops below V_{O_TARGET} .

The HR1210 is designed to exit burst mode only at the peak point of the AC line in order to minimize the current stress. There is a threshold voltage that can be configured via the GUI to prevent the bus voltage from dropping too low under transient. If the bus voltage drops below the threshold, the IC exits burst mode immediately without waiting for peak point detection.

Power Factor Compensation

Traditional PFC control schemes only regulate the inductor current to match the shape of the input voltage. However, the input capacitor current is not controlled, which may cause PF deterioration and an undesired phase delay. With a larger capacitor or a higher input voltage, the PF becomes less efficient, especially at light-load conditions.

To improve the PF, the HR1210 implements a patented method to compensate the input capacitor current. There are four input voltage ranges and input capacitors set for the compensation setting, which are configurable in the GUI and are stored in the IC MTP. With this

function, the PF can be more effective across the whole input voltage range.

Frequency Jittering

The HR1210 implements a jitter function that can reduce EMI noise. When jitter is enabled, the switching frequency is modulated by a triangular waveform with the modulation frequency of f_M . It is modulated to the maximum value at the peak of the triangle, and to the minimum value at the valley of the triangle. The modulation amplitude and f_M are configurable using the GUI. Figure 24 shows the jitter switching frequency modulation.

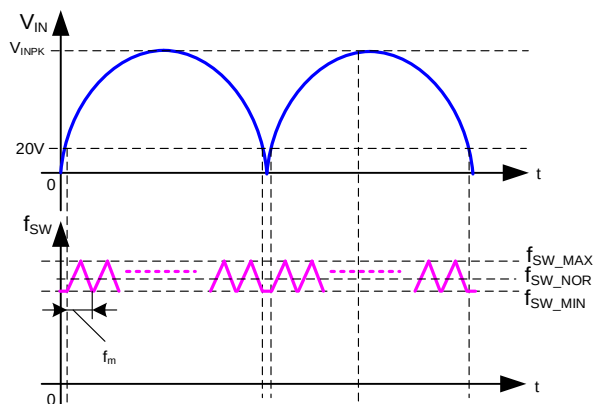


Figure 24: Switching Frequency Modulation during Jitter

Digital LLC Controller

LLC Brown-In/Out

The LLC starts to work when the bus voltage rises above the brown-in threshold. The LLC shuts down when the bus voltage drops below the brown-out threshold. There is a programmable timer delay in the GUI for both brown-in and brown-out for the LLC switch.

Soft Start

During LLC soft start, the internal V_{COMP} is overridden by a soft-start generator output voltage. The soft-start timer can be set via the GUI to define the soft-start time.

At the beginning of soft start, the low-side gate (LSG) turns on first for a configurable time to charge the BST capacitor. Then the high-side gate (HSG) and LSG alternate turning on and off.

Because of resonant capacitor (C_R) voltage imbalance during start-up, the current slew rate in the resonant tank has a significant difference

between the HSG and LSG gate driver turn-on period.

The HR1210's LSG gate driver does not turn off until the resonant tank current drops below 0A ($V_{CSHB} < V_{CSNR}$) to avoid hard switching during soft start (see Figure 25).

If both the HSG and LSG are driven with a 50% duty cycle, the resonant tank current may not reverse in a switching half-cycle, which may lead to hard switching.

Figure 25 shows the waveform difference between 50% duty cycle driving.

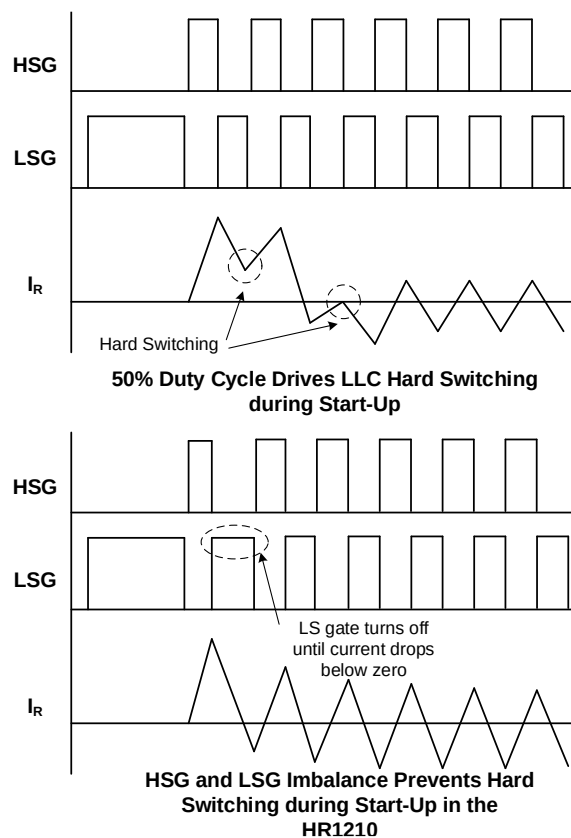


Figure 25: LLC Start-Up to Avoid Hard Switching in the HR1210

Current Mode Control

Figure 26 shows the control block diagram of the HB LLC. The on-time comparator determines the HSG on time by comparing the voltage derived from the current sense (V_C) with V_{COMP} , which is generated from the feedback voltage on the optocoupler (FBL).

The LSG follows the HSG on time. A digital counter with a $1 / f_{OSC1_NOR}$ minimum step is

implemented to ensure the on time matches between the HSG and LSG.

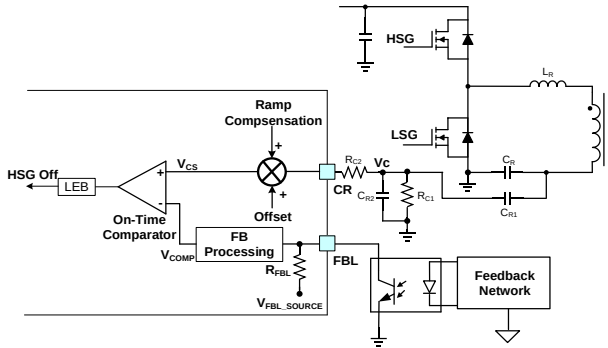


Figure 26: LLC Current Mode Control Block Diagram

Figure 27 shows the LLC current mode control waveform.

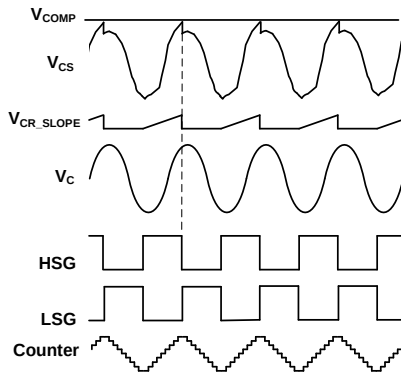


Figure 27: LLC Current Mode Control Waveform

The current-sense voltage (V_C) is proportional to the voltage on the resonant tank capacitor (C_R). The proportion is determined by the external capacitor divider (C_{R1} , C_{R2}). The capacitor dividing ratio should be set to ensure the proper maximum output power (primary current) of the LLC stage can be delivered.

To prevent subharmonic oscillation, a digital 4-bit configurable slope compensation can be added. The compensation voltage (V_{CR_SLOPE}) is the product of the slope and on time, and is added to V_C to generate V_{CS} .

The HR1210 senses the voltage of the optocoupler on FBL (V_{FBL}), which generates the reference (V_{COMP}) of the internal on-time comparator. The LSG follows the previous HSG on time but will not turn off until V_{CS} drops below V_{COMP} . There is an internal pull-up resistor (R_{FBL}), and V_{FBL} increases when the output load

increases. V_{FBL} is used for skip/burst mode detection and over-power protection (OPP).

Operation Mode

The LLC works in three modes: continuous mode, skip mode, and burst mode. The controller samples the FBL pin voltage via the 10-bit ADC to determine which mode the LLC should work at.

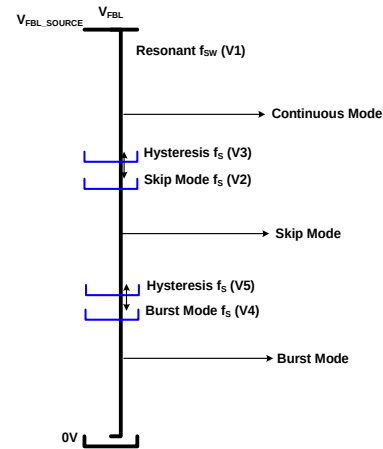


Figure 28: LLC Working Mode Determined by FBL

Figure 28 shows the LLC working mode based on the different FBL voltage (V_{FBL}) level. When V_{FBL} reaches the threshold that triggers skip mode (V2), the LLC system enters skip mode. If V_{FBL} drops (the load decreases) below the threshold that triggers burst mode (V4), the LLC switch triggers burst-off, and LLC enters burst mode. The skip mode and burst mode thresholds have exit levels with a hysteresis (V3 and V5) above which the LLC goes back to continuous mode or skip mode, respectively. All the thresholds (V2 to V5) are configurable via the GUI.

In skip mode and burst mode, V_{COMP} is estimated with Equation (16):

$$V_{COMP} = A_X \times V_{FBL} + B_X \quad (16)$$

Where A_X is the proportional coefficient, and B_X is an offset for V_{COMP} . Both can be set via the GUI.

In continuous mode, V_{COMP} is calculated with Equation (17):

$$V_{COMP} = V_{FBL} - V_{FBL_OFFSET} \quad (17)$$

Figure 29 shows the V_{COMP} generation block diagram.

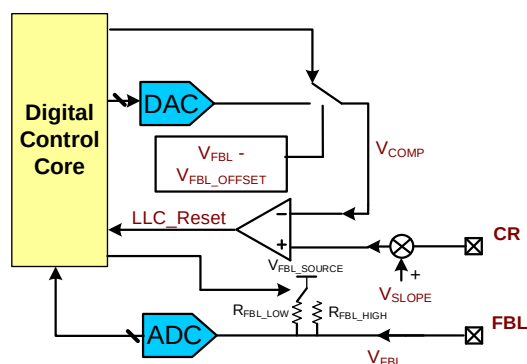


Figure 29: V_{COMP} Generation Block Diagram

Skip Mode

For frequency control of the HB LLC topology, the switching frequency increases as the load decreases, and this leads magnetization loss and switching loss to increase during light-load conditions. To reduce the power consumption while regulating the output, the HR1210 implements skip mode to reduce the average switching frequency, thus reducing the magnetic losses.

When the system enters skip mode, a switch idle time is inserted between every N (programmable in the GUI) switching cycle. The skip period (t_{SKIP}) is kept at the configured value for stability. The first HSG gate after the idle time is always turned on at the HB peak point (ZVS) to minimize the switching loss (see Figure 30).

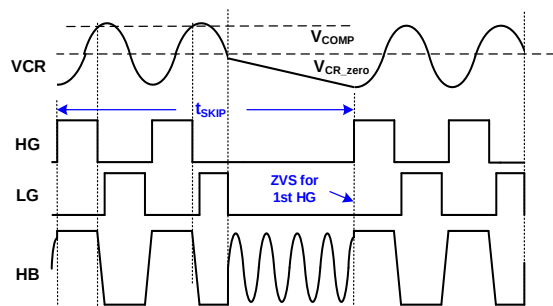


Figure 30: LLC Skip Mode

The switching frequency of HSG and LSG follows the current mode control scheme as described previously, except that the last LSG (during one skip cycle) on-time will end when V_{CR} drops V_{CR_ZERO} .

Burst Mode

To further limit the average switching frequency as the load gets lighter, a longer switch idle time is inserted into the skip mode. This is called burst mode.

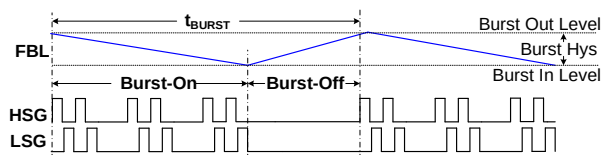


Figure 31: LLC Burst Mode

The LLC works in skip mode during burst-on (see Figure 31). During burst-off, the switching is completely off. Burst-off ends when the FBL voltage (V_{FBL}) exceeds the (configurable) burst out threshold.

To minimize the audible noise created by burst mode, users can activate the burst frequency control function via the GUI to limit the burst frequency to a low value. With this function activated, the burst frequency ($1 / t_{BURST}$) can be adjusted to a preset range (using the GUI) by increasing or decreasing the switching pulses during burst-on.

The HR1210 has a large, switchable FBL pull-up resistor R_{FBL_HIGH} to reduce the optocoupler current in deep burst mode. When the operation condition is ready for FBL pull-up resistor switch, it gradually switches between R_{FBL_LOW} and R_{FBL_HIGH} . The time frame in which the switching counts during one burst-on period is less than the set value, which is programmable in GUI.

The HR1210 features an ultra-low power mode. It enters ultra-low power mode when the PFC is in burst-off and V_{FBL} is below the ultra-low power mode threshold. In this mode, the IC consumption is reduced by shutting down some of the internal circuits. This is implemented by an internal comparator that compares V_{FBL} with a configurable reference from the 8-bit DAC.

If the BST capacitor is discharged during burst-off and the device is in deep burst mode, the LSG is turned on for a configurable time (t_{HSG_ini}) when the burst-off time (t_{B-off}) exceeds the timer, which is set by the GUI to charge the BST voltage.

Adaptive Dead-Time Adjustment (ADTA)

The dead-time period between HSG and LSG drivers should always be in half-bridge topologies to prevent and cross-conduction through the power stage MOSFETs, which may result in excessive current, high EMI, and destruction in practical applications. A traditional, fixed dead-time control scheme is widely used in resonant converters due to its simple implementation. However, this method may lead to hard switching in light loads or large L_M design conditions, which eventually leads to thermal and reliability issues.

The HR1210 incorporates an intelligent ADTA logic circuit, which is capable of detecting the dV/dt of SW through an internal high-voltage capacitor. This circuit automatically inserts a proper dead time with respect to the actual operating conditions of the converter. Figure 32 shows the simplified block diagram of the ADTA.

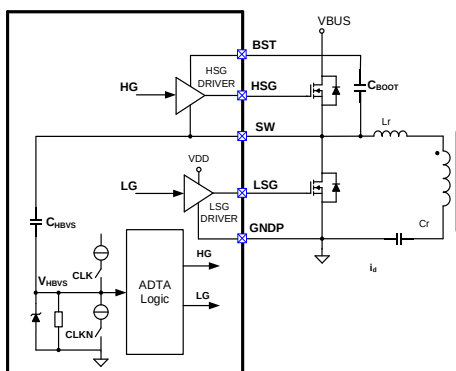


Figure 32: Block Diagram of ADTA

Once the HSG switches off, SW goes from a high voltage to a low voltage driven by the resonant tank current (I_R). A negative dV/dt draws a current from C_{HBVS} , which pulls V_{HBVS} down. If the current exceeds the internal bias current, V_{HBVS} is pulled down to zero and clamped. When the SW slew rate becomes slower, the current drawn through V_{HBVS} also decreases, and V_{HBVS} starts to ramp up. This V_{HBVS} voltage change is used for dead-time detection, and the LSG will switch on after a delay time.

Figure 33 shows the operation waveform of ADTA.

The dead time is the duration between the HSG switch turning off and the LSG switch turning on. The dead time relies on the completion of SW's transition.

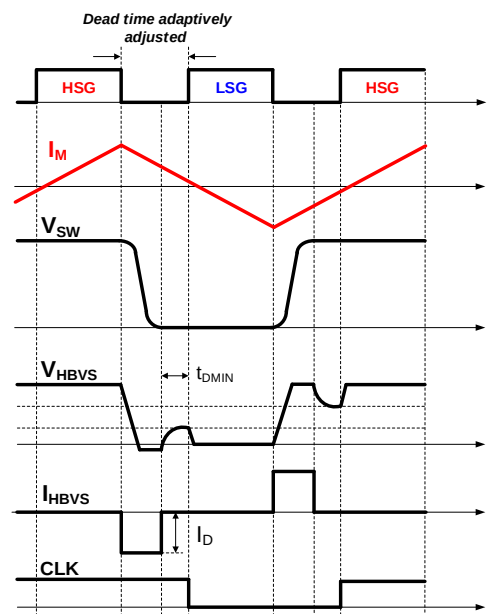


Figure 33: Operation Waveform of ADTA

When the LSG switches off, SW goes from zero to high, creating an input current from C_{HBVS} . The dead time also is adjusted automatically with the opposite logic.

There are three possible dead times: minimum dead time (t_{DMIN}), maximum dead time (t_{DMAX}), and adaptive dead time (between t_{DMIN} and t_{DMAX}). When the transition time of SW is less than t_{DMIN} , the logic blocks the HSG and LSG until t_{DMIN} is reached. This avoids any shoot-through of the high-side and low-side MOSFET. If the dead time is too long, it may lead to duty cycle loss and loss of soft switching. Maximum dead time t_{DMAX} forces the gate to switch on under this condition. Both t_{DMIN} and t_{DMAX} are configurable via the GUI.

Figure 34 shows the possible dead times under ADTA logic.

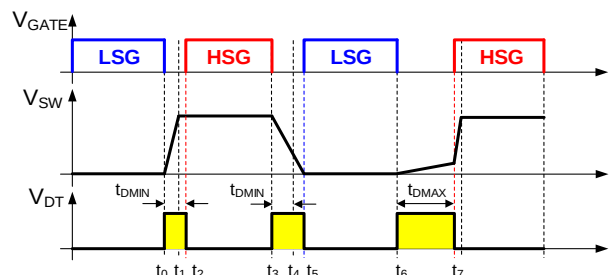


Figure 34: Min, Max, and Adaptive Dead Time

Capacitive Mode Protection (CMP)

If fault conditions such as overload, short circuit, or a load transient occur, the LLC converter may enter capacitive mode protection (CMP). In capacitive mode, the voltage applied on the resonant tank lags behind the current, which makes the MOSFETs lose ZVS. The device may be damaged, so it is not recommended to leave the converter in capacitive mode.

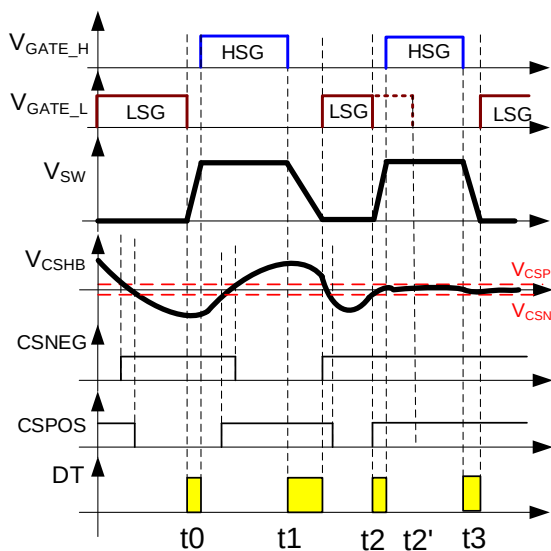


Figure 35: Operating Principles of CMP

Figure 35 shows the principles of capacitive mode protection. CSPOS and CSNEG are the current polarity flags, which are generated by comparing the voltage of the CSHB pin with the internal V_{CSPR} and V_{CSNR} voltage thresholds.

t0: At t0, the converter operates in inductive mode. $V_{CSHB} < V_{CSNR}$ when the low-side gate (LSG) driver is turned off. The current flows at the right polarity (negative). CMP does not occur.

t1: At t1, the converter is operates in inductive mode. $V_{CSHB} > V_{CSPR}$ when the high-side gate (HSG) driver is turned off. The current flows at right polarity (positive). CMP does not occur.

t2: At t2, the LLC converter works in capacitor mode. V_{CSHB} reaches V_{CSNR} . The LSG is forced off to avoid this mode. Without capacitor mode protection, the LSG does not turn off until t2'.

If V_{CSHB} never exceeds V_{CSPR} while the HSG is on, CMP is not activated while the HSG turns off. Vice versa, if V_{CSHB} never drops below V_{CSNR} while the LSG is on, CMP is not activated when the LSG turns off.

Over-Current Protection (OCP)

The HR1210 provides short-circuit protection by triggering the V_{CSHB} voltage at V_{CS_OCP} . An internal counter is incremented each time V_{CS_OCP} is triggered. OCP occurs when the counter counts to the set value (configurable via the GUI) (see Figure 36). This condition generally occurs when the CSHB pin voltage continues to rise during a short circuit.

The IC can be selected for latch protection mode or auto-restart protection mode using the GUI when LLC OCP occurs.

The IC behavior in latch or auto restart protection mode is described in the Open-Loop Protection (OLP) section on page 21.

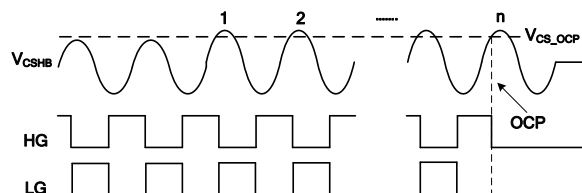


Figure 36: OCP Sequence

Current Sensing on CSHB

Both CMP and OCP detect the current signal on CSHB. A proper current-sensing circuit should be designed on CSHB.

There are two kinds of current-sensing circuits: capacitor divider based lossless, and sense resistor. Lossless current sensing is typically preferred in high-power applications (see Figure 37).

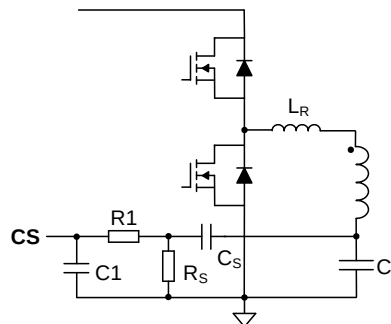


Figure 37: Current Sensing with Lossless Network

To design the lossless current-sensing network, Equation (18) should be satisfied:

$$C_S \leq \frac{C_R}{100} \quad (18)$$

To avoid mistriggering, the capacitive detection threshold V_{CSPR} (or V_{CSNR}) in normal light-load conditions, R_S should fulfill the condition below, estimated with Equation (19):

$$R_S > \frac{V_{CSPR}}{I_M} \times \left(1 + \frac{C_R}{C_S}\right) \quad (19)$$

Where I_M is the peak magnetizing current, calculated with Equation (20):

$$I_M = \frac{V_{BUS}}{8L_M \times f_{max}} \quad (20)$$

Where V_{BUS} is the LLC input voltage, L_M is the transformer winding inductance and f_{MAX} is the maximum switching frequency.

R_S should be smaller than the value calculated with Equation (21):

$$R_S < \frac{V_{CS_OCP}}{I_{CPRK}} \times \left(1 + \frac{C_R}{C_S}\right) \quad (21)$$

Where I_{CPRK} is the peak current of the resonant tank at a low input voltage and full load. I_{CPRK} can be estimated with Equation (22):

$$I_{CPRK} = \sqrt{\left(\frac{N \times V_O}{4L_M \times f_s}\right)^2 + \left(\frac{I_O \times \pi}{2N}\right)^2} \quad (22)$$

Where N is the turn ratio of transformer, I_O is the output current, V_O is the output voltage, f_{sw} is the switching frequency, and L_M is the magnetizing inductance.

The $R1$ and $C1$ network is used to attenuate switching noise in the CSHB pin.

The sense resistor current-sensing solution is to use a sensing resistor in series with the resonant tank (see Figure 38). This method is simpler with fewer external components, but may cause undesired power consumption on the sensing resistor.

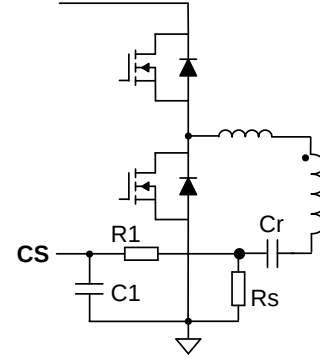


Figure 38: Current-Sensing with a Sense Resistor

The sense resistor can be estimated with Equation (23):

$$R_S < \frac{V_{CS_OCP}}{I_{CPRK}} \quad (23)$$

Over-Power Protection (OPP)

Over-power protection (OPP) can protect the LLC converter from excessive over-power conditions.

The HR1210 monitors the FBL pin voltage (V_{FBL}). If V_{FBL} exceeds V_{OPP_LLC} (configurable via the GUI), an internal programmable timer is set. This timer is reset once V_{FBL} falls below V_{OPP_LLC} . OPP is triggered if the timer counts to the end without resetting. V_{OPP_LLC} should not exceed the minimum value of V_{FBL_SOURCE} .

Latch protection mode and auto-restart protection mode are optional responses for OPP in the GUI.

The IC behavior in latch or auto-restart protection mode is described in the Open-Loop Protection (OLP) section on page 21.

Protection on SO Pin

The HR1210 monitors the voltage on the SO pin (V_{SO}) and provides a protection function when V_{SO} exceeds V_{SO_OVP} for a programmable timer t_{OVP_STABLE} .

The SO pin can be connected to the primary auxiliary winding with a resistor divider to sense the output voltage and when to trigger over voltage protection (OVP).

V_{SO} can be estimated with Equation (24):

$$V_{SO} = \frac{R_{SO1}}{R_{SO1} + R_{SO2}} \times \frac{N_{PAU}}{N_S} \times (V_O + V_{FD}) \quad (24)$$

Where: N_{PAU} is the turns of auxiliary winding, N_S is the number of secondary winding turns, V_O is the output voltage, and V_{FD} is forward voltage drop of the output rectifier or SR. R_{SO1} and R_{SO2} are the sampling voltage dividers.

An external NTC can also be used on SO as an external OTP function. Pull up the SO pin with an NTC resistor to a constant voltage source (e.g. V_{REG}). V_{SO} can be estimated with Equation (25):

$$V_{SO} = \frac{R_{SO}}{R_{NTC} + R_{SO}} \times V_{REG} \quad (25)$$

Where R_{SO} is the external pull-down resistor connecting SO to GND, and V_{REG} is the VREG pin voltage.

Figure 39 shows how the SO pin offers over-voltage protection (OTP) and over-temperature protection (OTP).

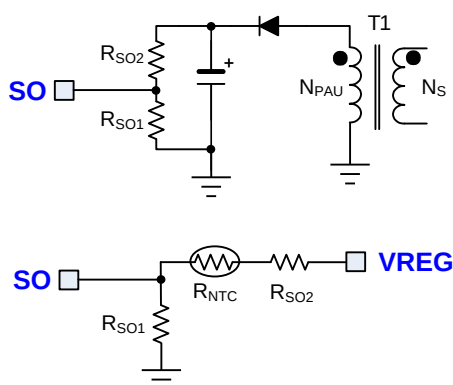


Figure 39: OVP and OTP via the SO Pin

The IC can be selected for latch protection mode or auto-restart protection mode using the GUI when the LLC SO protection triggers.

The IC behavior in latch or auto-restart protection mode is described in the Open-Loop Protection (OLP) section on page 21.

High-Side Gate Driver (HSG)

Figure 40 shows the high-side gate driver.

An external bootstrap (BST) capacitor is required to provide energy for the high-side gate driver. An integrated bootstrap diode charges this capacitor through VREG. This diode simplifies the external driving circuit for the high-side switch, allowing the BST capacitor to be charged when the low-side MOSFET is on.

Considering the BST capacitor charging time, in order to provide enough gate driver energy, a BST capacitor of 100nF to 470nF is recommended.

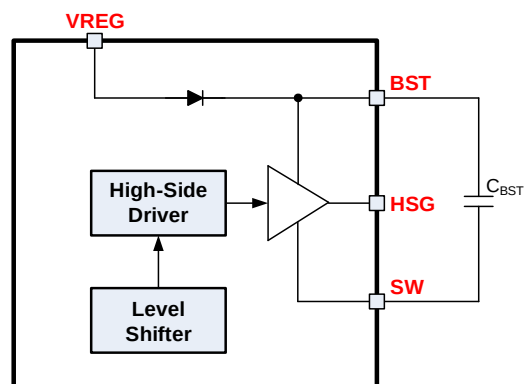


Figure 40: High-Side Gate Driver

PCB Layout Guidelines

- 1) Use the bulk capacitor's negative terminal as the ground for the PFC, LLC power loop, and IC ground. Ensure the ground layout overlap as small as possible.
- 2) The IC ground trace should be wide and short to reduce voltage drop.
- 3) Keep all the power loops and signal loop areas as small as possible.
- 4) Keep the signal traces far away from the switching point.
- 5) CSP and CSHB are key signals. These traces should be treated at the highest priority.

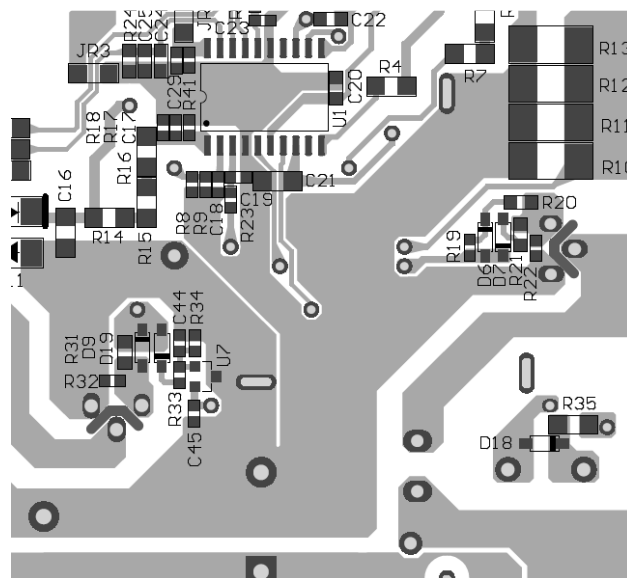
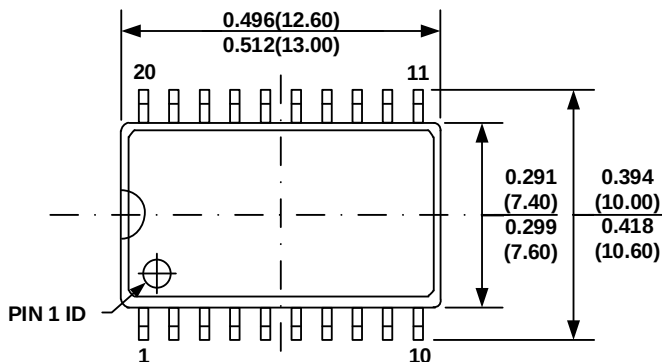


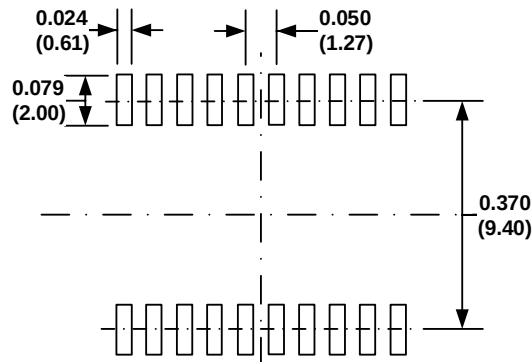
Figure 41: Grounding of IC and Power Loop

PACKAGE INFORMATION

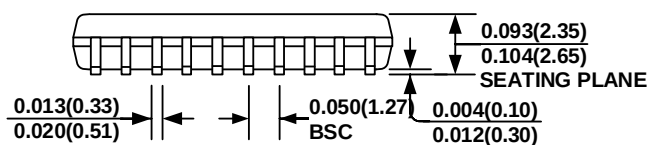
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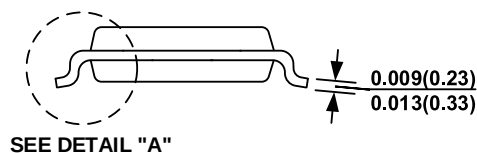
TOP VIEW



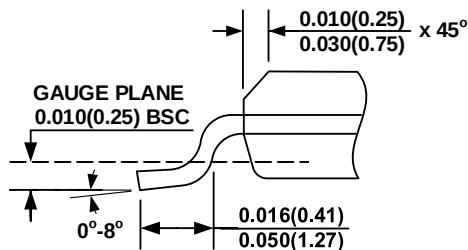
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



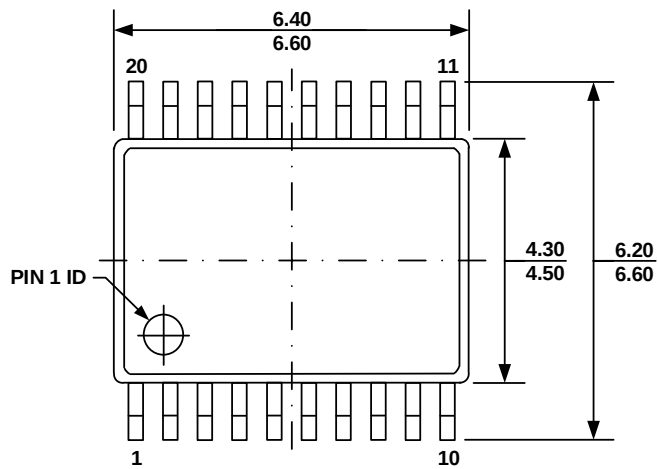
DETAIL "A"

NOTE:

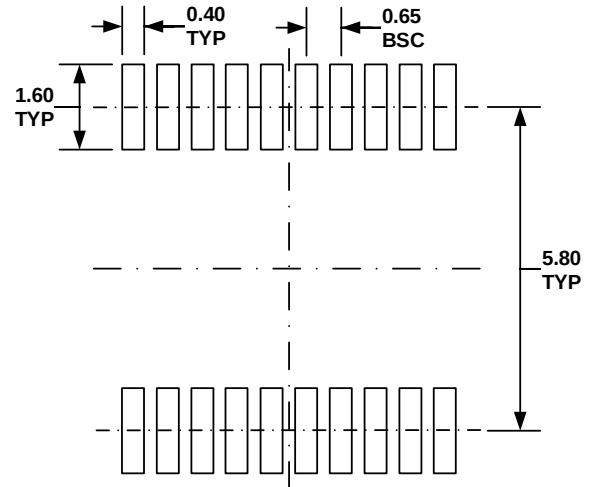
- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
- 6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION

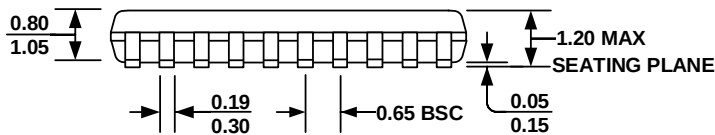
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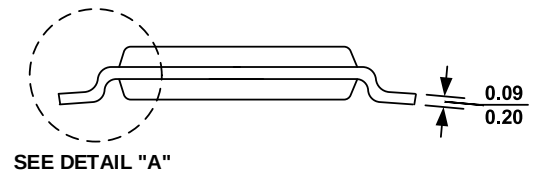
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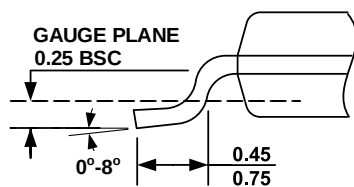
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

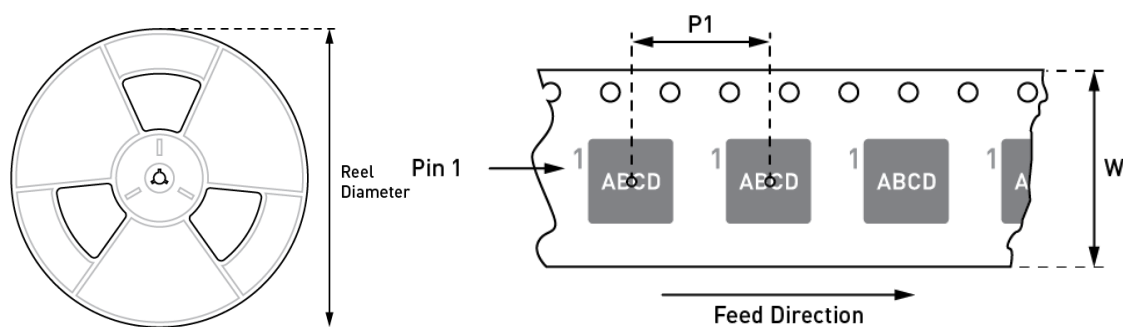


DETAIL "A"

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AC.
- 6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
HR1210GY-xxxx-Z	SOIC-20 (wide body)	1000	37	13in	24mm	12mm

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