MPM3683-7

2.7V-16V, 8A, Step-Down Power Module in QFN (7x7x4mm) Package

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MPM3683-10

DESCRIPTION

The MPM3683-7 is an easy-to-use, fully integrated, step-down, DC/DC power module with 8A of continuous current and 10A of peak current. The MPM3683-7 integrates a DC/DC converter, power inductor, and some basic passive components. The MPM3683-7 can deliver output current over a wide input voltage supply range with excellent load and line regulation.

The MPM3683-7 uses constant-on-time (COT) control to provide fast transient response and ease loop stabilization.

The operating frequency can be set to 600kHz, 800kHz, or 1000kHz easily with the MODE configuration, allowing the MPM3683-7 frequency to remain constant regardless of the input and output voltages.

The MPM3683-7 has an internal soft-start (SS) timer of about 1.6ms. This can be increased with an extra SS capacitor placed between TRK/REF and AGND. An open-drain power good signal indicates that the output voltage is within the nominal voltage range.

The MPM3683-7 has fully integrated, non-latched protection features including over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MPM3683-7 is available in a space-saving QFN-28 (7mmx7mmx4mm) package.

FEATURES

- Wide Input Voltage Range from 2.7V
  - 2.7V to 16V with External 3.3V Bias
  - 4V to 16V with Internal Bias or External 3.3V Bias
- Differential Output Voltage Remote Sense
- Low $R_{DS(ON)}$ Integrated Power MOSFETs
- Integrated Inductor
- Proprietary Switching Loss Reduction Technique
- Adaptive Constant-on-Time (COT) for Ultrafast Transient Response
- Stable with Zero-ESR Output Capacitor
- 0.5% Reference Voltage over 0°C to +70°C Junction Temperature Range
- 1% Reference Voltage from -40°C to +125°C Junction Temperature Range
- Selectable Pulse Skip or Forced Continuous Conduction Mode (CCM) Operation
- Excellent Load Regulation
- Output Voltage Tracking
- Output Voltage Discharge
- PG Active Clamped Low Level during Power Failure
- Programmable Soft-Start Time from 1.6ms
- Pre-Bias Start-Up
- Selectable Switching Frequency from 600kHz, 800kHz, and 1000kHz
- Non-Latch OCP, UVP, UVLO, Thermal Shutdown, and OVP
- Output Adjustable from 0.6V to up to 5.5V Max
- Available in a QFN-28 (7mmx7mmx4mm) Package

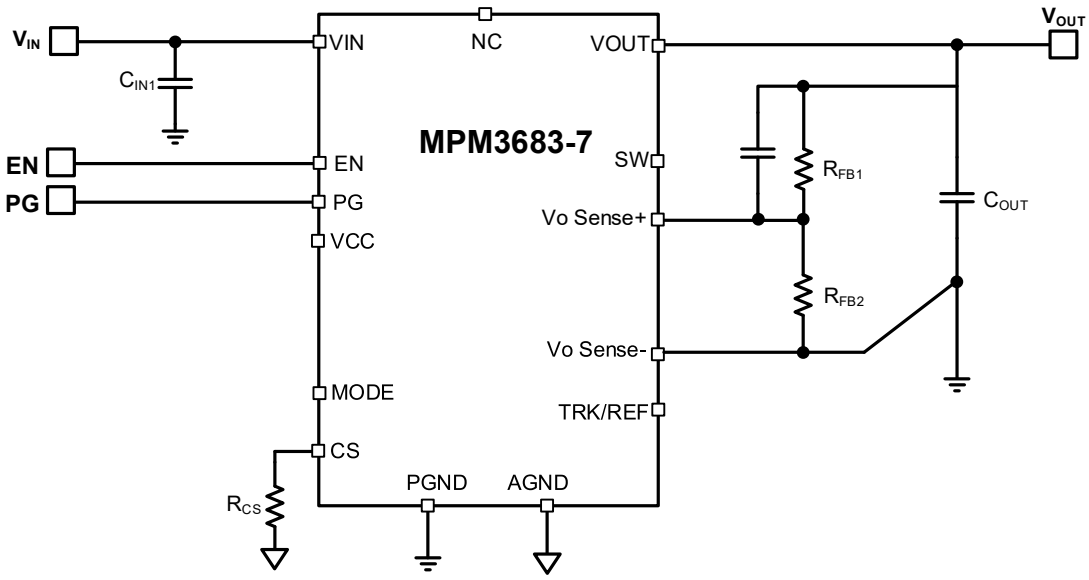
APPLICATIONS

- Telecom and Networking Systems
- Base Stations
- Industrial Systems
- Servers & Storage
- FPGA & ASIC Cards

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

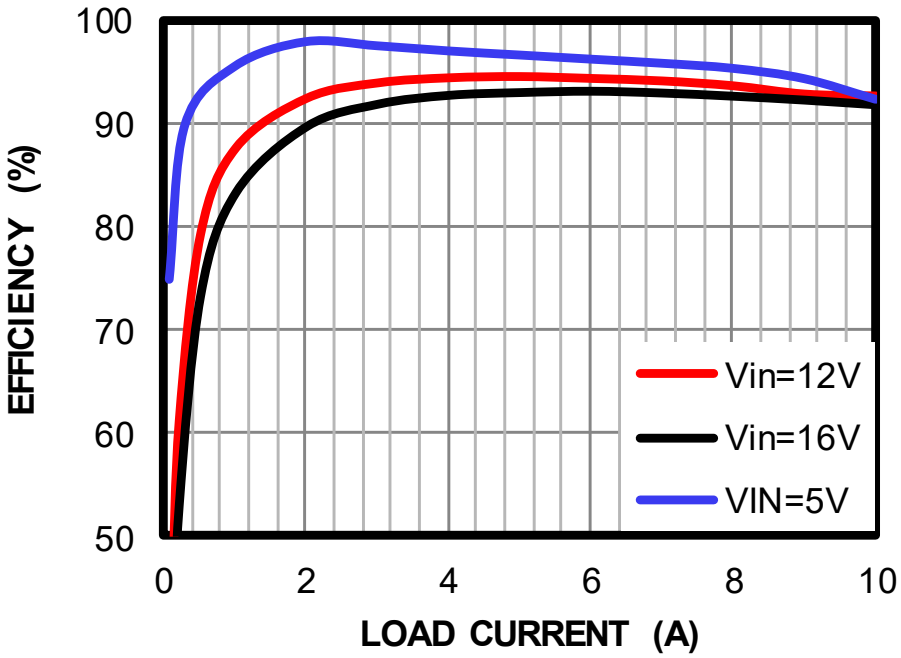
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION



Efficiency

V_{IN} = 5V/12V/16V, V_{OUT} = 3.3V, I_{OUT} = 0-10A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MPM3683-10

ORDERING INFORMATION

Part Number	Package	Top Marking	MSL
MPM3683GQN-7	QFN-28 (7mmx7mmx4mm)	*See Below*	3

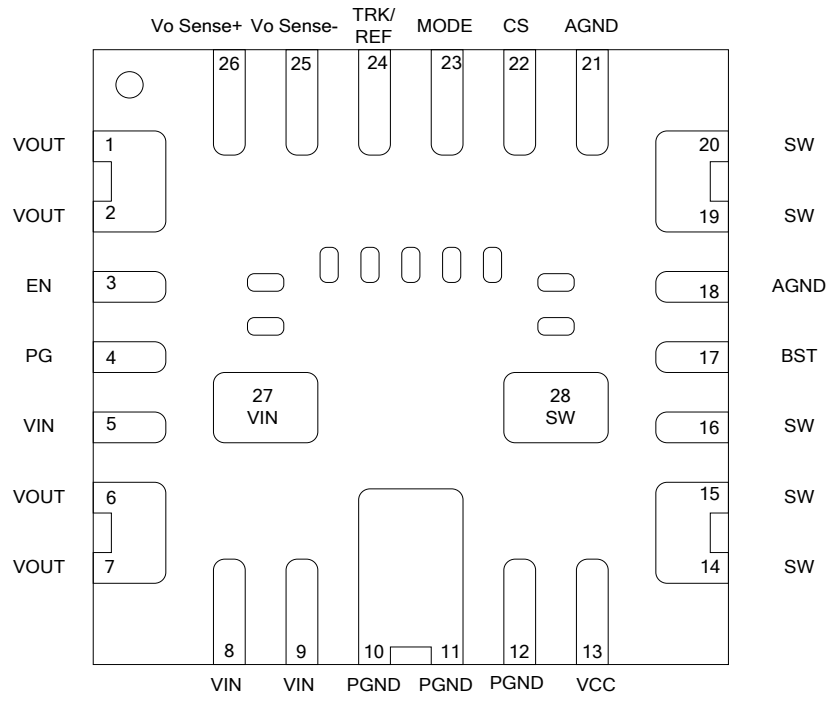
TOP MARKING

MPS YYWW
MP3683-7
LLLLLLLLL
M

MPS: MPS prefix
YY: Year code
WW: Week code
MP3683-7: Product code of MPM3683GQN-7
LLLLLLLLL: Lot number
M: Module

PACKAGE REFERENCE

TOP VIEW



QFN-28 (7mmx7mmx4mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1, 2, 6, 7	VOUT	**Module voltage output node.**
3	EN	**Enable.** EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. Connect EN to VIN through a pull-up resistor or a resistive voltage divider for automatic start-up. Do not float EN.
4	PG	**Power good output.** PG is an open-drain signal. A pull-up resistor (connected to a DC voltage) indicates high if the output voltage is within regulation. There is a delay of about 1ms from when Vo Sense+ becomes greater than or equal to 92.5% and when PG pulls high.
5, 8, 9, 27	VIN	**Input voltage.** VIN supplies power for the internal MOSFET and regulator. Input capacitors are needed at VIN to decouple the input rail. Use wide PCB traces to make the connection.
10, 11, 12	PGND	**System ground.** PGND is the reference ground of the regulated output voltage and requires careful consideration during the PCB layout. Use wide PCB traces to make the connection.
13	VCC	**Internal 3.3V LDO output.** The driver and control circuits are powered from the VCC voltage. The module integrates an LDO output capacitor and does not require an additional external capacitor.
14 - 16, 19, 20, 28	SW	**Switch output.** A large copper plane is recommended on SW to improve the thermal performance.
17	BST	**Bootstrap.** A bootstrap capacitor is integrated internally and does not require an external connection.
18, 21	AGND	**Analog ground.** Select AGND as the control circuit reference point.
22	CS	**Current limit.** Connect a resistor to ground to set the current limit trip point.
23	MODE	**Operation mode selection**. Program MODE to select CCM, pulse-skip mode, and the operating switching frequency. See Table 1 on page 16 for additional details.
24	TRK/REF	**External tracking voltage input.** The output voltage tracks the TRK/REF input signal. Decouple TRK/REF with a ceramic capacitor as close to TRK/REF as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. The capacitance of this capacitor determines the soft-start time. See Equation 2 on page 16 for additional details.
25	Vo Sense-	**Vo Sense-.** Connect Vo Sense- to the negative side of the voltage sense point directly. Short Vo Sense- to GND if the remote sense is not used.
26	Vo Sense+	**Vo Sense+.** Place a resistor from Vo Sense+ to GND to set the output voltage.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN} to GND).....-0.3V to 18V
$V_{SW(DC)}$ to GND .....-0.3V to V_{IN} + 0.3V
$V_{SW\ (25ns)}$ to GND.....-5V to 25V
V_{CC} 4.5V
All other pins .....-0.3V to +4.3V
Continuous power dissipation (T_A = +25°C) (2)
QFN-28 (7mmx7mmx4mm) 2.7W
Junction temperature .....170°C
Lead temperature .....260°C
Storage temperature..... -55°C to +170°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4V to 16V
$V_{IN(DC)}$ - $V_{SW(DC)}$ .....-0.3V to V_{IN} + 0.3V
$V_{SW(DC)}$.....-0.3V to V_{IN} + 0.3V
Output voltage (V_{OUT}).....0.6V to 5.5V
External VCC bias (V_{CC_EXT}).....3.12V to 3.6V
EN voltage(4) (V_{EN})..... 3.6V
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-28 (7mmx7mmx4mm)	32	11	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature.
3) The device is not guaranteed to function outside of its operating conditions.
4) EN pin has zener diode embedded for clamping the voltage at 3.6V. Please refer to the Operation Section for current limitation.
5) Measured on EVM3683-7-QN-01A.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, T_J = -40°C to 125°C (7), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		10	20	μA
Supply current (quiescent)	I_{IN}	V_{EN} = 2V, $V_{Vo\ Sense+}$ = 0.62V		650	850	μA
MOSFET						
Switch leakage	SW_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
	SW_{LKG_LS}	V_{EN} = 0V, V_{SW} = 12V		0	30	
Current Limit						
Current limit threshold	V_{LIM}		1.15	1.2	1.25	V
Low-side negative current limit	I_{LIM_NEG}			-9		A
Negative current limit time-out (6)	t_{NCL_Timer}			200		ns
Switching Frequency						
Switching frequency (7)	f_{SW}	MODE = GND, I_{OUT} = 0A, V_{OUT} = 1V, T_J = +25°C	480	600	720	kHZ
		MODE = 34.8kΩ, I_{OUT} = 0A, V_{OUT} = 1V, T_J = +25°C	680	800	920	kHZ
		MODE = 80.6kΩ, I_{OUT} = 0A, V_{OUT} = 1V, T_J = +25°C	850	1000	1150	kHZ
Minimum on time (7)	T_{ON_MIN}	$V_{VO\ SENSE+}$ = 500mV			50	ns
Minimum off time (7)	T_{OFF_MIN}	$V_{VO\ SENSE+}$ = 500mV			180	ns
Over-Voltage and Under-Voltage Protection (OVP, UVP)						
OVP threshold	V_{OVP}		113%	116%	119%	V_{REF}
UVP threshold	V_{UVP}		77%	80%	83%	V_{REF}
Feedback Voltage and Soft Start (SS)						
Feedback voltage	V_{REF}	T_J = -40°C to +125°C	594	600	606	mV
		T_J = 0°C to +70°C	597	600	603	mV
TRK/REF sourcing current	I_{TRACK_Source}	$V_{TRK/REF}$ = 0V		42		μA
TRK/REF sinking current	I_{TRACK_Sink}	$V_{TRK/REF}$ = 1V		12		μA
Soft-start time	t_{SS}	C_{TRACK} = 100nF, T_J = 25°C		1.6		ms
Error Amplifier						
Feedback current	$I_{Vo\ Sense+}$	$V_{Vo\ Sense+}$ = REF		50	100	nA
Enable and Under-Voltage Lockout (UVLO)						
Enable input rising threshold	VIH_{EN}		1.17	1.22	1.27	V
Enable hysteresis	$V_{EN\text{-}HYS}$			200		mV
Enable input current	I_{EN}	V_{EN} = 2V		0		μA
Soft shutdown discharge MOSFET	R_{ON_DISCH}			80	150	Ω
VIN UVLO						
VIN under-voltage lockout threshold rising	VIN_{Vth_Rise}	V_{CC} = 3.3V	2.1	2.4	2.7	V
VIN under-voltage lockout threshold falling	VIN_{Vth_Fall}		1.55	1.85	2.15	V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, T_J = -40°C to 125°C [7], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Regulator						
VCC under-voltage lockout threshold rising	VCC_{Vth_Rise}		2.65	2.8	2.95	V
VCC under-voltage lockout threshold falling	VCC_{vth_Fall}		2.35	2.5	2.65	V
VCC regulator	V_{CC}		2.88	3.00	3.12	V
VCC load regulation		Icc = 25 mA		0.5		%
Power Good (PG)						
Power good high threshold	$PG_{Vth_Hi_Rise}$	Vo Sense+ from low to high	89.5%	92.5%	95.5%	V_{REF}
Power good low threshold	$PG_{Vth_Lo_Rise}$	Vo Sense+ from low to high	113%	116%	119%	V_{REF}
	$PG_{Vth_Lo_Fall}$	Vo Sense+ from high to low	77%	80%	83%	V_{REF}
Power good low to high delay	PG_{Td}	T_J = 25°C		0.9		ms
Power good sink current capability	V_{PG}	I_{PG} = 10mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			3	µA
Power good low-level output voltage	V_{OL_100}	V_{IN} = 0V, pull PG up to 3.3V through a 100kΩ resistor @ 25°C		650	850	mV
	V_{OL_10}	V_{IN} = 0V, pull PG up to 3.3V through a 10kΩ resistor @ 25°C		800	1000	mV
Thermal Protection						
Thermal shutdown [7]	T_{SD}			160		°C
Thermal shutdown hysteresis [7]				30		°C

NOTES:

6) Not tested in production, guaranteed by over-temperature correlation.

7) Guarantee by engineering sample characterization

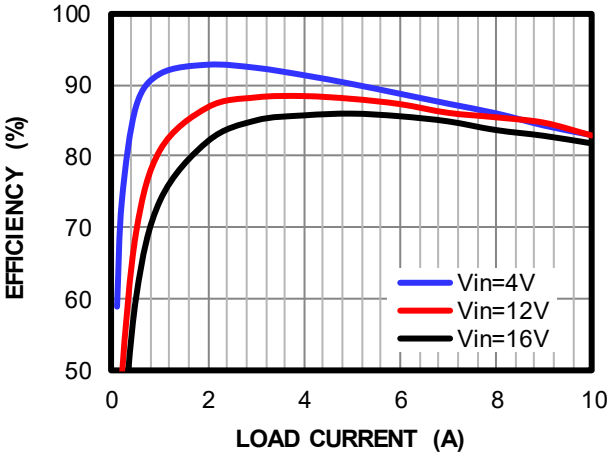
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, CCM = 1000kHz, T_A = 25°C, unless otherwise noted.

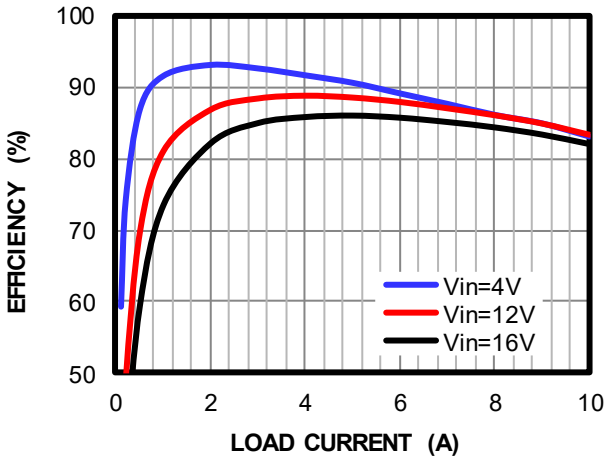
Efficiency

V_{IN} = 4V/12V/16V, V_{OUT} = 1V, I_{OUT} = 0-10A



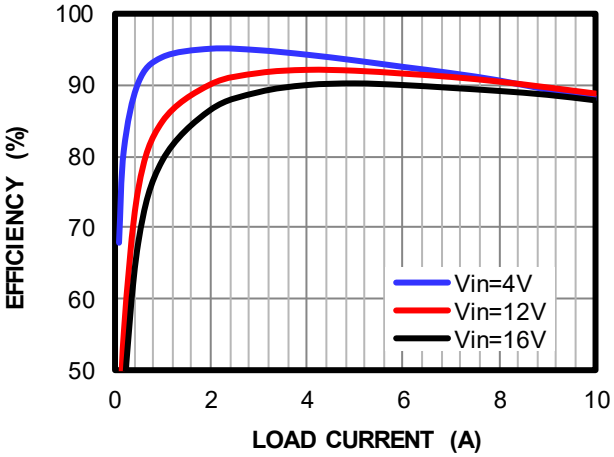
Efficiency

V_{IN} = 4V/12V/16V, V_{OUT} = 1.2V, I_{OUT} = 0-10A



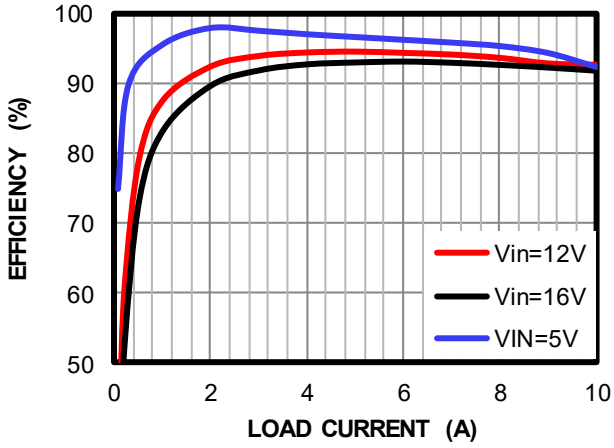
Efficiency

V_{IN} = 4V/12V/16V, V_{OUT} = 1.8V, I_{OUT} = 0-10A



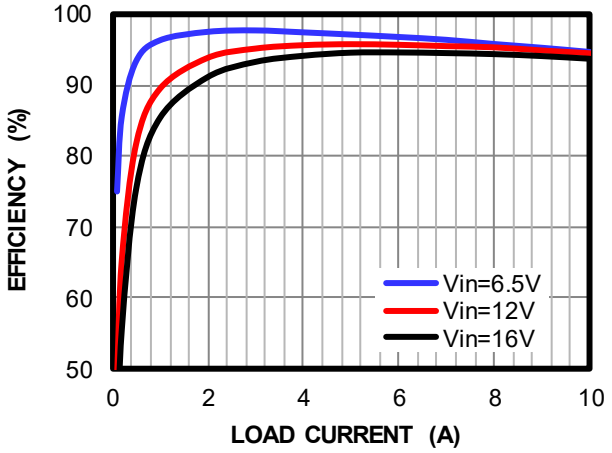
Efficiency

V_{IN} = 5V/12V/16V, V_{OUT} = 3.3V, I_{OUT} = 0-10A



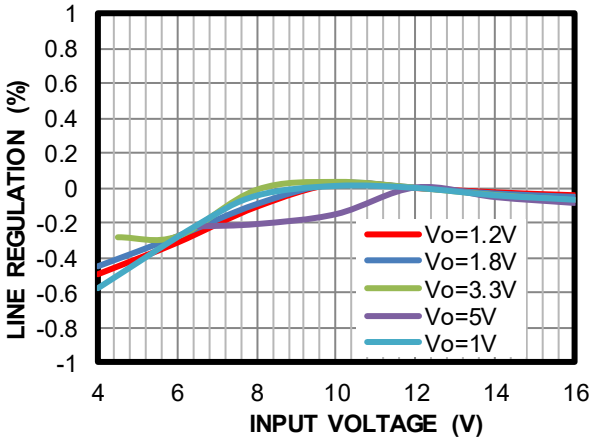
Efficiency

V_{IN} = 6.5V/12V/16V, V_{OUT} = 5V, I_{OUT} = 0-10A



Line Regulation

V_{OUT} = 1V/1.2V/1.8V/3.3V/5V, I_{OUT} = 10A



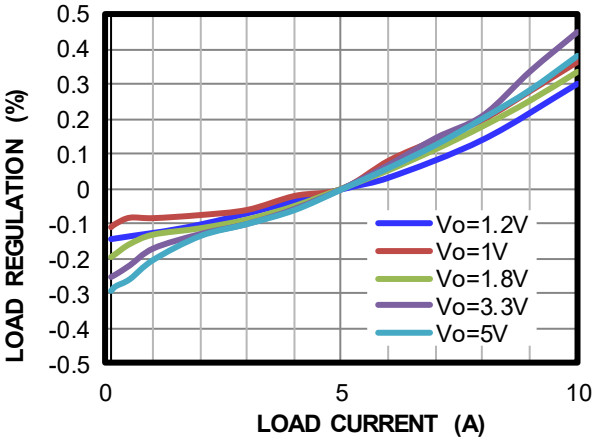
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, CCM=1000kHz, T_A = 25°C, unless otherwise noted.

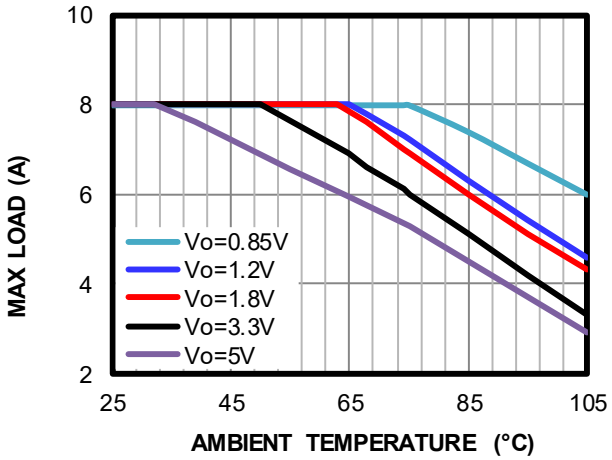
Load Regulation

V_{IN} = 12V, V_{OUT} = 1V/1.2V/1.8V/3.3V/5V, I_{OUT} = 0-10A



Thermal Derating

V_{IN} = 12V

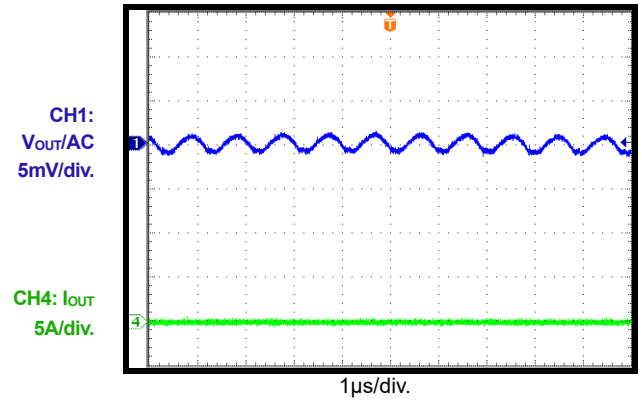


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

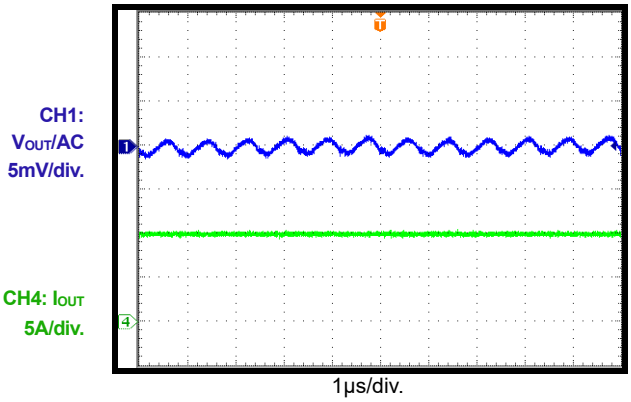
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, CCM=1000kHz, T_A = 25˚C, unless otherwise noted.

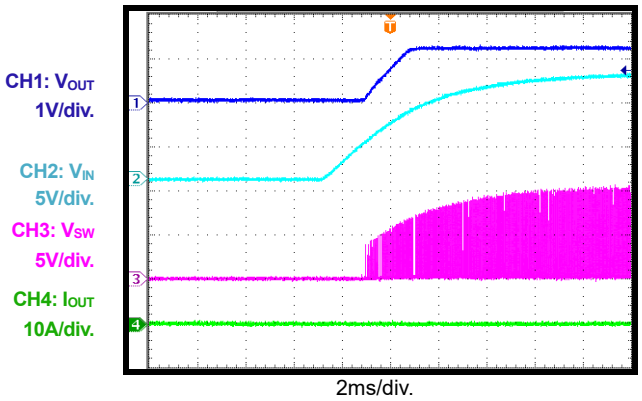
Vo Ripple
I_{OUT} = 0A



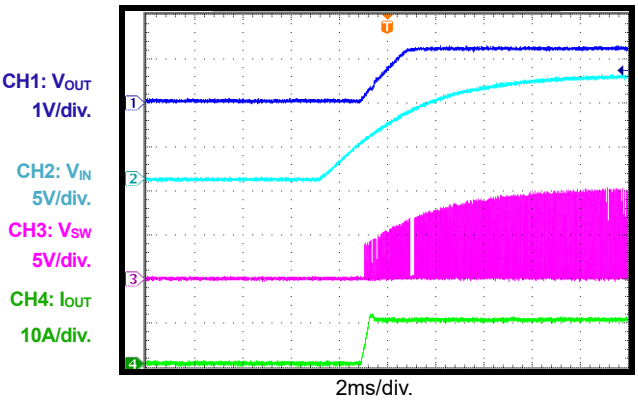
Vo Ripple
I_{OUT} = 10A



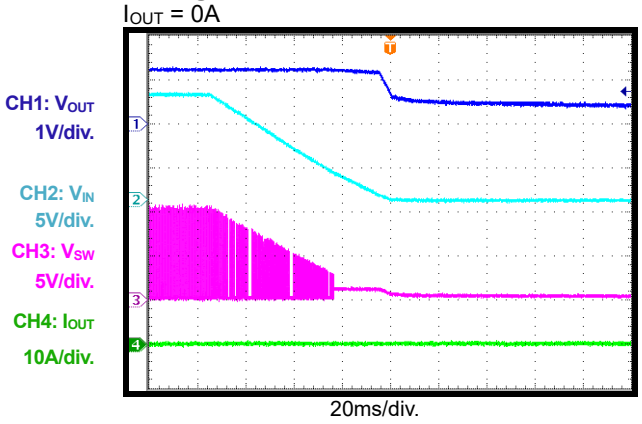
VIN Start-Up through Input Voltage
I_{OUT} = 0A



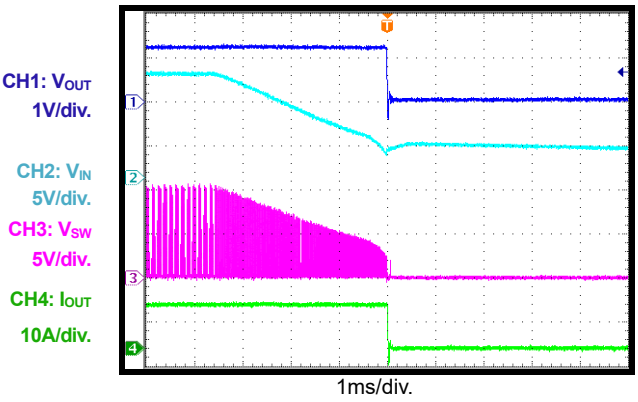
VIN Start-Up through Input Voltage
I_{OUT} = 10A



VIN Shutdown through Input Voltage
I_{OUT} = 0A



VIN Shutdown through Input Voltage
I_{OUT} = 10A

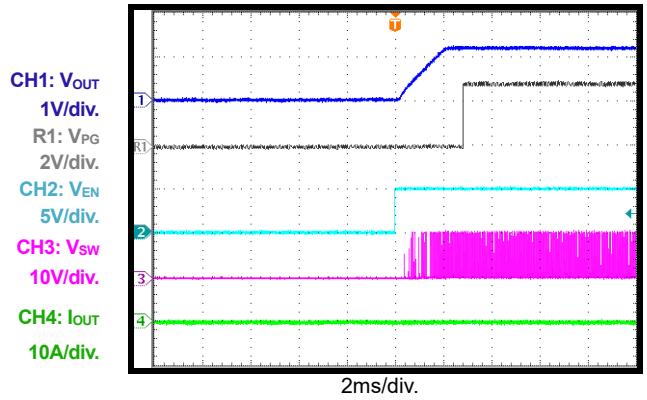


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

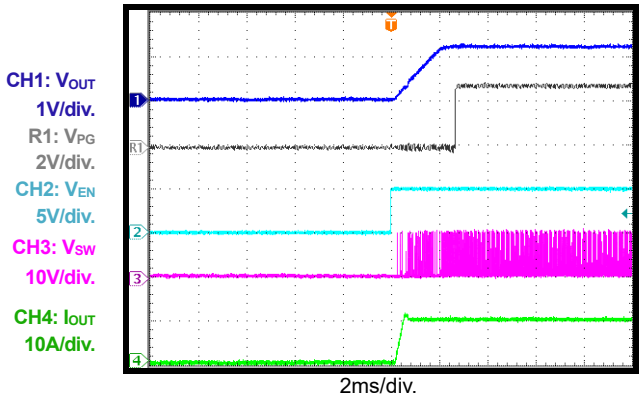
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, CCM=1000kHz, T_A = 25°C, unless otherwise noted.

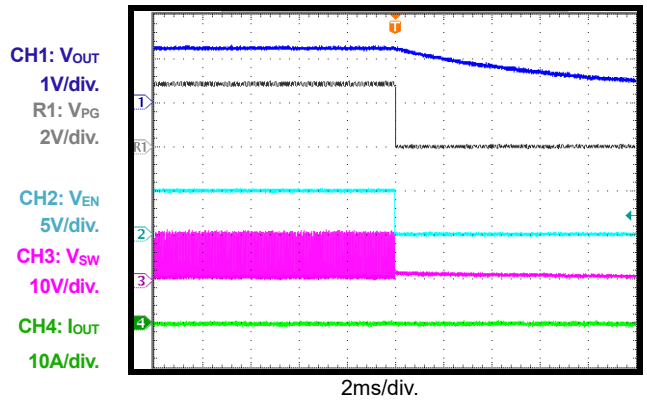
EN On
I_{OUT} = 0A



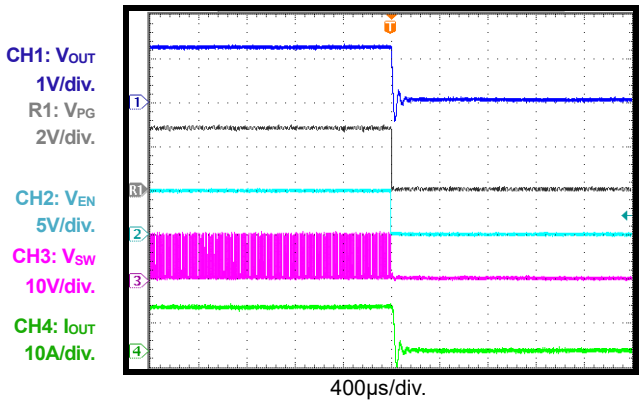
EN On
I_{OUT} = 10A



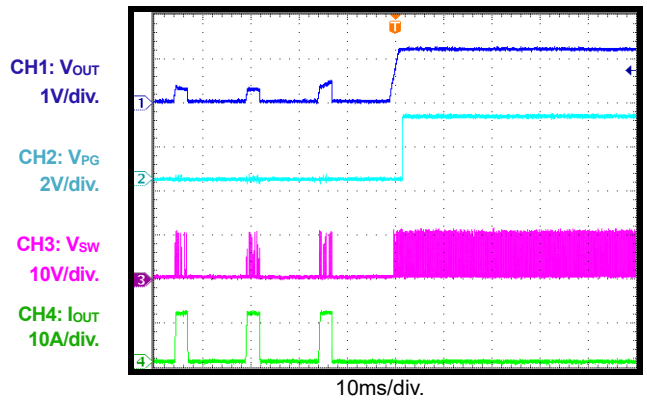
EN Off
I_{OUT} = 0A



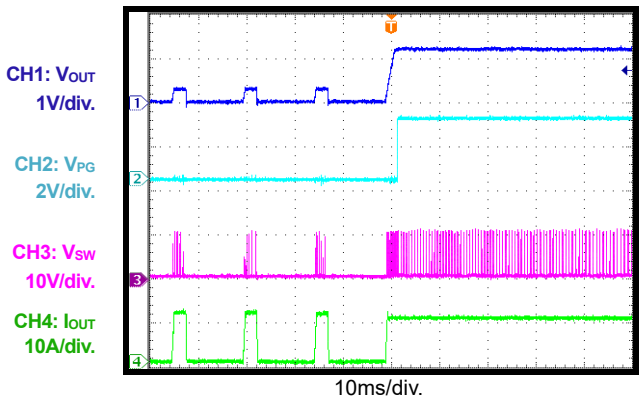
EN Off
I_{OUT} = 10A



SCP Recovery
I_{OUT} = 0A



SCP Recovery
I_{OUT} = 10A



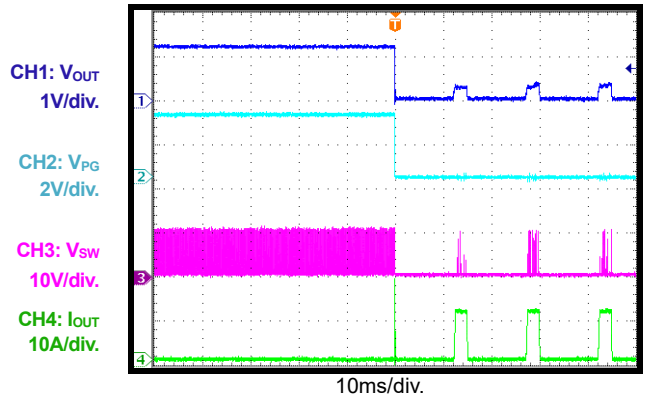
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, CCM=1000kHz, T_A = 25°C, unless otherwise noted.

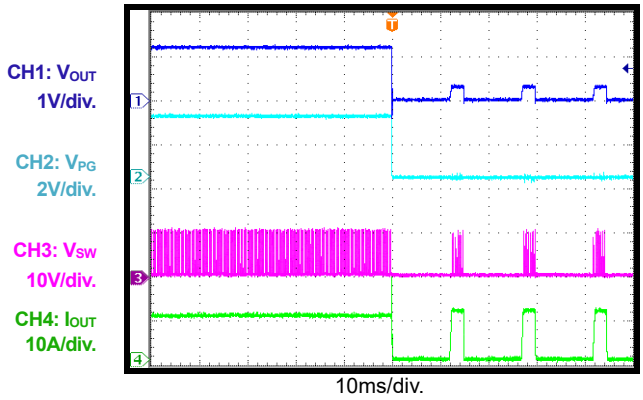
SCP Entry

I_{OUT} = 0A

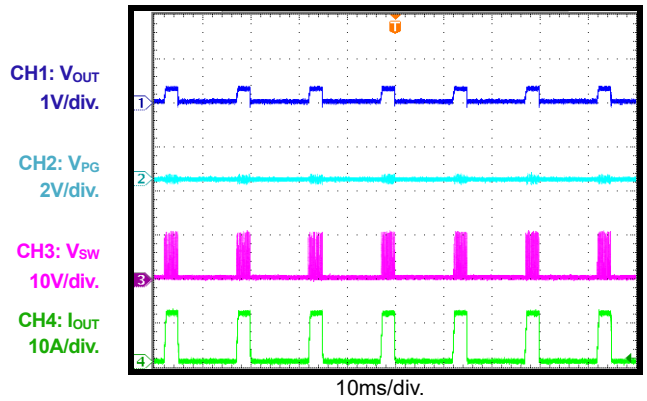


SCP Entry

I_{OUT} = 10A

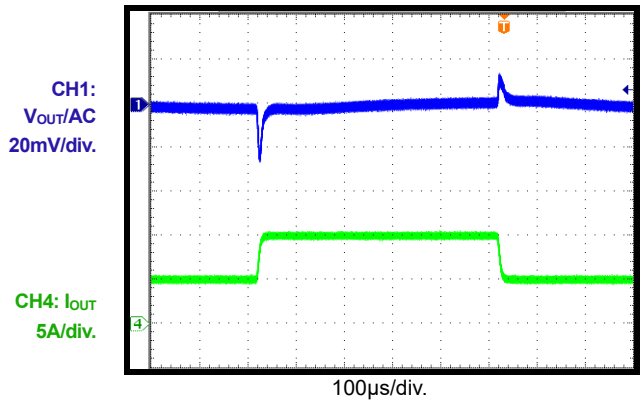


SCP Steady State



Load Transient

I_{OUT} = 5-10A,1A/µs

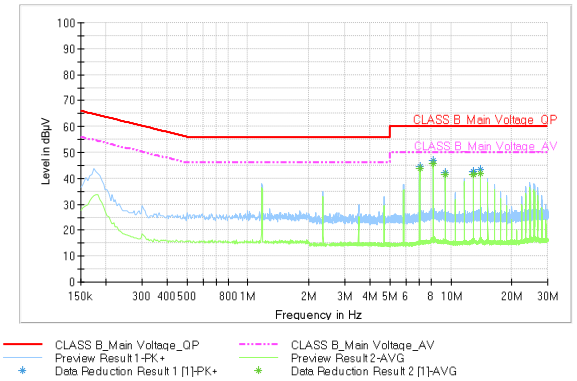


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

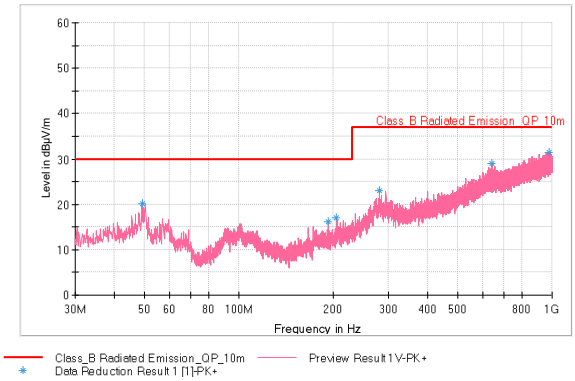
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, CCM=1000kHz, T_A = 25°C, unless otherwise noted.

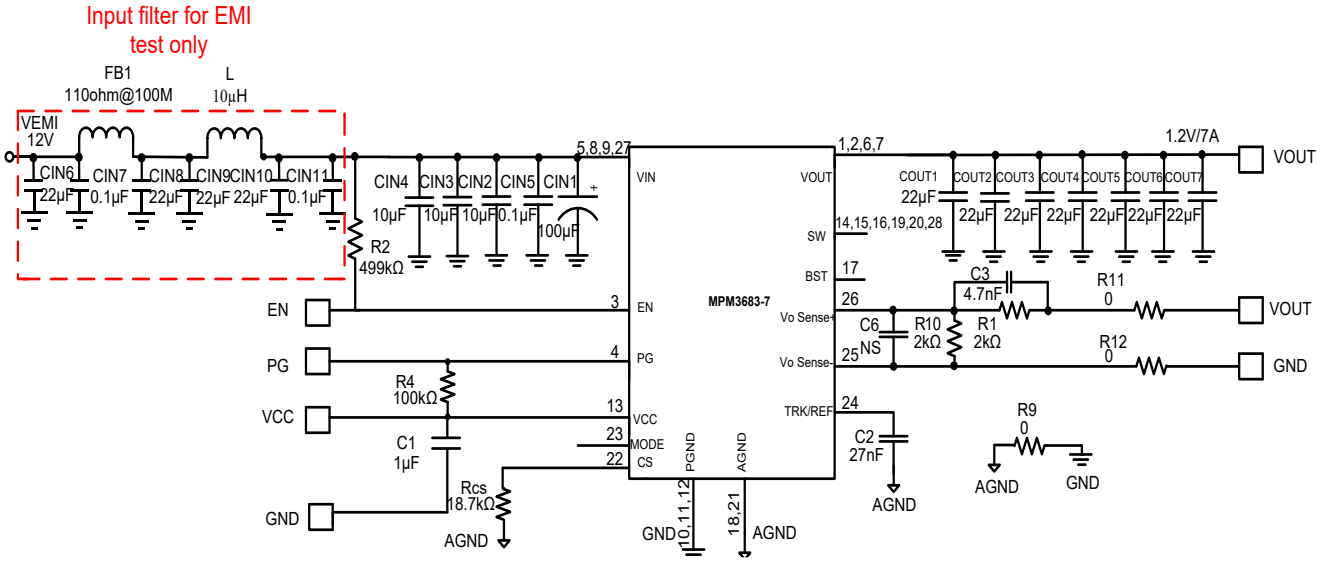
Conducted Emission, EN55022 Class B
Vout=1.2V,Io=7A,EMI tested with the input filter installed as shown in the EMI test circuit



Radiated Emission, EN55022 Class B
Vout=1.2V,Io=7A, EMI tested with the input filter installed as shown in the EMI test circuit



EMI Test Circuit:



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

BLOCK DIAGRAM

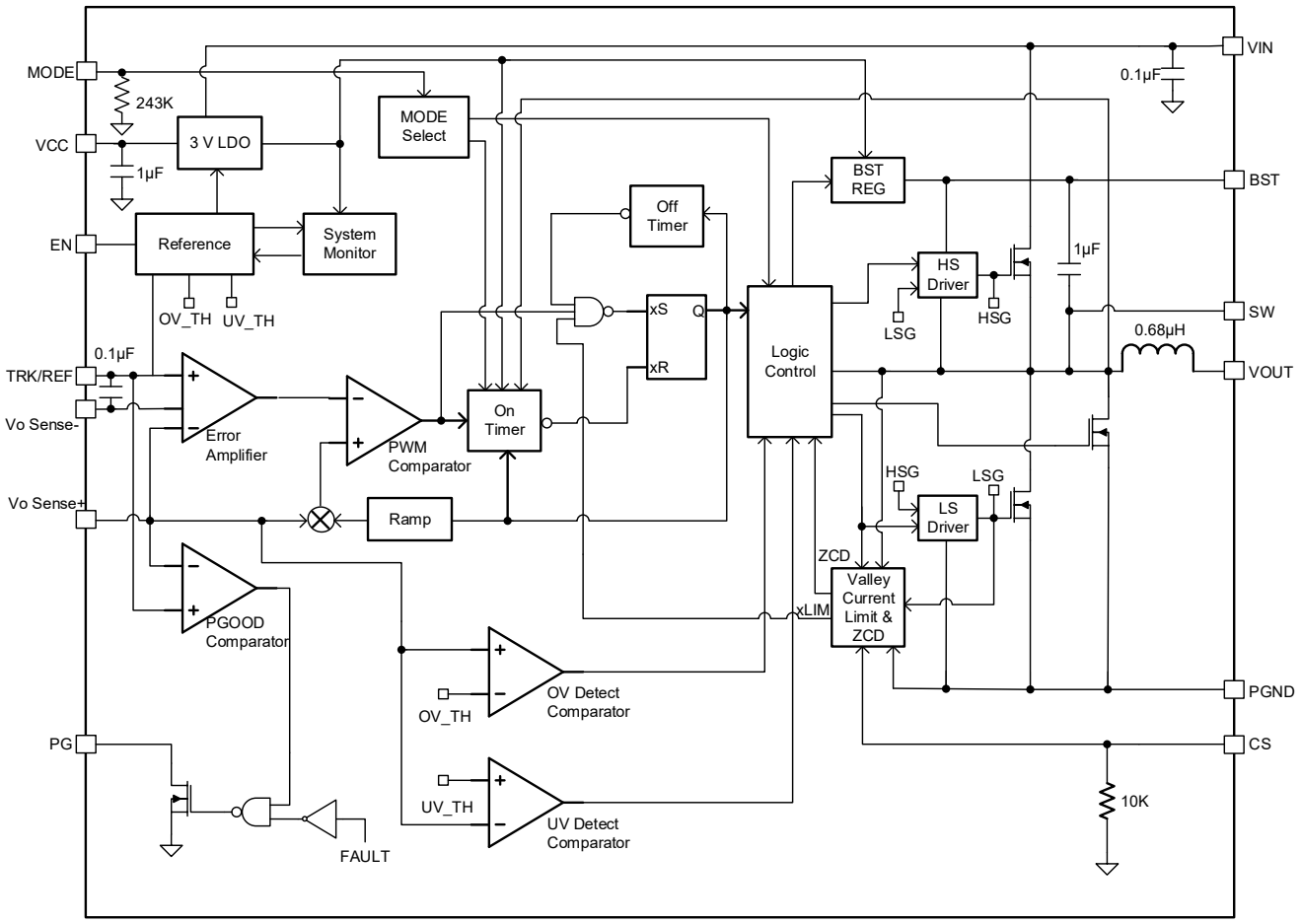


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

OPERATION

Constant-on-Time (COT) Control

The MPM3683-7 employs constant-on-time (COT) control to achieve a fast load transient response. Figure 2 details the control stage of the MPM3683-7.

The operational amplifier (AMP) corrects any error voltage between Vo Sense+ and V_{REF}. With the help of AMP, the MPM3683-7 can provide excellent load regulation over the entire load range, regardless of whether it is operating in forced continuous conduction mode (CCM) or pulse-skip mode.

The dedicated Vo Sense- pin helps to provide feedback remote GND sensing.

The MPM3683-7 uses internal ramp compensation to support low ESR MLCC output capacitor solutions. The adaptive, internal ramp is optimized so that the MPM3683-7 is stable in the entire operating input and output voltage ranges with a proper design of the output L/C filter.

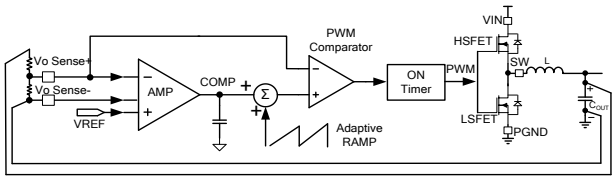


Figure 2: COT Control

Pulse-Width Modulation (PWM) Operation

Figure 3 shows how the pulse-width modulation (PWM) is generated. AMP corrects any error between Vo Sense+ and REF and generates a fairly smooth DC voltage (COMP). The internal ramp is superimposed onto COMP, and the superimposed COMP is compared with the Vo Sense+ signal. Whenever Vo Sense+ drops below the superimposed COMP, the integrated high-side MOSFET (HS-FET) turns on. The HS-FET remains on for a fixed on time determined by the input voltage, output voltage, and selected switching frequency. After the on period elapses, the HS-FET turns off and turns on again when Vo Sense+ drops below the superimposed COMP. By repeating this operation, the MPM3683-7 regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss. A dead short occurs between VIN and PGND if both the HS-FET and the LS-FET are turned on at the same time. This is called shoot through. To avoid shoot through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

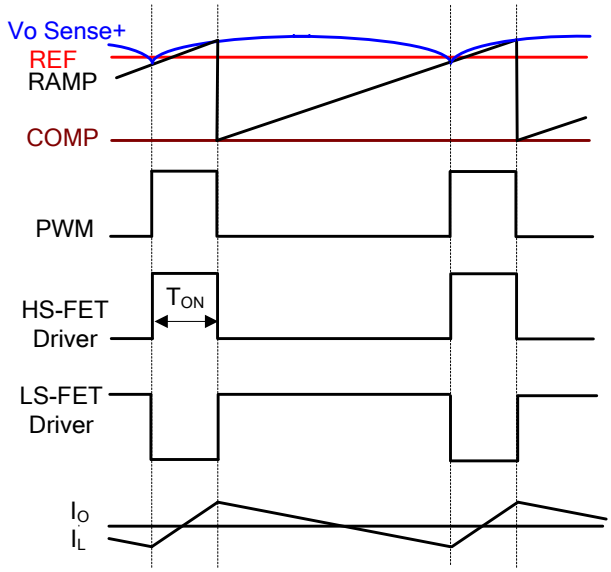


Figure 3: Heavy-Load Operation (PWM)

Continuous Conduction Mode (CCM) Operation

CCM occurs when the output current is high and the inductor current is always above zero amps. The MPM3683-7 can also be configured to operate in forced CCM operation when the output current is low (see the Mode Selection section on page 15 for details).

In CCM operation, the switching frequency is fairly constant (PWM mode), so the output ripple remains almost constant throughout the entire load range.

Pulse-Skip Operation

At light-load condition, the MPM3683-7 can be configured to work in pulse-skip mode to optimize the efficiency. When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the MPM3683-7 transitions from CCM to pulse-skip mode if it is configured to do so (see the Mode Selection section on page 15 for details).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

Figure 4 shows pulse-skip mode operation in light-load condition. When Vo Sense+ drops below the superimposed COMP, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until the inductor current reaches zero. In pulse-skip mode operation, Vo Sense+ will not reach the superimposed COMP while the inductor current is approaching zero. The LS-FET driver enters tri-state (Hi-Z) when the inductor current reaches zero. A current modulator takes over control of the LS-FET and limits the inductor current below -1mA. Therefore, the output capacitors discharge slowly to PGND through the LS-FET. In light-load condition, the HS-FET is not turned on as frequently in pulse-skip mode as it is in forced CCM. As a result, the efficiency in pulse-skip mode is improved greatly compared to that in forced CCM operation.

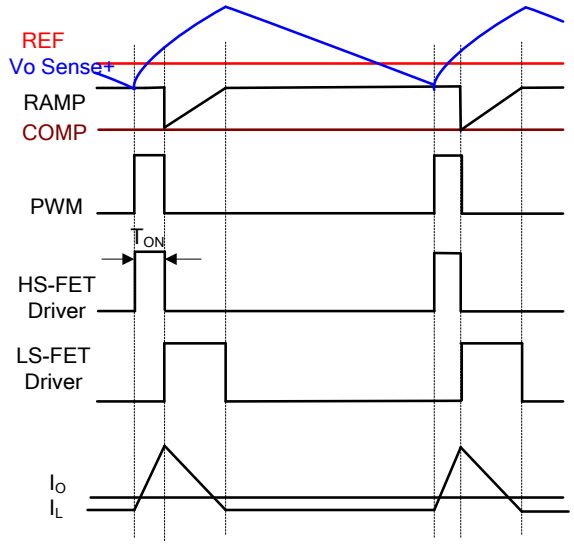


Figure 4: Pulse-Skip Mode at Light Load

As the output current increases from the light-load condition, the current modulator regulation time period becomes shorter, and the HS-FET is turned on more frequently. Therefore, the switching frequency increases accordingly. The output current reaches critical levels when the current modulator time is zero. The critical level of the output current is determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

Where F_{SW} represents the switching frequency, and L=0.68µH represents the inductance of the integrated inductor.

The MPM3683-7 enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

The MPM3683-7 can be configured to operate in forced CCM, even in a light-load condition (see Table 1).

Mode Selection

The MPM3683-7 provides both forced CCM operation and pulse-skip mode of operation under light-load condition. The MPM3683-7 has three options for switching frequency selection (600kHz, 800kHz, and 1000kHz). Select the operation mode under light-load condition and the switching frequency by choosing the value of the resistor connected between MODE and AGND or VCC (see Table 1).

Table 1: MODE Selection

MODE	Light-Load Mode	Switching Frequency
VCC	Pulse skip	600kHz
Float	Pulse skip	800kHz
243kΩ (±20%) to GND	Pulse skip	1000kHz
GND	Forced CCM	600kHz
34.8kΩ (±20%) to GND	Forced CCM	800kHz
80.6kΩ (±20%) to GND	Forced CCM	1000kHz

Soft Start (SS)

With the integrated 100nF soft-start capacitor, the minimum soft-start time is limited to 1.6ms. This time can be increased by adding an external capacitor between TRK/REF and AGND.

The value of the soft-starting capacitor C_{SS} is determined by:

$$C_{SS}(nF) = \frac{t_{ss}(ms) \times 36\mu A}{0.6(V)} - 100nF \quad (2)$$

Output Voltage Tracking and Reference

The MPM3683-7 provides an analog input pin (TRK/REF) to track another power supply or accept an external reference. When an external

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

voltage signal is connected to TRK/REF, it acts as a reference for the MPM3683-7 output voltage. The Vo Sense+ voltage follows this external voltage signal exactly, and the soft-start settings are ignored. The TRK/REF input signal can be in the range of 0.3V to 1.4V. During the initial start-up, the TRK/REF must first reach 600mV or above to ensure proper operation. Afterward, it can be any value between 0.3V and 1.4V.

Pre-Bias Start-Up

The MPM3683-7 has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the TRK/REF pin exceeds the sensed output voltage at Vo Sense+ pin. Before the TRK/REF voltage reaches the pre-biased Vo Sense+ level, if the BST voltage (from BST to SW) is lower than 2.3V, the LS-FET is turned on to allow the BST voltage to be charged through VCC. The LS-FET is turned on for very narrow pulses, so the drop-in pre-biased level is negligible.

Output Voltage Discharge

When the MPM3683-7 is disabled through EN, output voltage discharge mode is enabled. This causes both the HS-FET and the LS-FET to latch off. A discharge MOSFET connected between SW and PGND is turned on to discharge the output voltage. The typical switch on resistance of this MOSFET is about 80Ω. Once the Vo Sense+ voltage drops below 10%*REF, the discharge MOSFET is turned off.

Current Sense and Over-Current Protection (OCP)

The MPM3683-7 features on-die current sensing and programmable over-current protection threshold for the inductor valley current.

The over-current protection is active when MPM3683-7 is enabled. During the LS-FET on state, the inductor current is sensed and mirrored to CS pin with the ratio of G_{CS}. By connecting a resistor (R_{CS}) between the CS and AGND pins, a V_{CS} voltage is generated which is proportional to the inductor current cycle-by-cycle. The HS-FET is allowed to turn on only when the V_{CS} voltage is below the internal over-current protection voltage threshold (V_{OCP}) (during the LS-FET on state) to limit the inductor valley current cycle-by-cycle. The MPM3683-7 integrates an 10kΩ current sensing resistor in between CS and AGND pins.

The over-current protection threshold of the inductor valley current is determined by:

$$I_{Valley} = \frac{[R_{CS}(M\Omega) + 0.01] \times V_{OCP}}{R_{CS}(M\Omega) \times 0.01 \times G_{CS}} \quad (3)$$

Calculate the value of the external current sensing resistor R_{CS} for the desired output current limit I_{LIM} by the following equation:

$$\frac{R_{CS}(M\Omega) \times 0.01}{R_{CS}(M\Omega) + 0.01} = \frac{V_{OCP}}{G_{CS} \times (I_{LIM} - \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{2 \times L(\mu H) \times f_s(MHz)})} \quad (4)$$

Where V_{OCP}=1.2V, G_{CS}=20μA/A, L=0.68μH, and I_{LIM} is the desired output current limit (A).

It should be noted that the MPM3683-7 provides accurate cycle-by-cycle over-current protection for the inductor valley current. However, the conversion between the inductor valley current and the output current may involve error introduced by the tolerance of the integrated inductor and switching frequency variation due to the COT operation. The values for R_{CS} selection is shown in Table 2 for typical applications.

Table 2: R_{CS} **Values for Typical Applications**

Conditions	R_{CS}	Switching Frequency
V_{IN}=12V,V_{OUT}=5V ,I_{LIM}=8A	249K	1000kHz
V_{IN}=12V,V_{OUT}=3.3 V,I_{LIM}=8A	78.7KΩ	1000kHz
V_{IN}=12V,V_{OUT}=1.8 V,I_{LIM}=10A	16.2KΩ	1000kHz
V_{IN}=12V,V_{OUT}=1.2 V,I_{LIM}=10A	16KΩ	1000kHz
V_{IN}=12V,V_{OUT}=1V ,I_{LIM}=10A	15KΩ	1000kHz

OCP hiccup is active 3ms after the MPM3683-7 is enabled. Once OCP hiccup is active, if the MPM3683-7 detects an over-current condition for 31 consecutive cycles or if the Vo Sense+

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

drops below the under-voltage protection (UVP) threshold, the device enters hiccup mode. In hiccup mode, the MPM3683-7 latches off the HS-FET immediately and latches off the LS-FET after zero-current detection (ZCD) is detected. Meanwhile, the TRK/REF capacitor is discharged as well. After about 11ms, the MPM3683-7 attempts to soft start automatically. If the over-current condition still remains after 3ms, the MPM3683-7 repeats this operation cycle until the over-current condition is removed and the output voltage rises back to the regulation level smoothly.

Negative Inductor Current Limit

When the LS-FET detects a -9A (typical) current, the MPM3683-7 turns off the LS-FET for 200ns to limit the negative current.

Output-Sinking Mode (OSM)

The MPM3683-7 employs output-sinking mode (OSM) to regulate the output voltage to the targeted value. When the Vo Sense+ voltage is higher than 104%*REF but lower than the OVP threshold, OSM is triggered. During OSM operation, the LS-FET remains on until it reaches the -5.5A negative current limit. Afterward, the LS-FET is turned off momentarily (200ns) before turning on again. The MPM3683-7 repeats this operation until the Vo Sense+ drops below 102%*REF. Afterward, the MPM3683-7 exits OSM after 15 consecutive cycles of forced CCM.

Over-Voltage Protection (OVP)

The MPM3683-7 monitors the output voltage by connecting Vo Sense+ to the tap of the output voltage feedback resistor divider to detect an over-voltage condition. This provides hiccup over-voltage protection (OVP) mode.

If the Vo Sense+ voltage exceeds 116% of the REF voltage, OVP is triggered. PG is pulled down until it reaches the low-side negative current limit (NOCP). Then the LS-FET is turned off momentarily for 200ns. The HS-FET is turned on during this period. After 200ns, the LS-FET is turned on again. The MPM3683-7 repeats this operation to discharge any over-voltage on the output. The MPM3683-7 exits OVP discharge mode when the feedback voltage drops below 105%*REF.

Over-Temperature Protection (OTP)

The MPM3683-7 has an over-temperature protection (OTP). The MPM3683-7 monitors the junction temperature internally. If the junction temperature exceeds the threshold value (typically 160°C), the converter shuts off and discharges the TRK/REF capacitors. OTP is a non-latch protection. There is a hysteresis of about 30°C. Once the junction temperature drops to about 130°C, a soft start is initiated.

The OTP function is effective once the MPM3683-7 is enabled.

Power Good (PG)

The MPM3683-7 has a power good (PG) output. PG is the open drain of a MOSFET. Connect PG to VCC or another external voltage source (less than 3.6V) through a pull-up resistor (typically 10kΩ). After applying the input voltage, the MOSFET turns on, so PG is pulled to GND before TRK/REF is ready. After the Vo Sense+ voltage reaches 92.5% of the REF voltage, PG is pulled high after a 0.9ms delay.

When the Vo Sense+ voltage drops to 80% of the REF voltage or exceeds 116% of the nominal REF voltage, PG is latched low. PG can only be pulled high again after a new soft start.

If the input supply fails to power the MPM3683-7, PG is clamped low, even though PG is tied to an external DC source through a pull-up resistor. The relationship between the PG voltage and the pull-up current is shown in Figure 5.

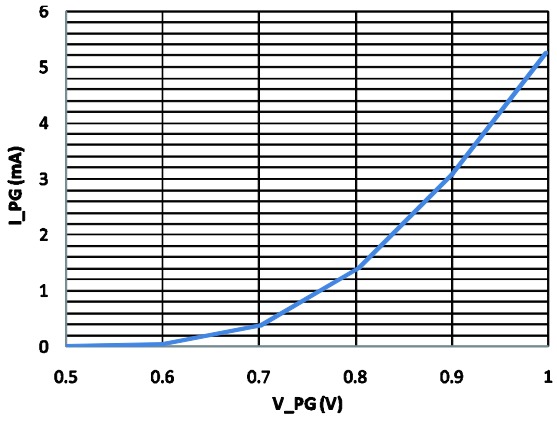


Figure 5: PG Clamped Voltage vs. Pull-Up Current

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

EN Configuration

The MPM3683-7 turns on when EN goes high. The MPM3683-7 turns off when EN goes low. EN cannot be left floating for proper operation. EN can be driven by an analog or digital control logic signal to enable or disable the MPM3683-7.

The MPM3683-7 provides accurate EN thresholds, so a resistor divider from VIN to AGND can be used to program the input voltage at which the MPM3683-7 is enabled.

This is highly recommended for applications where there is no dedicated EN control logic signal to avoid possible under-voltage lockout (UVLO) bouncing during power-up and power-down. The resistor divider values can be determined by Equation (5):

$$V_{IN_START}(V) = VIH_{EN} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (5)$$

Where VIH_{EN} is 1.22V, typically.

R_{UP} and R_{DOWN} should be chosen so that the EN voltage does not exceed 3.6V when VIN reaches the maximum value.

EN can also be connected to VIN directly through a pull-up resistor (R_{UP}). R_{UP} should be chosen so that the maximum current going into EN is 50μA. An easy calculation of R_{UP} is given in Equation (6):

$$R_{UP}(K\Omega) = \frac{VIN_{MAX}(V)}{0.05(mA)} \quad (6)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage

The circuit connection is shown in Figure 6.

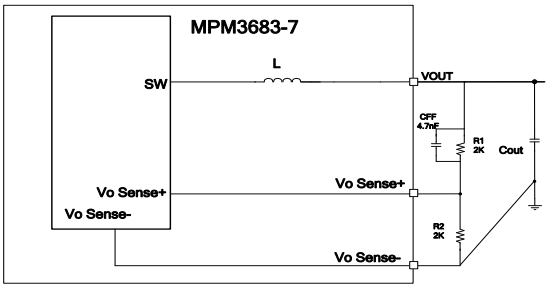


Figure 6: Circuit Connection

R2 can be determined with Equation (7):

$$R_2(k\Omega) = \frac{V_{REF}}{V_O - V_{REF}} \times R_1(k\Omega) \quad (7)$$

Table 3 lists the recommended resistor values for common output voltages.

Table 3: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R2 (kΩ)
1.0	3
1.2	2
1.8	1
3.3	0.442
5	0.272

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During the layout, place the input capacitors as close to VIN as possible.

The capacitance can vary significantly with the temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over a wide temperature range and offer very low ESR.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (8):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (8)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (9):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (9)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half of the maximum load current. The input capacitor value determines the converter input voltage ripple. If there is an input voltage ripple requirement in the system, select an input capacitor that meets the specification.

Estimate the input voltage ripple with Equation (10):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (11):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (11)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use POSCAP or ceramic capacitors. Estimate the output voltage ripple with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (12)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

The ESR dominates the switching frequency impedance for the POSCAP capacitors. For simplification, the output ripple can be approximated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (14)$$

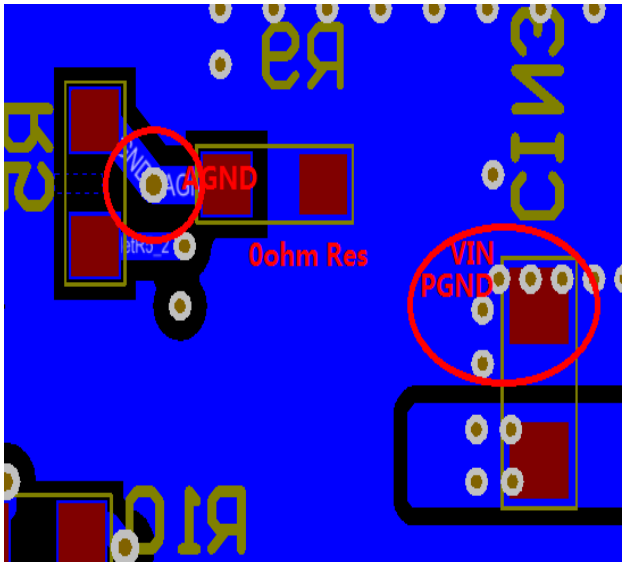
Where L is fixed at 0.68µH internally.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 6 and follow the guidelines below.

1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible.
2. Place the major MLCC capacitors on the same layer as the MPM3683-7.
3. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
4. Ensure that the high-current paths (PGND, IN, and OUT) have short, direct, and wide traces.
5. Place the ceramic input capacitor close to IN and PGND.
6. Keep the input capacitor and the IN connection as short and wide as possible.
7. Place as many PGND vias as possible as close to PGND as possible to minimize both the parasitic impedance and thermal resistance.
8. Place the external feedback resistors next to Vo Sense+.
9. Keep the feedback network away from the switching node.



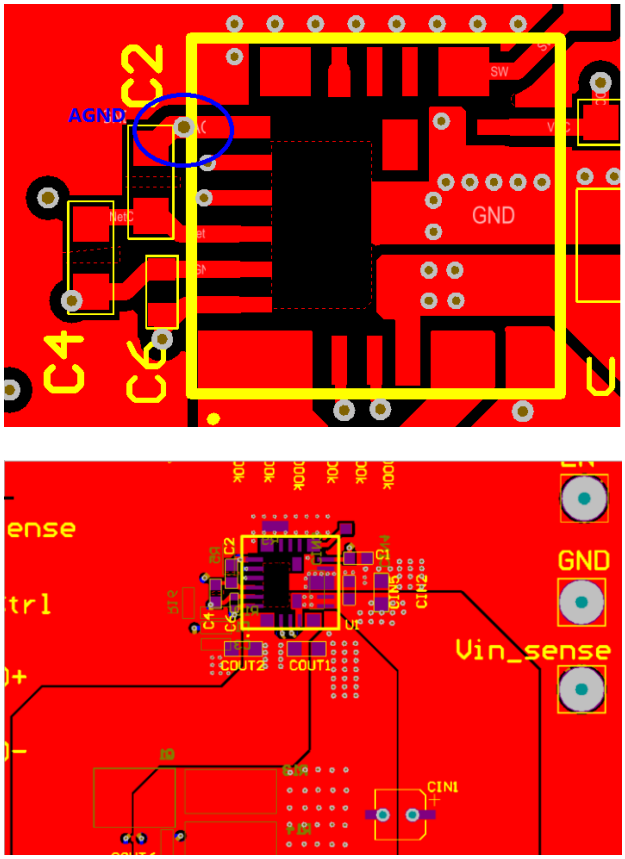


Figure 7: Recommended Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

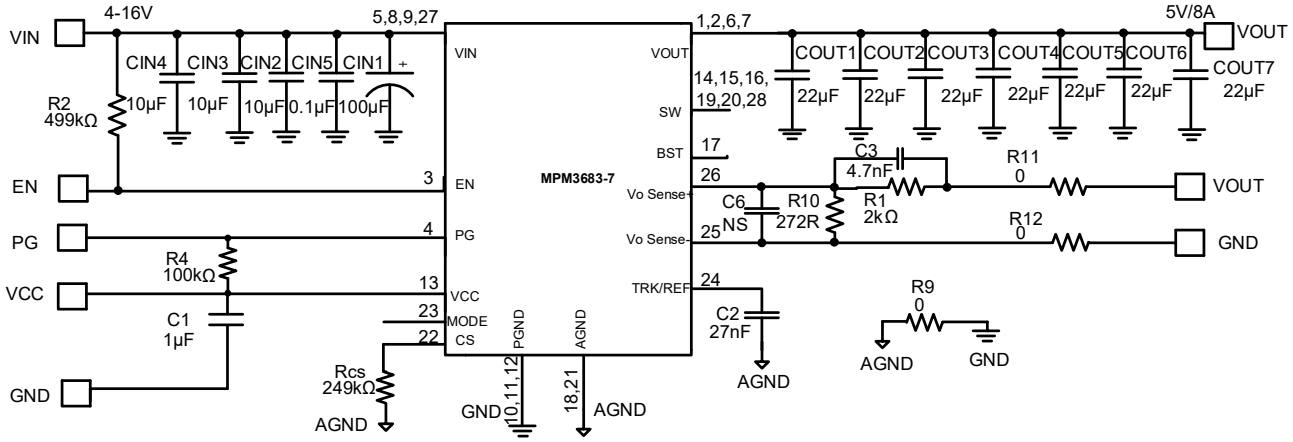


Figure 8: 12V$_{IN}$ 5V/8A Output, CCM1000KHz

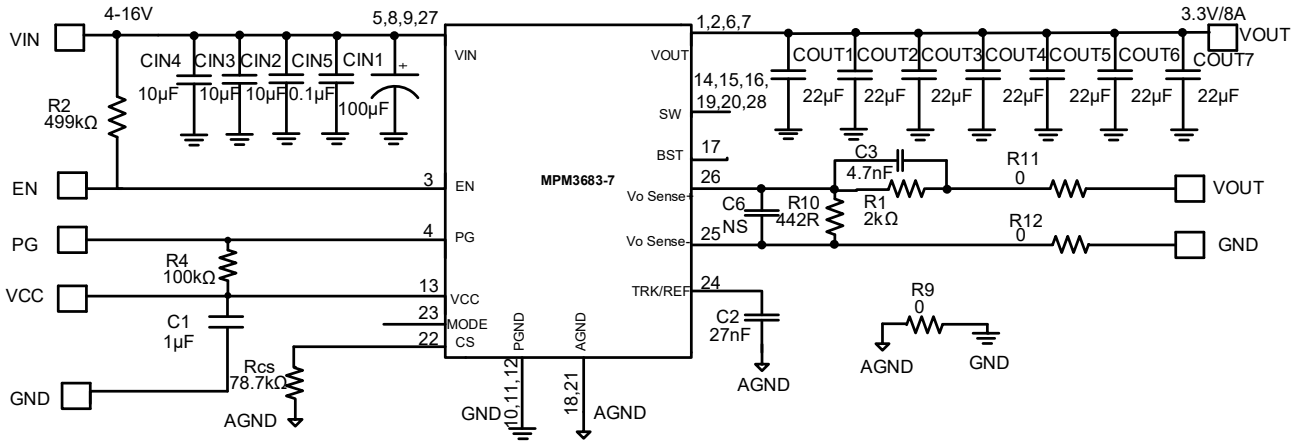


Figure 9: 12V$_{IN}$ 3.3V/8A Output, CCM1000KHz

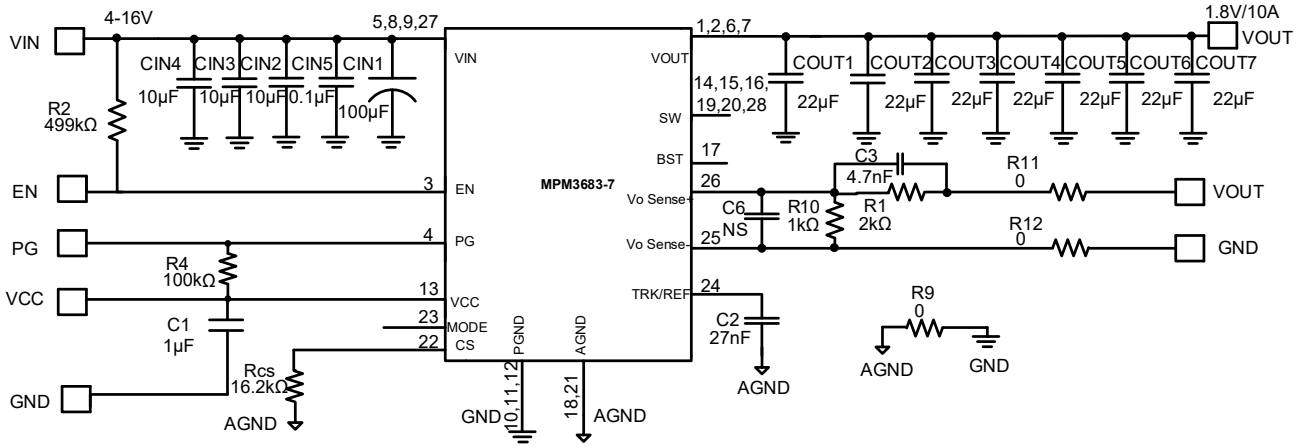


Figure 10: 12V$_{IN}$ 1.8V/10A Output, CCM1000KHz

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

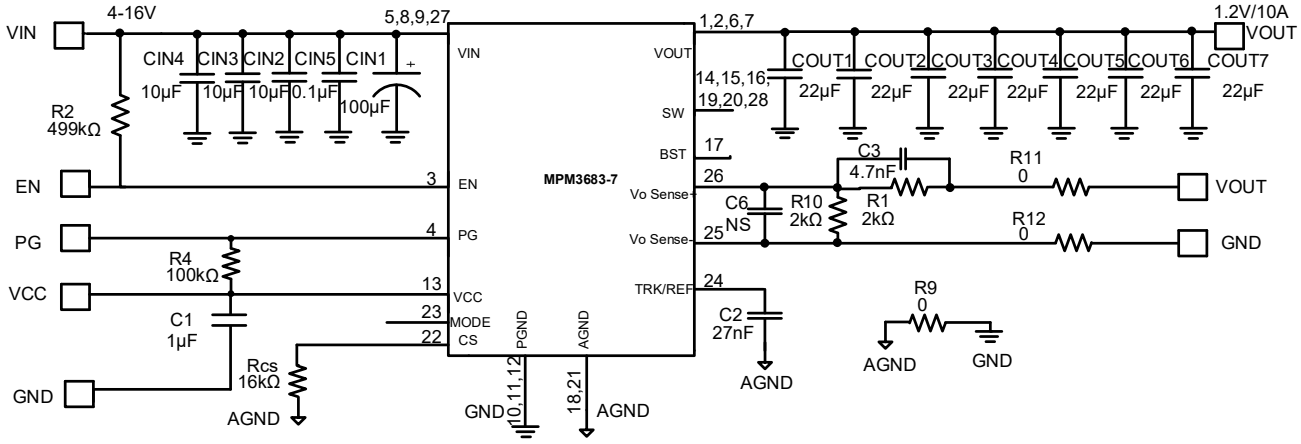


Figure 11: 12V$_{IN}$ 1.2V/10A Output, CCM1000KHz

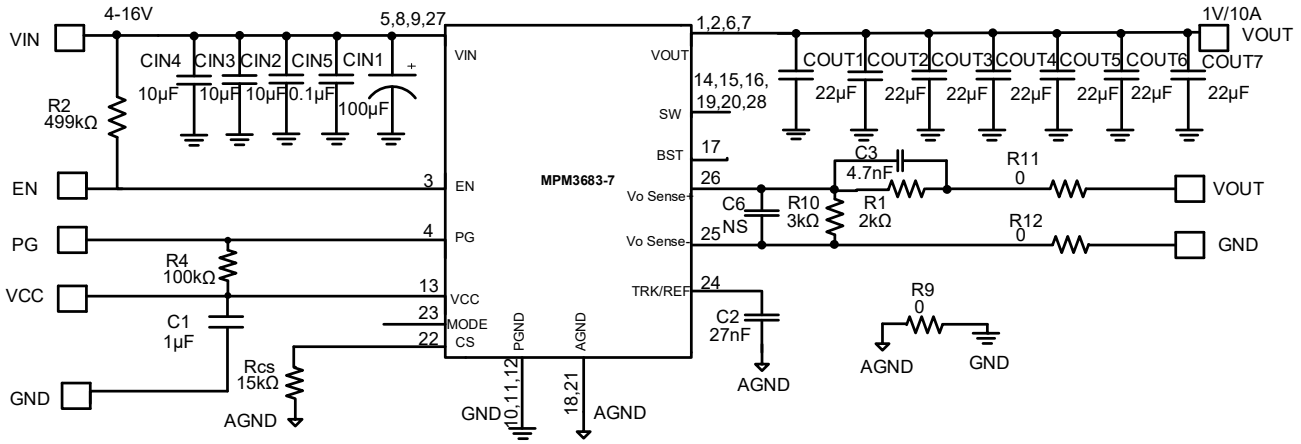
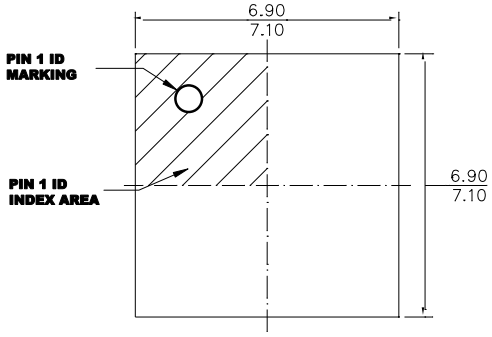


Figure 12: 12V$_{IN}$ 1V/10A Output, CCM1000KHz

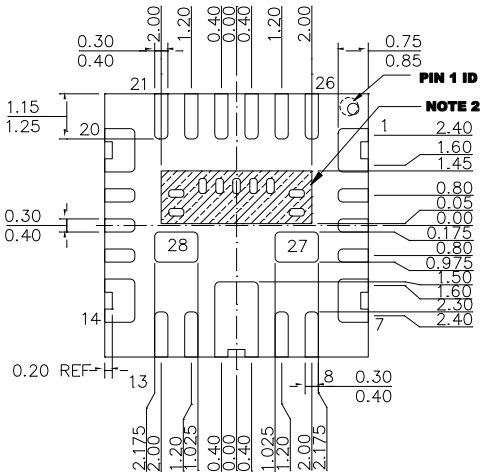
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PACKAGE INFORMATION

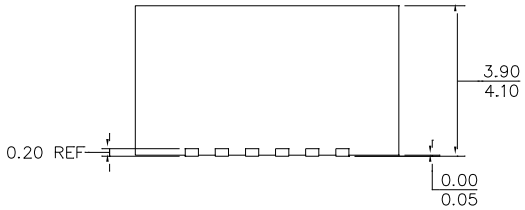
QFN-28 (7mmx7mmx4mm)



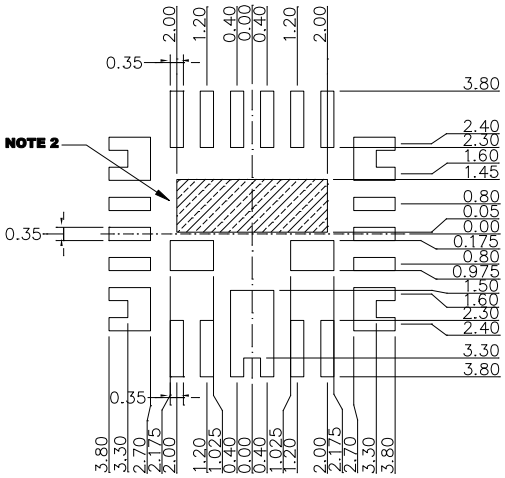
TOP VIEW



BOTTOM VIEW



SIDE VIEW



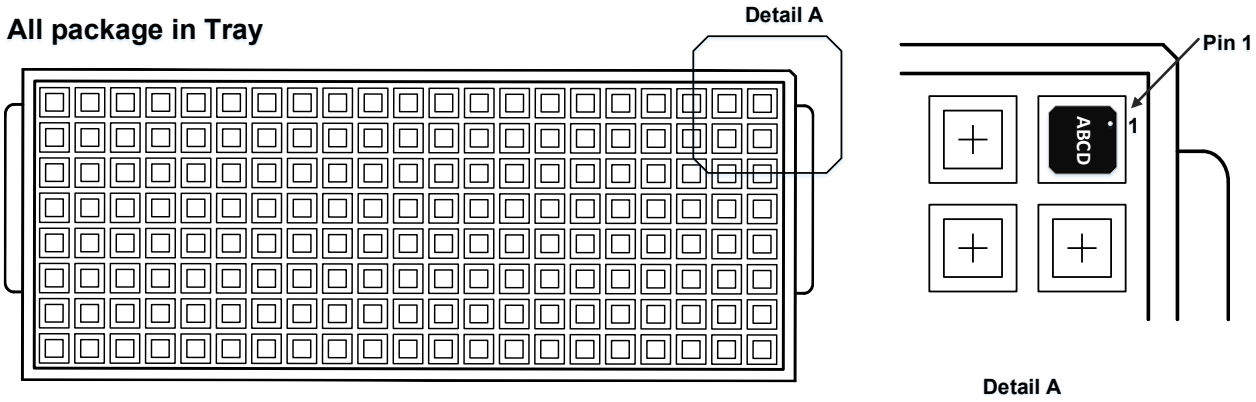
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

CARRIER INFORMATION



Note:

This is a schematic diagram of Tray. Different packages correspond to different trays with different length, width and height

Part Number	Package Description	Quantity/Reel	Quantity/Tube	Quantity/Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3683GQN-7	QFN 7x7x 4	N/A	N/A	416	N/A	N/A	N/A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

Revision History

Revision #	Revision Date	Description	Pages Updated
1.01	6/2/2020	update Thermal Derating curve;	page9
		Add EMI circuit;	page13
		Remove the TRK/REF pin to VOSNS- pin capacitor;	page23.24
		Add Table 2 to descript the Rcs and current limit relationship;	page17
		PCB Layout Guideline modified;	page22
		Add note for EN of ABS list:	page5
		Modified the Block Diagram to add the values for internal components;	page14
		Add MSL information to ORDERING INFORMATION	Page3
		Add CARRIER INFORMATION in the last page	page25

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.