MPQ2459

0.5A, 55V, 480KHz, Step-Down Converter in a TSOT23-6 Package AEC-Q100 Qualified

The Future of Analog IC Technology

DESCRIPTION

The MPQ2459 is a monolithic, step-down, switch-mode converter with a built-in power MOSFET. It achieves a 0.5A peak output current over a wide input-supply range with excellent load and line regulation. Current mode operation provides a fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MPQ2459 requires a minimal number of readily-available, standard, external components. The MPQ2459 is available in a TSOT23-6 package.

FEATURES

- Guaranteed Industrial/Automotive Temp Range Limits.
- 0.5A Peak Output Current
- 1Ω Internal Power MOSFET
- Stable with Low-ESR Ceramic Output Capacitors
- Up to 90% Efficiency
- 0.1μA Shutdown Mode
- Fixed 480kHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over-Current Protection
- Wide 4.5V-to-55V Input Operating Range
- Output Adjustable from 0.81V to 0.95×VIN
- Available in a TSOT23-6 Package
- Available in AEC-Q100 Grade 1

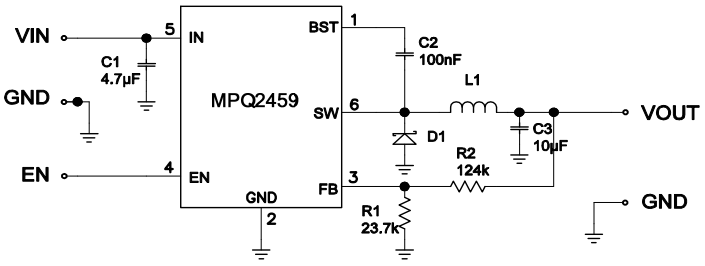
APPLICATIONS

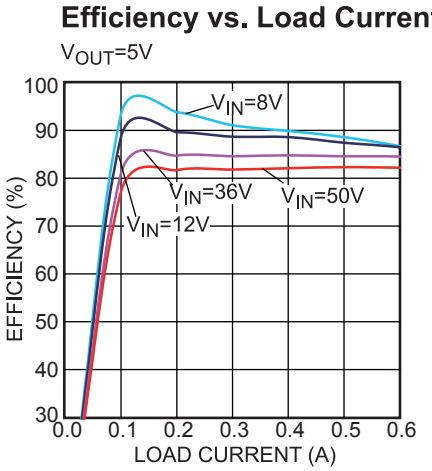
- Power Meters
- Distributed Power Systems
- Battery Chargers
- Pre-Regulators for Linear Regulators
- WLED Drivers

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION





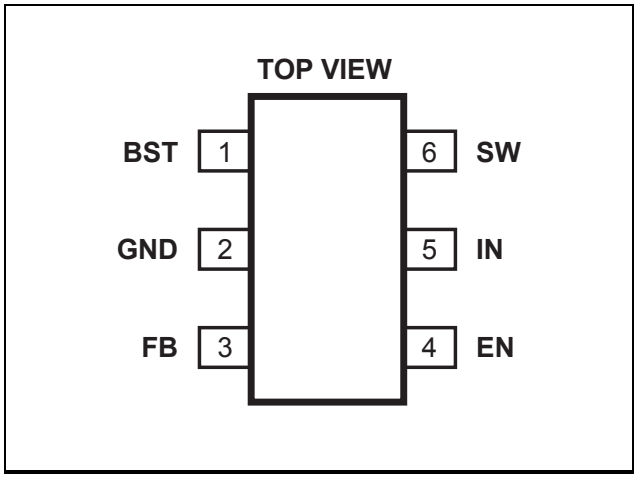
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ2459GJ*	TSOT23-6	AEQ
MPQ2459GJ-AEC1**	TSOT23-6	AEQ

* For Tape & Reel, add suffix –Z (eg. MPQ2459GJ–Z);
** For Tape & Reel, add suffix -Z (e.g. MPQ2459GJ-AEC1-Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} ..... −0.3V to 60V
V_{SW} ..... −0.3V to V_{IN}+0.3V
V_{BS} ..... V_{SW} + 6V
All Other Pins ..... −0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
TSOT23-6 ..... 0.568W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... −65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.5V to 55V
Output Voltage V_{OUT} ..... 0.81V to 0.95×V_{IN}
Operating Junction Temp. ..... −40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}
TSOT23-6	220	110 °C/W

Notes:

1) Absolute maximum are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device function is not guaranteed outside of the recommended operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = −40°C to +125°C, unless otherwise noted. Typical values are at T_J=25°C.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}		0.796	0.812	0.828	V
		T_J=25°C	0.800	0.812	0.824	V
Feedback Current	I_{FB}	V_{FB} = 0.85V			0.1	µA
Switch-ON Resistance	$R_{DS(ON)}$			1	2	Ω
Switch Leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 0V			1	µA
Current Limit	I_{LIM}	T_J=25°C	1	1.25	1.5	A
			0.9	1.25	1.6	
Oscillator Frequency	f_{SW}	V_{FB} = 0.6V	360	480	600	kHz
Foldback Frequency	f_{SW_F}	V_{FB} = 0V		150		kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.6V	90	93.5		%
Minimum ON Time (5)	τ_{ON}			100		ns
Under-Voltage-Lockout Threshold, Rising	V_{UVLO_R}		2.9	3.3	3.7	V
Under-Voltage-Lockout Threshold, Falling	V_{UVLO_F}		2.65	3.05	3.45	V
Under-Voltage-Lockout Threshold, Hysteresis	V_{UVLO_HYS}			250		mV
EN Threshold Rising	V_{EN_R}		1.1	1.35	1.6	V
EN Threshold Falling	V_{EN_F}		0.9	1.17	1.3	V
EN Input Hysteresis	V_{EN_HYS}			180		mV
EN Input Current	I_{EN}	V_{EN} = 2V		3.1	5	µA
		V_{EN} = 0V		0.1	1	
Supply Current, Shutdown	I_S	V_{EN} = 0V		0.1	1.0	µA
Supply Current, Quiescent	I_Q	V_{EN} = 2V, V_{FB} = 1V		0.73	0.92	mA
Thermal Shutdown (5)	T_{SD}			165		°C
Thermal Shutdown Hysteresis(5)	T_{SD_HYS}			20		°C

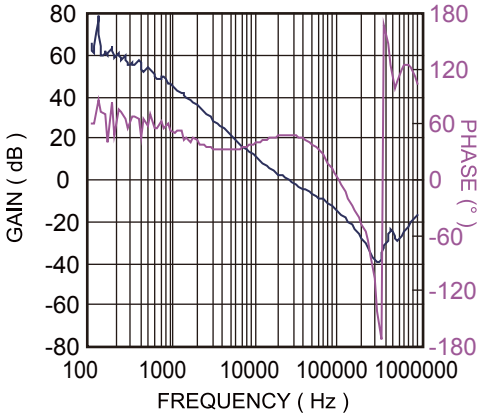
Notes:
5) Guaranteed by design.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

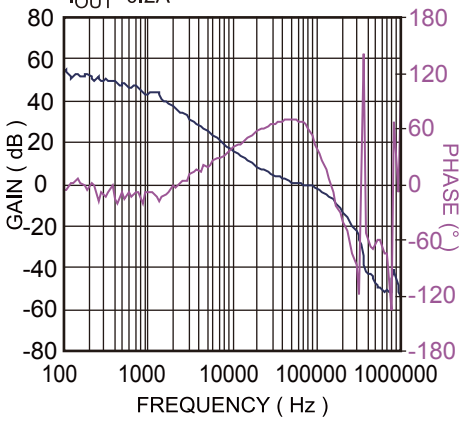
TYPICAL CHARACTERISTICS

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.5A, L=15µH, T_A=25°C, unless otherwise noted.

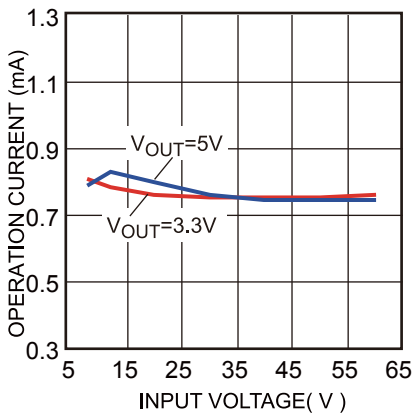
Bandwidth
I_{OUT}=0.8A



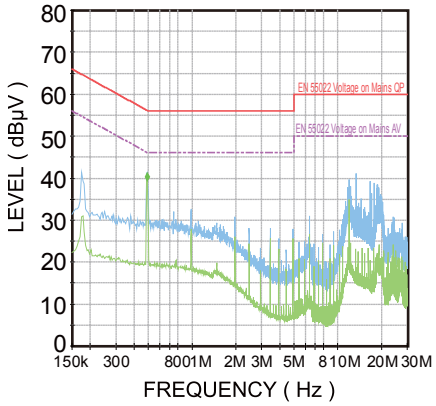
Bandwidth
V_{OUT}=3.3V,
I_{OUT}=0.2A



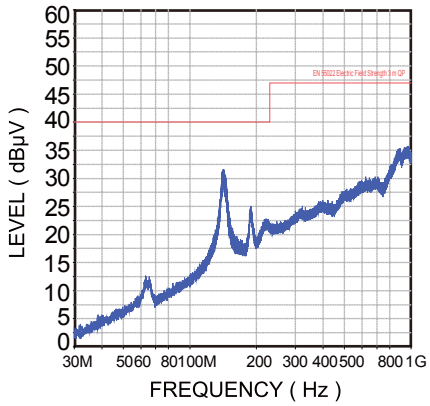
Operation Current
I_{OUT}=0A



Conduction EMI



Radiation EMI

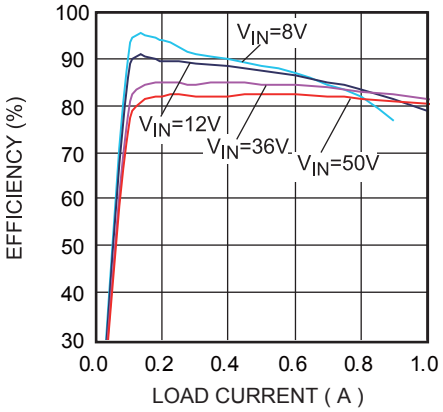


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

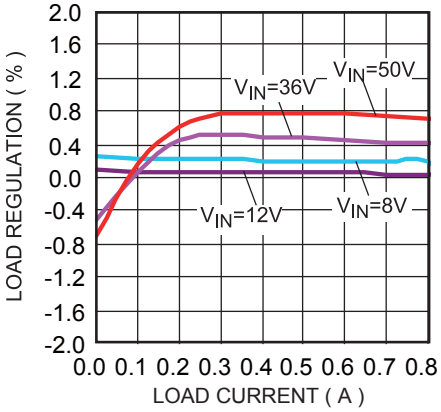
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT}=5V, L=22µH, T_A=25°C, unless otherwise noted.

Efficiency vs. Load

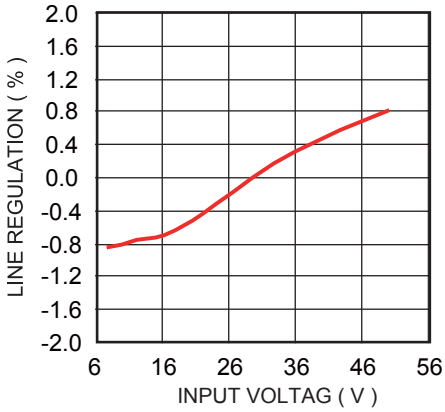


Load Regulation



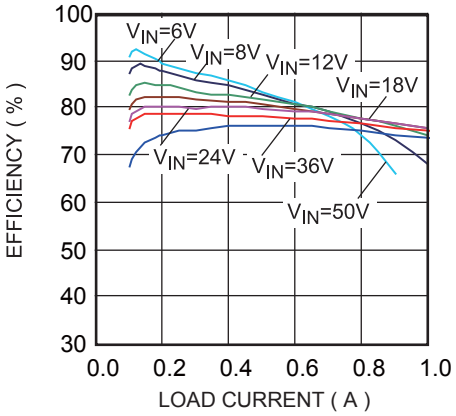
Line Regulation

I_{OUT}=0.5A



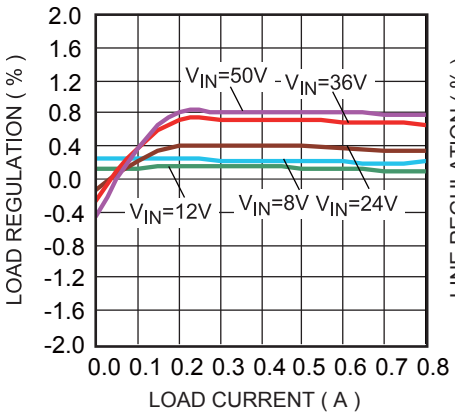
Efficiency vs. Load

V_{OUT}=3.3V



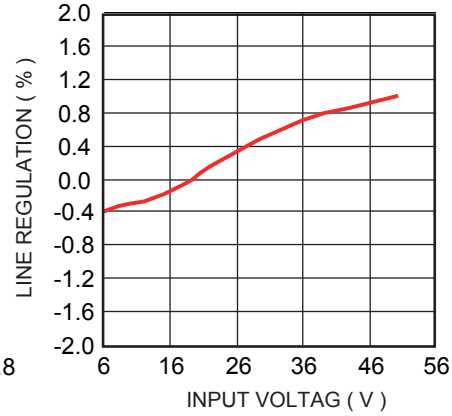
Load Regulation

V_{OUT}=3.3V

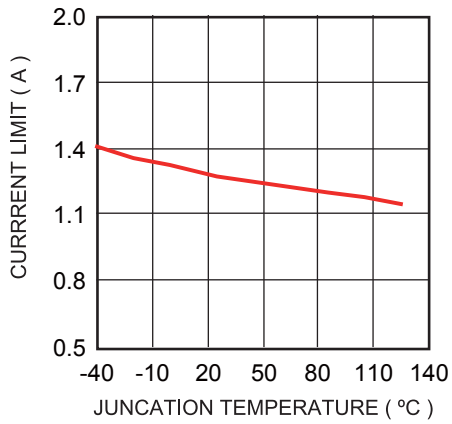


Line Regulation

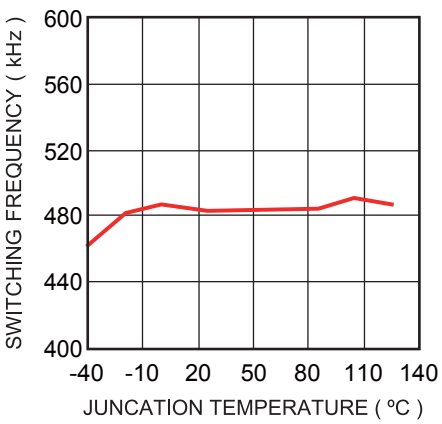
V_{OUT}=3.3V, I_{OUT}=0.5A



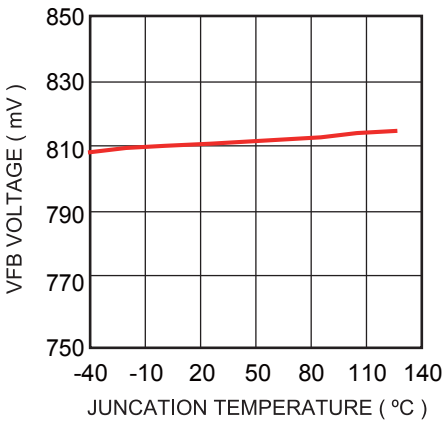
Current Limit vs. T_J



Frequency vs. T_J



Feedback Voltage vs. T_J

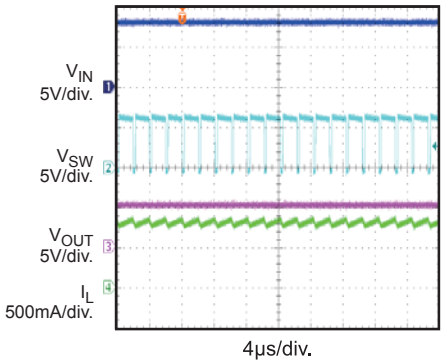


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

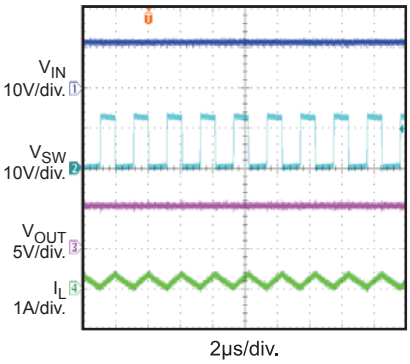
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT}=5V, L=22µH, T_A=25°C, unless otherwise noted.

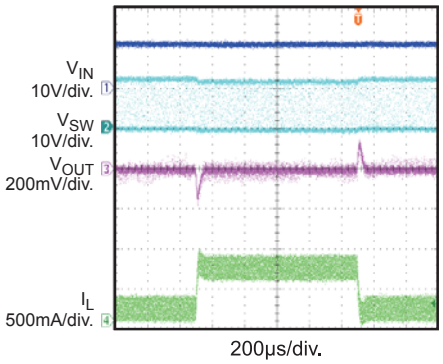
Steady State
V_{IN}=8V, I_{OUT}=0.8A



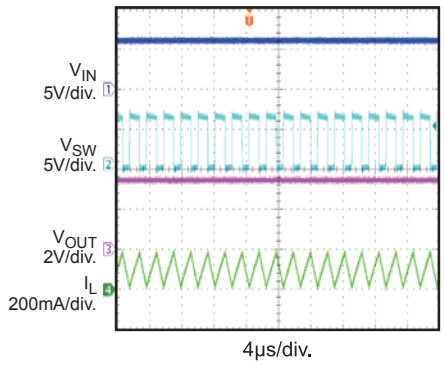
Steady State
I_{OUT}=0.15A



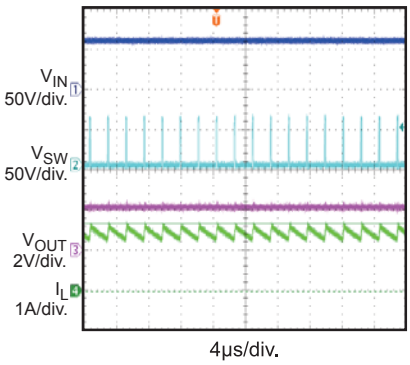
Load Transient
I_{OUT}=0.2A to 0.7A



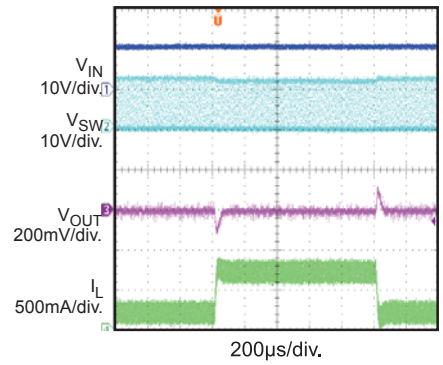
Steady State
V_{IN}=6V, V_{OUT}=3.3V, I_{OUT}=0.1A



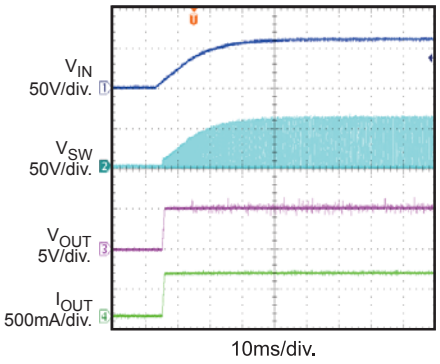
Steady State
V_{IN}=60V, V_{OUT}=3.3V, I_{OUT}=0.9A



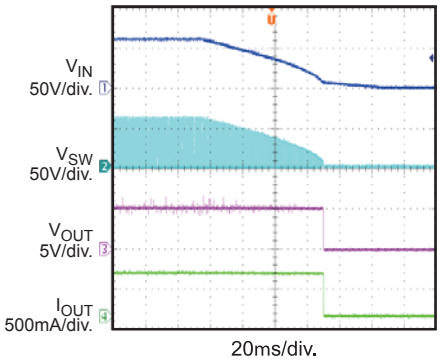
Load Transient
V_{OUT}=3.3V, I_{OUT}=0.2A to 0.7A



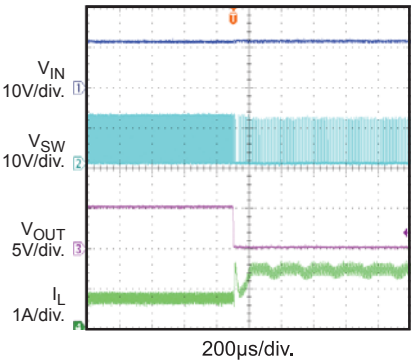
Power Ramp Up
V_{IN}=60V, I_{OUT}=0.5A



Power Ramp Down
V_{IN}=60V, I_{OUT}=0.5A



Short Output
I_{OUT}=0.65A



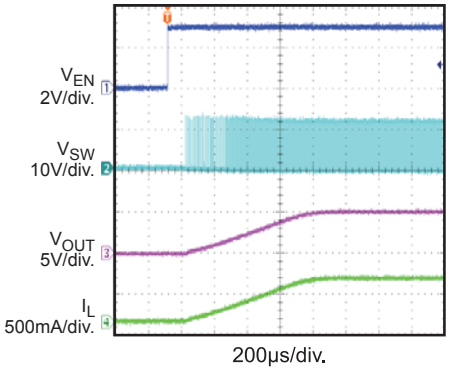
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT}=5V, L=22µH, T_A=25°C, unless otherwise noted.

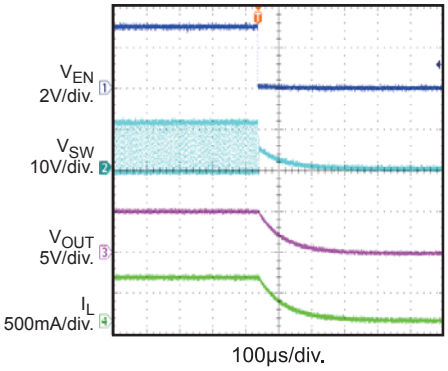
Enable On

I_{OUT}=0.5A



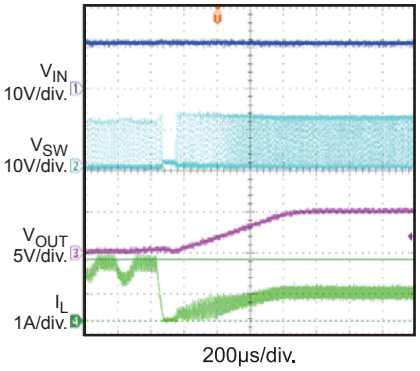
Enable Off

I_{OUT}=0.5A



Short Output Recovery

I_{OUT}=0.65A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	BST	Bootstrap. Connect a capacitor between SW and BST to form a floating supply across the power-switch driver. This capacitor drives the power switch's gate above the supply voltage.
2	GND	Ground. Voltage reference for the regulated, output voltage. Requires special layout considerations. Place this node outside of the D1-to-C1 ground path to prevent current-switching spikes from introducing voltage noise.
3	FB	Feedback. Sets the output voltage through an external resistor divider from the output to GND. To prevent current-limit runaway during a short-circuit fault, the frequency foldback comparator lowers the oscillator frequency when V_{FB} is below 250mV.
4	EN	ON/OFF Control. Pull EN above 1.2V to turn the device ON. For automatic enable, connect a 100kΩ resistor between this pin and IN.
5	IN	Supply Voltage. The MPQ2459 operates from a 4.5V-to-55V unregulated input. Requires C1 to prevent large voltage spikes from appearing at the input.
6	SW	Switch Output.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

OPERATION

The MPQ2459 is a current-mode buck regulator — the EA output voltage is proportional to the peak-inductor current.

At the beginning of a cycle, M1 is OFF. The EA output voltage exceeds the current-sense-amplifier output, and the current comparator's output is LOW. The rising edge of the 480kHz CLK signal sets the RS flip-flop. The flip-flip's output turns on M1 to connect the SW pin and inductor to the input supply.

The current-sense amplifier senses and amplifies the rising inductor current. The PWM comparator takes the sum of the current-sense amplifier's output and the ramp compensator and the error amplifier output as its inputs. When the sum of the current sense amplifier's output and the ramp-compensation signal exceeds the EA output voltage, the RS flip-flop resets and M1 turns OFF. The external Schottky rectifier diode (D1) conducts the inductor current.

If the sum of the current sense amplifier's output and the slope compensation signal does not exceed the EA output for a whole cycle, then the falling edge of the CLK resets the flip-flop.

The EA output integrates the voltage difference between the feedback and the 0.81V bandgap reference. When V_{FB}<0.81V, the EA output voltage increases. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage also increases current delivered to the output.

Enable Control

The MPQ2459 has a dedicated enable contro pin EN. With high enough VIN, the chip can be enabled and disabled by EN pin.

Internally a zener diode is connected from EN pin to GND pin. The typical clamping voltage of the zener diode is 7.5V. So VIN can be connected to EN though a high ohm resistor, if the system doesn't have another logic input acting as enable signal. The resistor needs to be designed to limit the EN pin sink current less than 100μA.

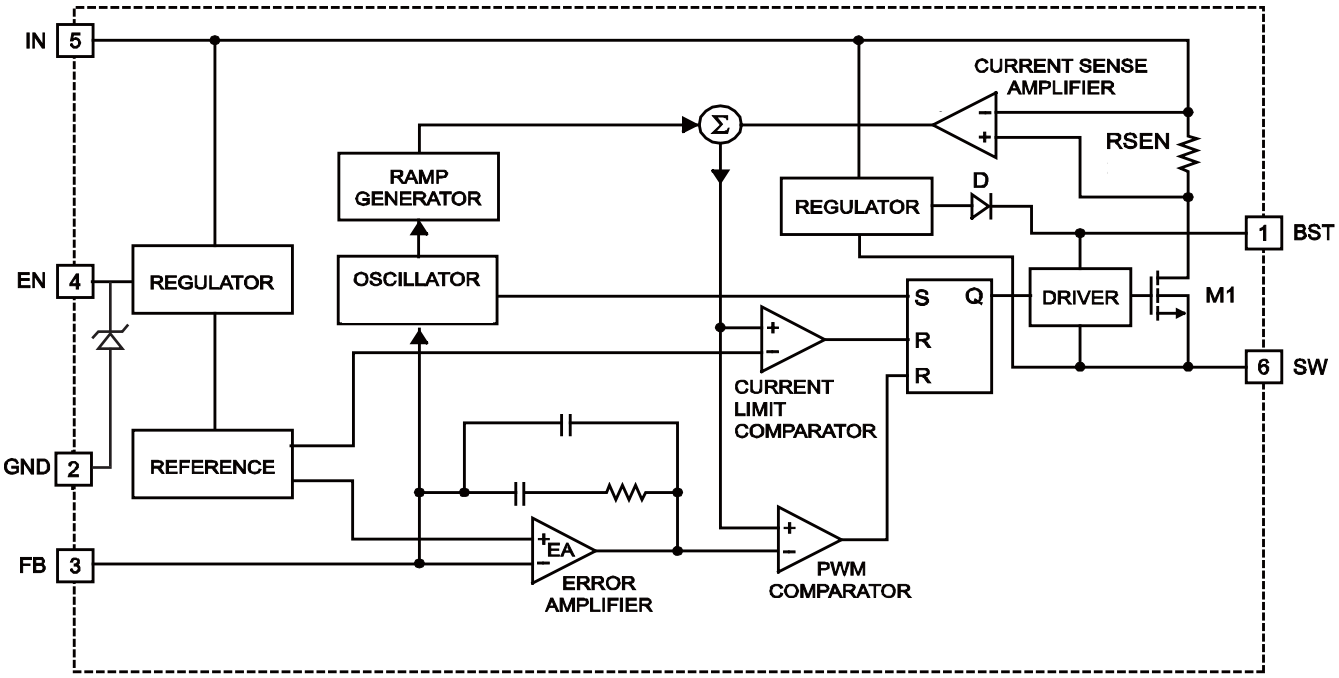


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application). Table 1 lists a selection of resistor combinations for common output voltages. The feedback resistor (R2) also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). R1 is then:

$$R1 = \frac{R2}{\frac{V_{OUT}}{0.812V} - 1}$$

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	102 (1%)	124 (1%)
2.5	59 (1%)	124 (1%)
3.3	40.2 (1%)	124 (1%)
5	23.7 (1%)	124 (1%)

Inductor Selection

Use an inductor with a DC-current rating at least 25% percent higher than the maximum load current for most applications. Select an inductor with a DC resistance <200mΩ for highest efficiency. Most designs can use the inductance value calculated from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}}$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current at 30% of the maximum load current. The maximum inductor peak current is then:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (<100mA), use a larger inductor to improve efficiency.

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input-capacitor impedance at the switching frequency should be less than the input-source impedance to prevent high-frequency-switching current from passing through the input. Use ceramic capacitors with X5R or X7R dielectrics because of their low ESR and small temperature coefficients. For most applications, a 4.7μF capacitor is sufficient.

Output Capacitor Selection

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance should be low at the switching frequency. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR characteristics. For most applications, a 22μF ceramic capacitor is sufficient.

PCB Layout Guide

PCB layout is very important to achieve stable operation. Please follow these guidelines and use Figure 2 as reference.

1) Keep the switching-current path short and minimize the loop area formed by input capacitor, high-side MOSFET, and Schottky diode.
2) Keep the connection from the Schottky diode to the SW pin and the input power ground as short and wide as possible.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as the FB path.
5) Connect IN, SW, and GND to large copper areas to cool the chip to improve thermal performance and long-term reliability. For single layer PCB, avoid soldering the exposed pad.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

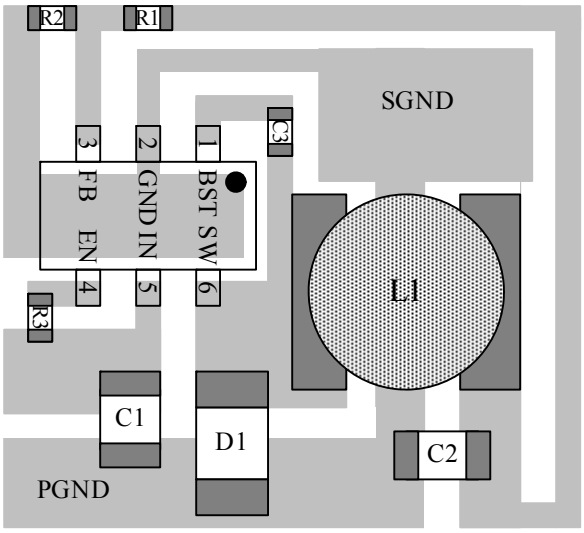


Figure 2: PCB Layout

External Bootstrap Diode

An external bootstrap diode improve regulator efficiency under the following conditions:

- V_{OUT}=5V or 3.3V; and
- Duty cycle is high: D= $\frac{V_{OUT}}{V_{IN}}$ >65%

Use an external BST diode from the BST pin to the regulator for best performance, as per Figure 3.

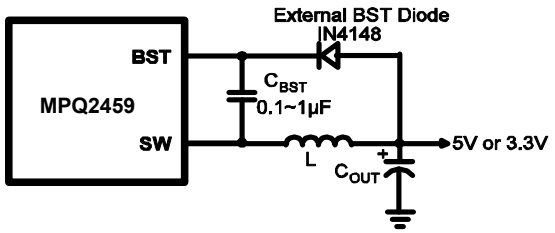


Figure 3: Optional External Bootstrap Diode to Enhance Efficiency.

Use an IN4148 external BST diode, and a 0.1µF-1µF. BST capacitor.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

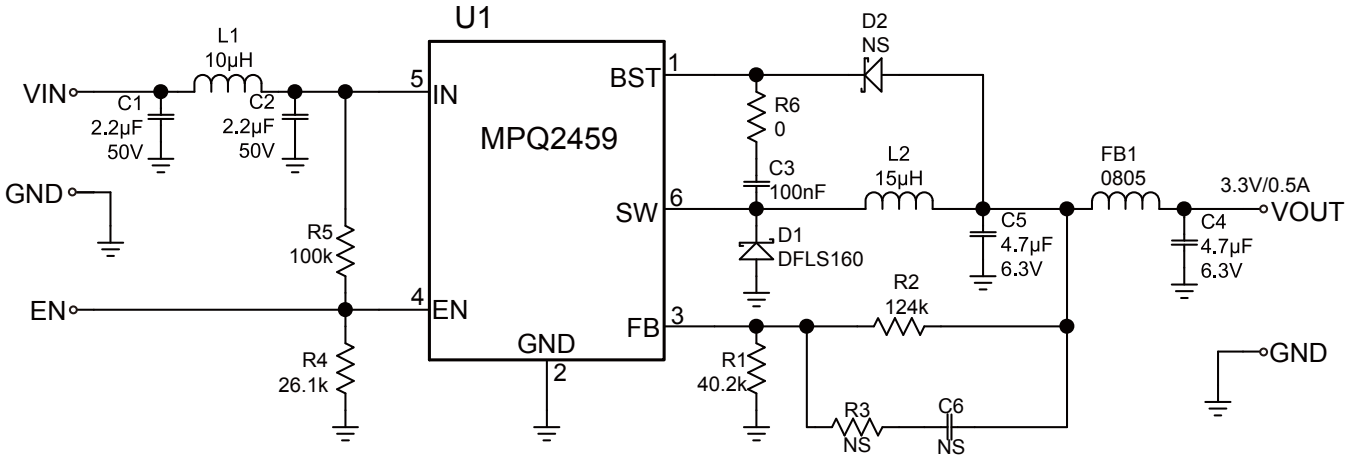
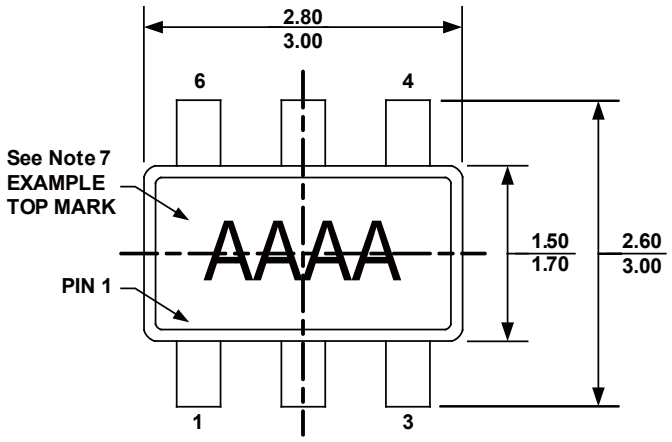


Figure 4: Typical Application Circuit with EMI Concern

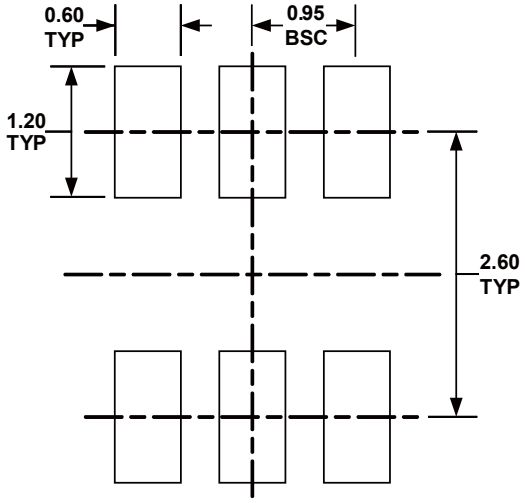
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

PACKAGE INFORMATION

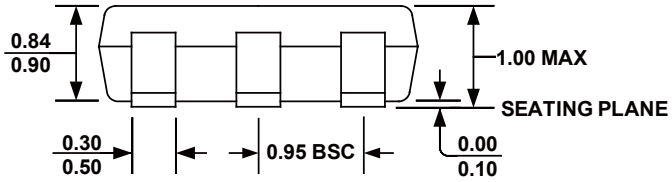
TSOT23-6



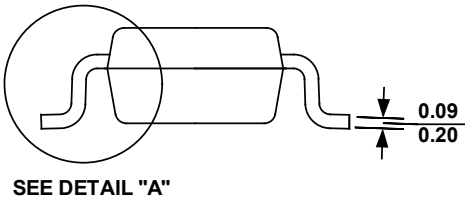
TOP VIEW



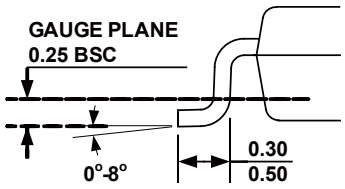
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL “A”

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE0.10 MILLIMETERS MAX
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.