

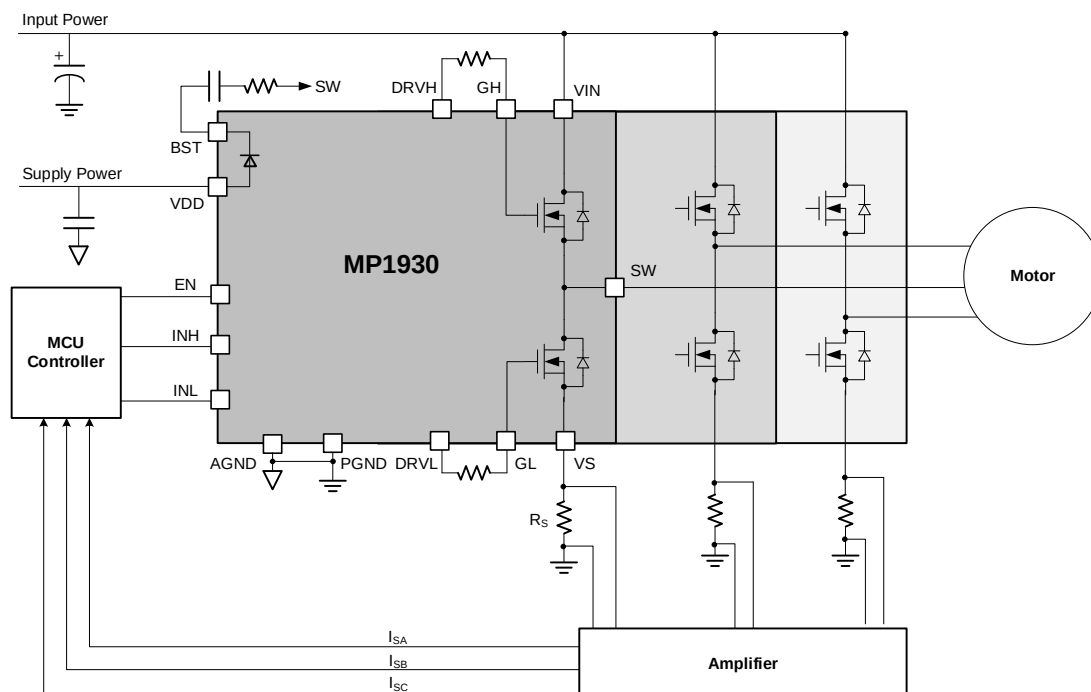


The MP1930 is available in a QFN-26 (7mmx7mm) package.

- Recommended 75V Maximum Input Voltage (V_{IN})
- Simple Logic Interface
- Up to 10A of Continuous Output Current (I_{OUT})
- Transistor-to-Transistor Logic (TTL)-Compatible Input
- On-Chip Bootstrap (BST) Diode
- Under-Voltage Lockout (UVLO) for Both the High-Side (HS) and Low-Side (LS) Pre-Drivers
- Quiescent Current (I_Q) Below 130 μ A
- Available in a QFN-26 (7mmx7mm) Package

- Motor Drivers
- Buck DC/DC Converters

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP1930GQN	QFN-26 (7mmx7mm)	See Below	3

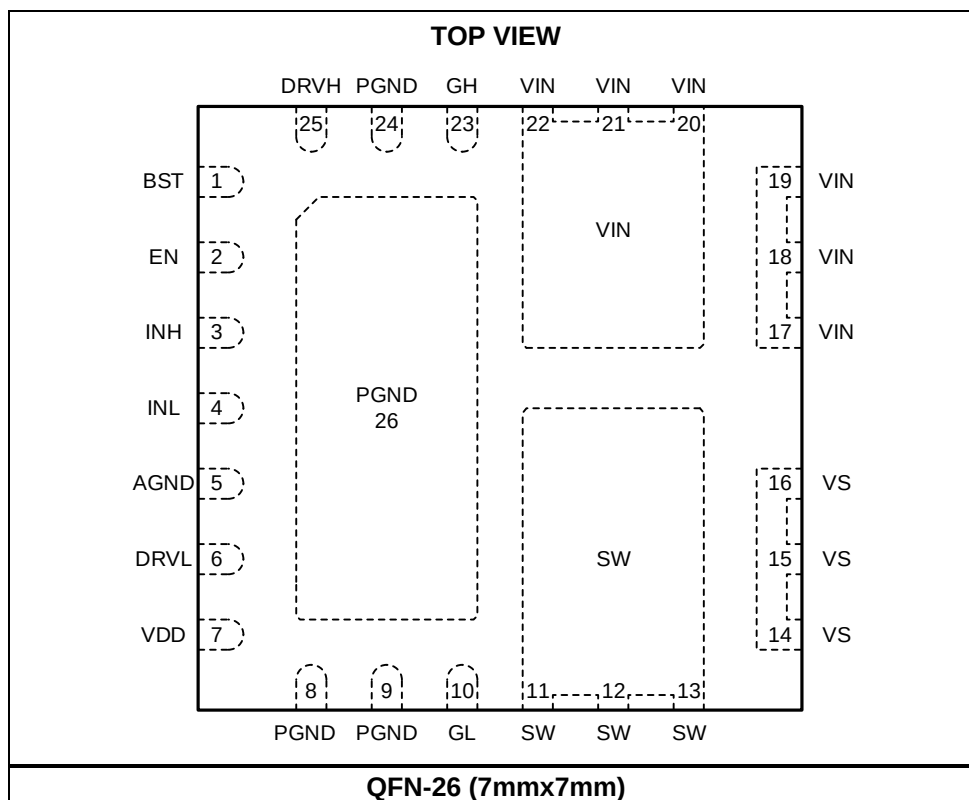
* For Tape & Reel, add suffix -Z (e.g. MP1930GQN-Z).

TOP MARKING

MPSYYWW
MP1930
LLLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP1930: Part number
LLLLLLLLLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	BST	Bootstrap. The BST pin is the positive power supply for the internal high-side MOSFET (HS-FET) driver. Connect a 0.22μF to 1μF bypass capacitor between the BST and SW pins.
2	EN	Enable. Pull the EN pin low to disable the IC; pull this pin high to enable the IC.
3	INH	Control signal input for the high-side (HS) driver.
4	INL	Control signal input for the low-side (LS) driver.
5	AGND	Driver ground.
6	DRVL	LS driver output. Connect a resistor between the DRVL and GL pins to decrease the start-up speed of the MOSFET.
7	VDD	Supply input. The VDD pin supplies power to all the driver circuitry. Place a 4.7μF to 22μF decoupling capacitor to ground, close to VDD, to ensure a stable and clean supply.
8, 9, 24, 26	PGND	Power ground.
10	GL	Gate node of the low-side MOSFET (LS-FET).
11, 12, 13	SW	Switching node.
14, 15, 16	VS	Source node of the LS-FET.
17, 18, 19, 20, 21, 22	VIN	Input voltage supply of the power stage. Connect the VIN pin to the node of the HS-FET's drain side.
23	GH	Gate node of the HS-FET.
25	DRVH	HS driver output. Connect a resistor between the DRVH and GH pins to decrease the start-up speed of the MOSFET.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Input voltage (V _{IN})	100V
Supply voltage (V _{DD})	-0.3V to +20V
SW voltage (V _{SW})	-1V to +100V
BST to SW	-0.3V to +18V
DRVH, GH to SW....	-0.3V to (BST - SW) + 0.3V
DRVL, GL to VSS	-0.3V to +20V
INH, INL, EN	-0.3V to +20V
Continuous power dissipation (T _A = 25°C) ⁽²⁾	5W
Junction temperature (T _J)	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

Recommended Operating Conditions ⁽³⁾

Supply voltage (V _{DD})	9V to 18V
Input voltage (V _{IN})	18V to 75V
Operating junction temp (T _J)....	-40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
QFN-26 (7mmx7mm).....	25	4.... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may generate an excessive die temperature, which can cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{DD} = 12V$, $V_{EN} = \text{high}$, $V_{IN} = 48V$, $V_S = \text{PGND}$, $f_{SW} = \text{float}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Currents						
VDD leakage current	I _{LK_VDD}	EN = low			1	μA
VDD quiescent current	I _{DDQ}	INL = INH = 0V		80	100	μA
VDD operating current	I _{DDO}	f _{SW} = 20kHz, disconnect DRVL, GL, DRVH, and GH		0.17		mA
		f _{SW} = 20kHz, DRVL = GL, DRVH = GH		0.8		mA
SW leakage current	I _{LK_SW}	EN = low			1	μA
MOSFET						
Drain-to-source breakdown voltage	V _{BR_DS}	V _{GS} = 0V, I _D = 250μA, EN = 0V	100			V
Gate threshold voltage	V _{GS_TH}	V _{DS} = V _{GS} , I _D = 250μA		1.9	2.4	V
Drain-to-source on resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 1A		11		mΩ
Total gate charge ⁽⁵⁾	Q _G	V _{DS} = 50V, V _{GS} = 0V to 4.5V, I _D = 20A		14.2		nC
Gate source charge ⁽⁵⁾	Q _{GS}			6.2		nC
Gate drain charge ⁽⁵⁾	Q _{GD}			5		nC
Inputs						
INL/INH high					2.4	V
INL/INH low			1			V
INL/INH internal pull-down resistance	R _{IN}			180		kΩ
Under-Voltage Protection (UVP)						
V _{DD} rising threshold	V _{DD_R}			5		V
V _{DD} hysteresis	V _{DD_H}			0.5		V
BST - SW rising threshold	V _{BST_R}			3.9		V
BST- SW hysteresis	V _{BS_TH}			0.3		V
Bootstrap (BST) Diode						
BST diode forward voltage at 100μA	V _{F1}				0.8	V
BST diode forward voltage at 10mA	V _{F2}				1	V
BST diode dynamic resistance	R _D	100mA		2.9		Ω
Low-Side (LS) Gate Driver						
Low output voltage	V _{OUT_LL}	I _{OUT} = 100mA		0.15	0.3	V
High output voltage to rail	V _{OUT_HL}	I _{OUT} = -100mA		0.33	0.5	V
High-Side (HS) Gate Driver						
Low output voltage	V _{OUT_LH}	I _{OUT} = 100mA		0.15	0.3	V
High output voltage to rail	V _{OUT_HH}	I _{OUT} = -100mA		0.33	0.6	V
Switching Specifications of the LS Gate Driver						
INL falling to DRVL falling shutdown propagation delay	t _{DLFF}			20		ns
INL rising to DRVL rising start-up propagation delay	t _{DLRR}			20		ns
DRVL rising time		C _L = 1nF		19		ns
DRVL falling time		C _L = 1nF		12		ns

ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = 12V$, $V_{EN} = \text{high}$, $V_{IN} = 48V$, $V_S = \text{PGND}$, $f_{SW} = \text{float}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Specifications of the HS Gate Driver						
INH falling to DRVH falling shutdown propagation delay	t_{DHFF}			20		ns
INH rising to DRVH rising start-up propagation delay	t_{DHRR}			20		ns
DRVH rising time		$C_L = 1\text{nF}$		19		ns
DRVH falling time		$C_L = 1\text{nF}$		12		ns
Switching Specifications for Matching						
Minimum input pulse width to change the output	t_{PW}				50 ⁽⁵⁾	ns
BST diode start-up or shutdown time	t_{BS}			10 ⁽⁵⁾		ns
Thermal shutdown				150		$^\circ\text{C}$
Thermal shutdown hysteresis				25		$^\circ\text{C}$

Note:

5) Guaranteed by design.

TIMING DIAGRAM

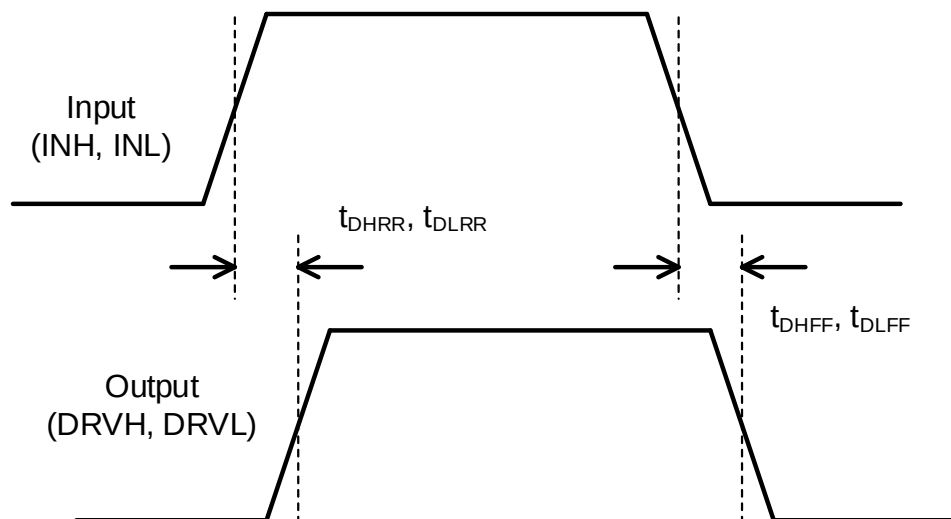


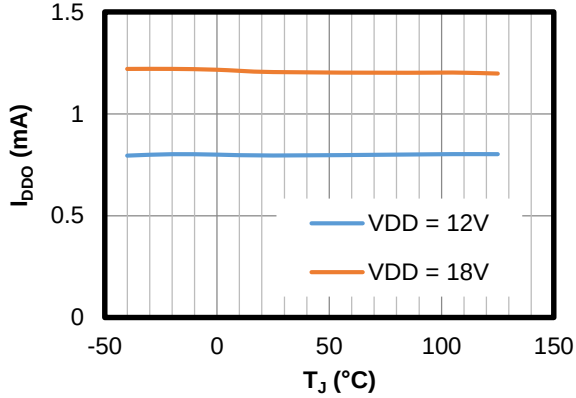
Figure 1: Timing Diagram

TYPICAL CHARACTERISTICS

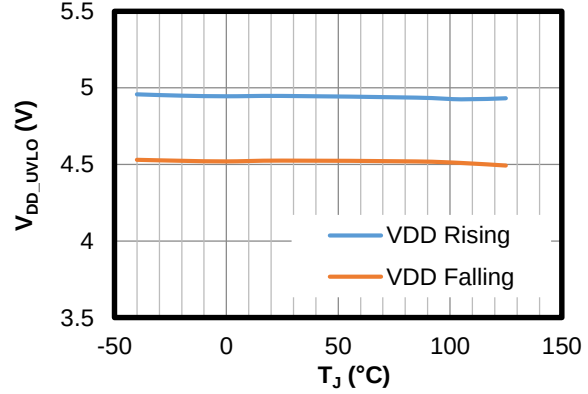
$V_{IN} = 48V$, $V_{DD} = 12V$, $T_A = 25^{\circ}C$, unless otherwise noted.

VDD Operating Current vs. Junction Temperature

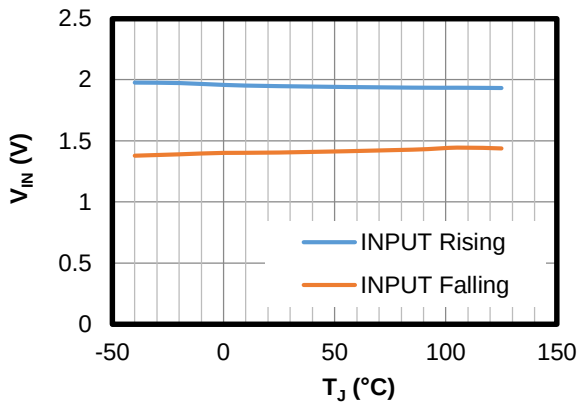
$f_{SW} = 20kHz$, $DRV_L = GL$, $DRV_H = GH$



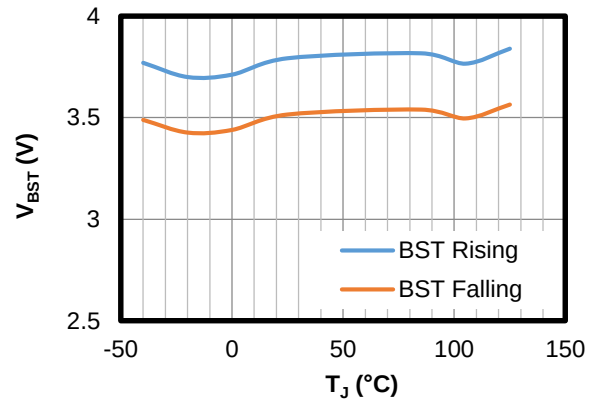
V_{DD} UVLO Threshold vs. Junction Temperature



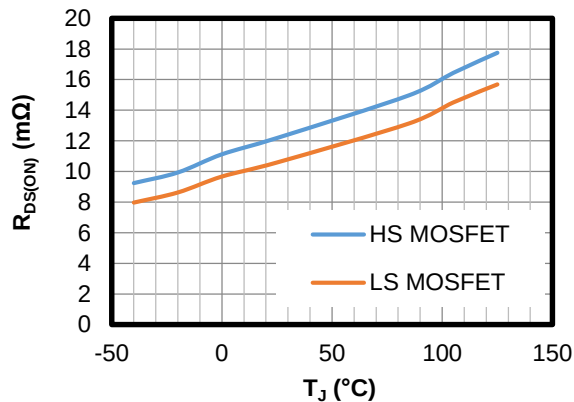
Input Voltage vs. Junction Temperature



Bootstrap Threshold vs. Junction Temperature



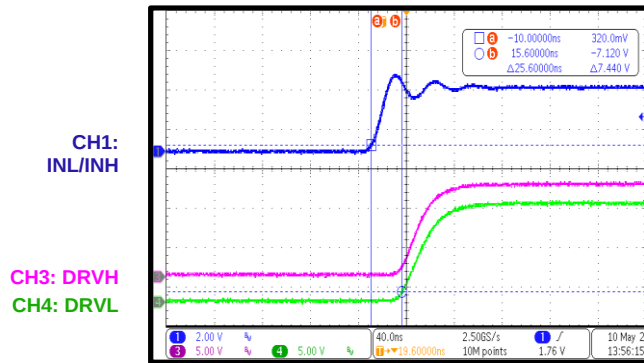
MOSFET On Resistance vs. Junction Temperature



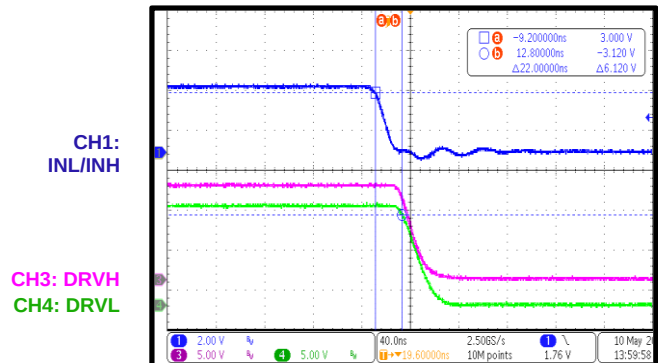
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 12V$, $f_{SW} = 20kHz$, $T_A = 25^{\circ}C$, unless otherwise noted.

Start-Up Propagation Delay and Driver Rising Time

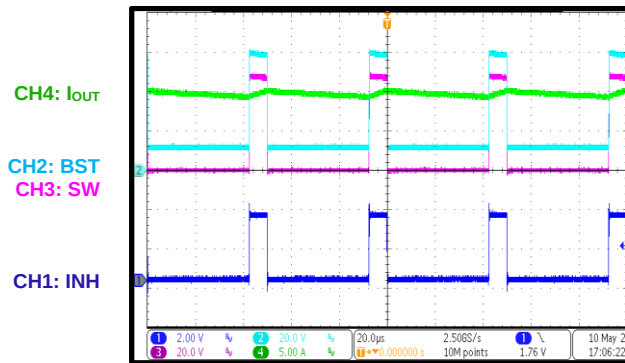


Shutdown Propagation Delay and Driver Falling Time



SW Waveform

$V_{IN} = 48V$, $I_{OUT} = 10A$



FUNCTIONAL BLOCK DIAGRAM

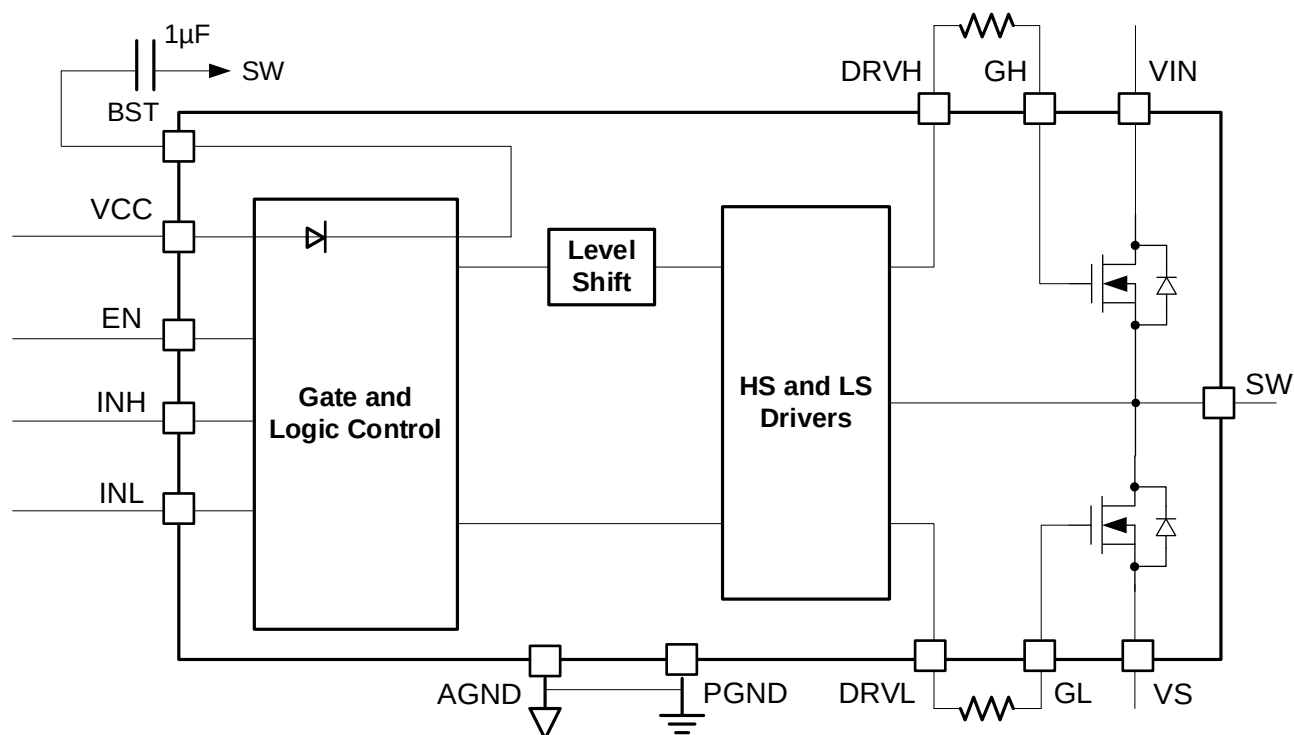


Figure 2: Functional Block Diagram

OPERATION

The INH and INL input signals can be controlled independently. If both INH and INL control the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) of the same bridge, set a sufficient dead time (DT) between low INH and INL (and vice versa) to avoid shoot-through. DT is the time interval between the two inputs crossing the rising or falling threshold. To prevent shoot-through, the minimum start-up DT must be at least 15ns, and the minimum shutdown DT must be at least 20ns.

Under-Voltage Lockout (UVLO)

If the V_{DD} voltage (V_{DD}) or BST voltage (V_{BST}) drops below their respective under-voltage lockout (UVLO) thresholds, both the DRVH and DRVL outputs go low to turn off both MOSFETs. Once V_{DD} exceeds its UVLO threshold, both DRVH and DRVL remain low until a rising edge is detected on either INH or INL.

Table 1 shows the operation of the HS-FET and LS-FET under different INH, INL, and UVLO conditions.

Table 1: States of the Driver Outputs under Different Conditions

EN	V _{BST} - V _{SW}	V _{DD}	INH	INL	DRVH	DRVL	UVLO Latch Status	Operating Conditions
0	X ⁽⁶⁾	X ⁽⁶⁾	X ⁽⁶⁾	X ⁽⁶⁾	Open	Pull down	X ⁽⁶⁾	X ⁽⁶⁾
1	X ⁽⁶⁾	X ⁽⁶⁾	0	0	0	0	X ⁽⁶⁾	Normal operation
	X ⁽⁶⁾	X ⁽⁶⁾	1	1	0	0	X ⁽⁶⁾	
	X ⁽⁶⁾	Exceeds UVLO	0	1	0	1	Normal	
	Exceeds UVLO	Exceeds UVLO	1	0	1	0	Normal	
	Exceeds UVLO	Exceeds UVLO	1	1	1	1	Normal	
	Drops below UVLO	Above UVLO	X ⁽⁶⁾	X ⁽⁶⁾	0	0	Normal to tripped	Normal-to-tripped transition
	Exceeds UVLO	Drops below UVLO	X ⁽⁶⁾	X ⁽⁶⁾	0	0	Normal to tripped	
	X ⁽⁶⁾	Exceeds UVLO	0 or 1	0 or 1	0	0	Tripped	When the UVLO latch is tripped
	X ⁽⁶⁾	Below UVLO	X ⁽⁶⁾	X ⁽⁶⁾	0	0	Tripped	
	X ⁽⁶⁾	Exceeds UVLO	0 to 1	0 to 1	0	0	Tripped, then reset by INL and INH	Tripped to normal transition
	X ⁽⁶⁾	Exceeds UVLO	1 to 0	1	0	0 to 1	Tripped, then reset by falling INH	
	Below UVLO	Exceeds UVLO	1	1 to 0	0	0	Tripped, then reset by falling INL	
	Exceeds UVLO	Exceeds UVLO	1	1 to 0	1	1 to 0	Tripped, then reset by falling INL	
	Below UVLO	Exceeds UVLO	0	0 to 1	0	0 to 1	Tripped, then reset by INL	
	Below UVLO	Exceeds UVLO	0 to 1	0	0	0	Tripped, then reset by INH	
	Exceeds UVLO	Exceeds UVLO	0 to 1	0	0 to 1	0	Tripped, then reset by INH	

Note:

6) "X" refers to an undetermined logic voltage.

APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor (C_{IN}) can reduce the device's switching noise as well as the surge current drawn from the input supply. For the VDD pin, it is recommended to use a larger-value ceramic capacitor with X5R or X7R dielectrics (e.g. a 4.7 μ F ceramic capacitor rated for a minimum of 25V) due to their low-ESR and temperature coefficients.

Adding the Bootstrap (BST) Resistor

The switching ring at the SW pin may cause MOSFET damage, especially at high input voltage (V_{IN}). Add a small resistor in series with the bootstrap (BST) capacitor (C_{BST}) to reduce the risk of damage. A large resistor causes more power dissipation. Generally, a 3.3 Ω resistance is sufficient.

Adding the Driving Resistor

The driving resistor limits the start-up and shutdown rates of the MOSFET for improved electromagnetic compatibility (EMC) performance. A large driving resistance results in more power dissipation.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, follow the guidelines below:

1. Place some input bypass ceramic capacitors next to the MP1930 on the same layer.
2. Do not pull all the input bypass capacitors on the device's backside.
3. Use as many vias and V_{IN} planes as possible to reduce the switching spike.
4. Place a VDD decoupling capacitor close to the device.
5. Connect AGND and PGND at the point of the VDD capacitor's ground connection.
6. Keep the path of the switching current short.
7. Minimize the loop area formed by C_{IN} .
8. Keep the connection between SW and the input power ground as short and wide as possible.
9. Place C_{BST} as close to the device as possible.

TYPICAL APPLICATION CIRCUIT

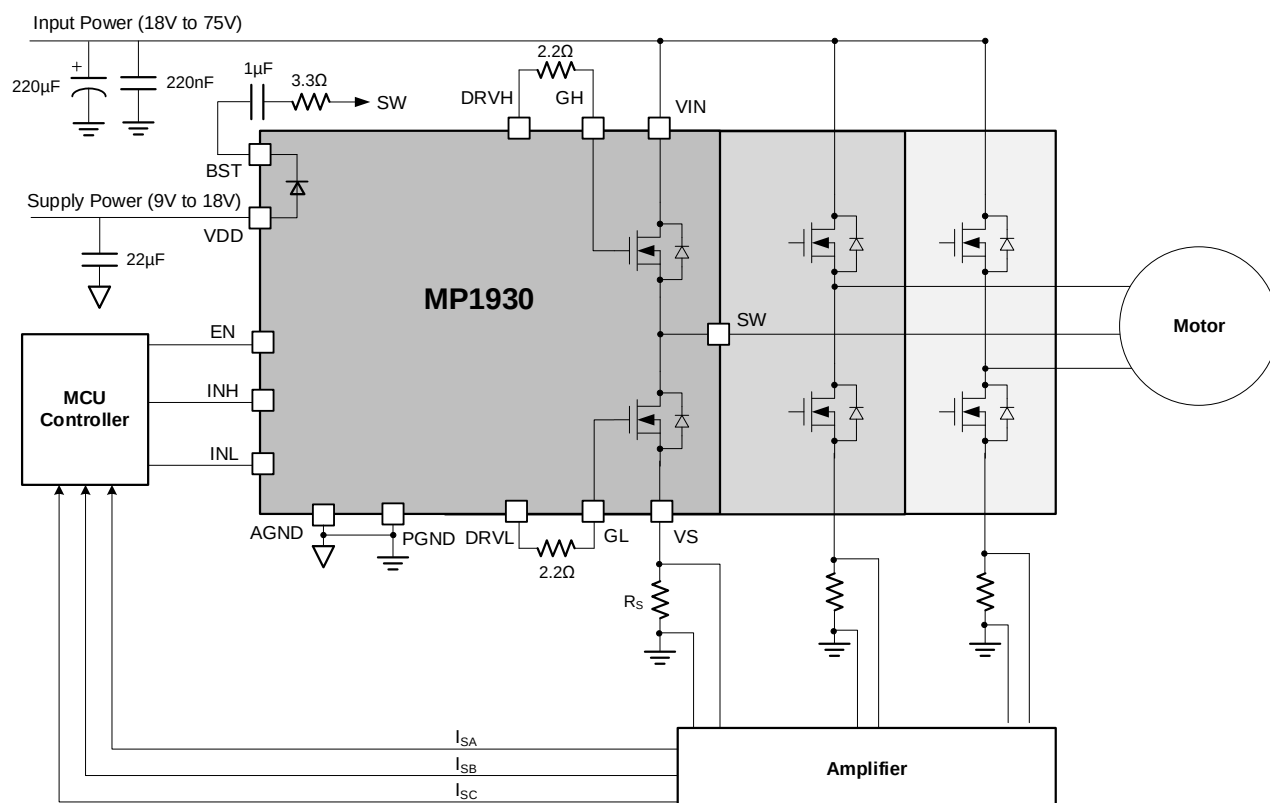
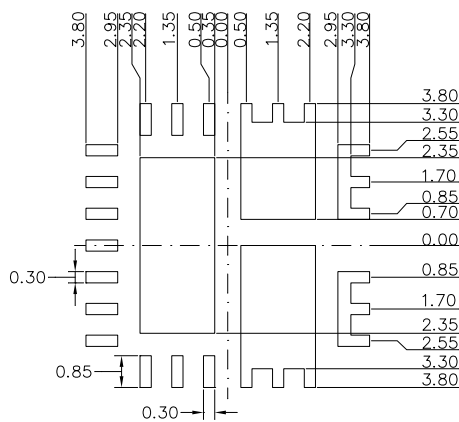
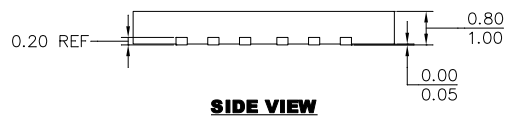
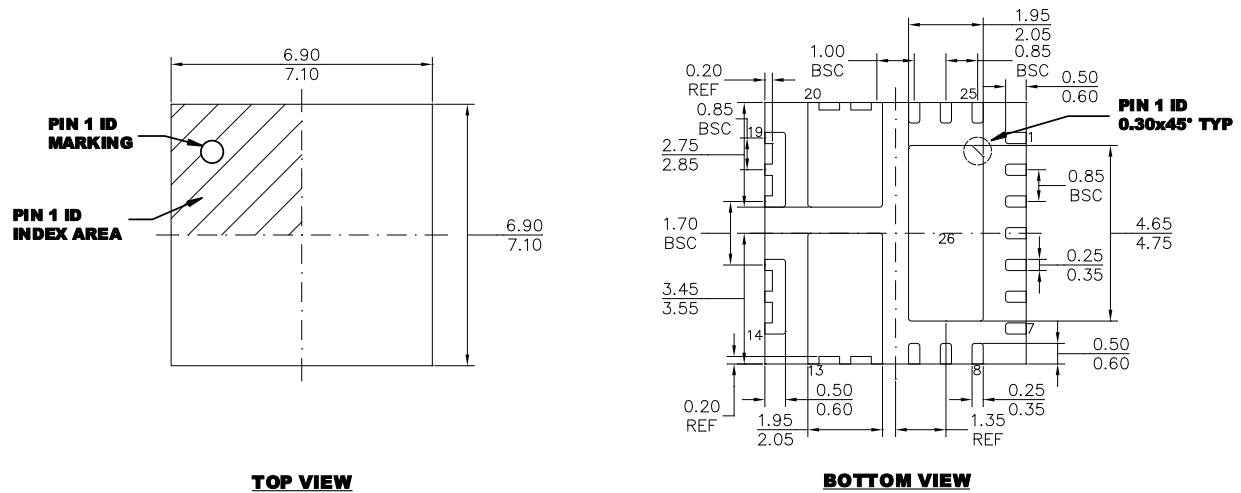


Figure 3: Typical Application Circuit (with BLDC Motor Driver)

PACKAGE INFORMATION

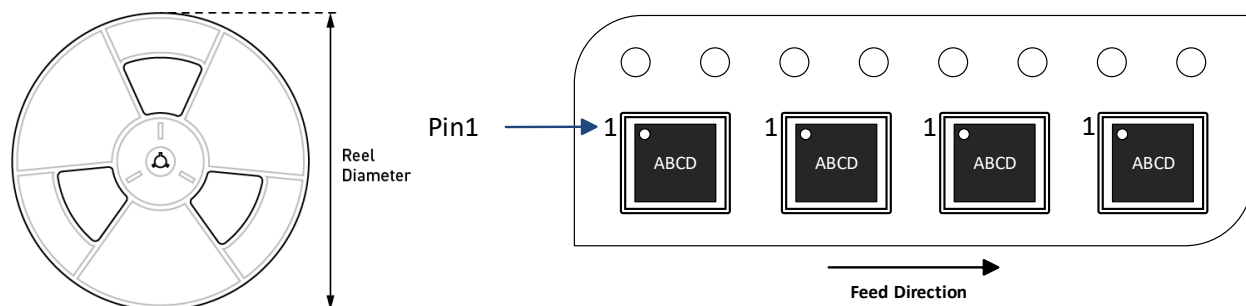
QFN-26 (7mmx7mm)



NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP1930GQN-Z	QFN-26 (7mmx7mm)	2500	N/A	N/A	13in	16mm	12mm



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/11/2024	Initial Release	-

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