MPQ8633B

16V, 20A, Synchronous, Step-Down Converter with Adjustable Current Limit, Programmable Frequency, and Voltage Tracking

The Future of Analog IC Technology®

DESCRIPTION

The MPQ8633B is a fully integrated, high-frequency, synchronous, buck converter. It offers a very compact solution that achieves up to 20A of output current with excellent load and line regulation over a wide input supply range. The MPQ8633B operates at high efficiency over a wide output current load range.

The MPQ8633B adopts an internally compensated constant-on-time (COT) control mode that provides fast transient response and eases loop stabilization.

The operating frequency can be set to 600kHz, 800kHz, or 1000kHz easily with MODE configuration, allowing the MPQ8633B frequency to remain constant regardless of the input and output voltages.

The output voltage start-up ramp is controlled by an internal 1ms timer. It can be increased by adding a capacitor on TRK/REF. An open-drain power good (PGOOD) signal indicates if the output is within its nominal voltage range. PGOOD is clamped at around 0.7V with an external pull-up voltage when the input supply fails to power the MPQ8633B.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MPQ8633B requires a minimal number of readily available, standard, external components and is available in a QFN-21 (3mmx4mm) package.

FEATURES

- Wide Input Voltage Range
  - 2.7V to 16V with External 3.3V VCC Bias
  - 4V to 16V with Internal Bias or External 3.3V VCC Bias
- Differential Output Voltage Remote Sense
- Programmable Accurate Current Limit Level
- 20A Output Current
- Low $R_{DS(ON)}$ Integrated Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Adaptive COT for Ultrafast Transient Response
- Stable with Zero ESR Output Capacitor
- 0.5% Reference Voltage over 0°C to +70°C Junction Temperature Range
- 1% Reference Voltage from -40°C to +125°C Junction Temperature Range
- Selectable Pulse Skip or Forced CCM Operation
- Excellent Load Regulation
- Output Voltage Tracking
- Output Voltage Discharge
- PGOOD Active Clamped at Low Level during Power Failure
- Programmable Soft-Start Time from 1ms
- Pre-Bias Start-Up
- Selectable Switching Frequency from 600kHz, 800kHz, and 1000kHz
- Non-Latch OCP, UVP, UVLO, Thermal Shutdown, and Latch-Off for OVP
- Output Adjustable from 0.6V to 90%*VIN, up to 5.5V Max
- Available in a QFN-21 (3mmx4mm) Package

APPLICATIONS

- Telecom and Networking Systems
- Servers, Cloud-Computing, Storage
- Base Stations
- General Purpose Point-of-Load (PoL)
- 12V Distribution Power Systems
- High-end TV
- Game Consoles and Graphic Cards

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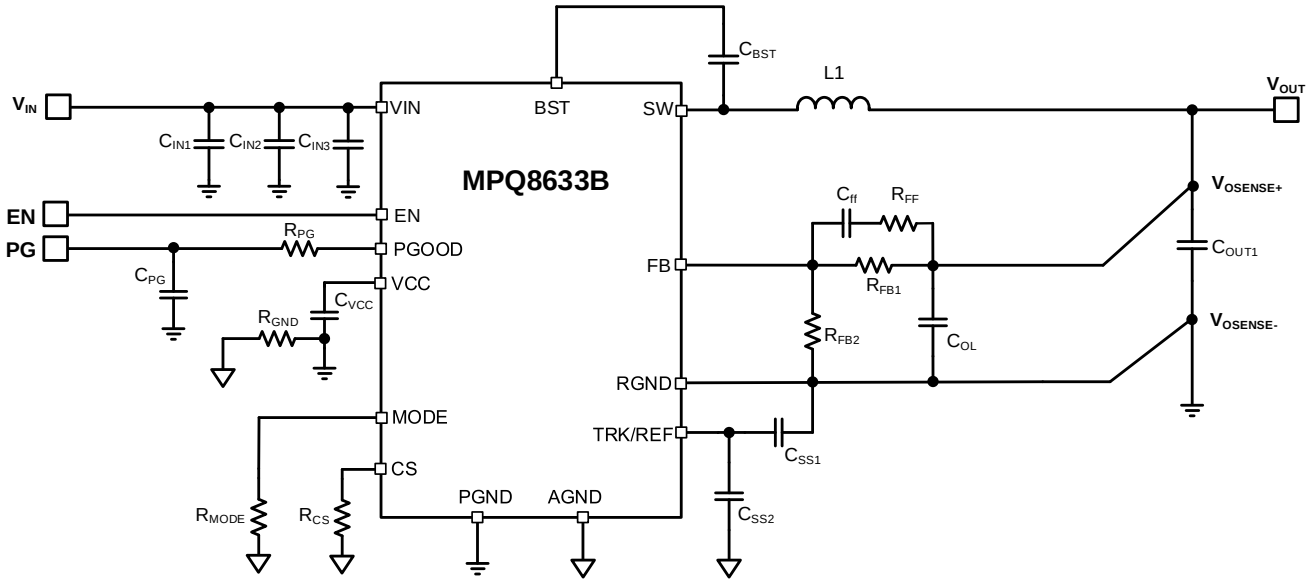
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ8633BGLE*	QFN-21 (3mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPQ8633BGLE–Z)

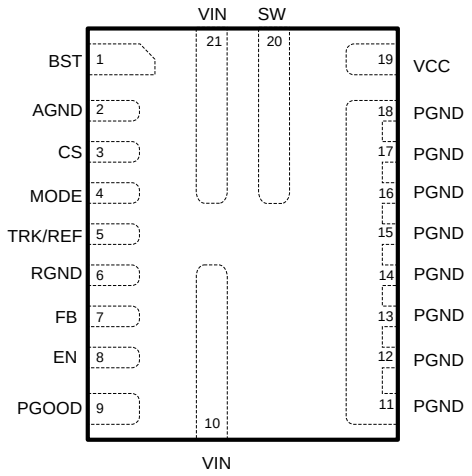
TOP MARKING

MPYW
8633
BLLL
E

MP: MPS prefix
Y: Year code
W: Week code
8633B: First five digits of the part number
LLL: Lot number
E: MPQ8633BGLE

PACKAGE REFERENCE

TOP VIEW



QFN-21 (3mmx4mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{IN} - V_{SW} (DC)..... -0.3V to +18.3V
V_{IN} - V_{SW} (25ns)..... -5V to +28V
V_{SW} (DC)..... -0.3V to +18.3V
V_{SW} (25ns) (2) ..... -5V to +25V
V_{BST}..... 22.3V
V_{BST} - V_{SW} (25ns) (2) 5V
V_{CC}, EN 4.5V
All other pins ..... -0.3V to 4.3V
Junction temperature ..... 170°C
Lead temperature..... 260°C
Storage temperature .....-65°C to +170°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4V to 16V
Output voltage (V_{OUT})..... 0.6V to 5.5V
External VCC bias (V_{CC_EXT})..... 3.12V to 3.6V
Output voltage (V_{OUT}).....0.6V to 5.5V
External VCC bias (V_{CC_EXT})..... 3.12V to 3.6V
Maximum output current (I_{OUT_MAX}) 20A
Maximum output current limit (I_{OC_MAX}) 24A
Maximum peak inductor current (I_{L_PEAK})..... 28A
EN voltage (V_{EN}) 3.6V
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance (4)

	θ_{JB}	θ_{JC_TOP}	
QFN-21 (3mmx4mm)	8	18	°C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) Measured using a differential oscilloscope probe.
3) The device is not guaranteed to function outside of its operating conditions.
4) θ_{JB} is the thermal resistance from the junction to the board around the PGND soldering point.
θ_{JC_TOP} is the thermal resistance from the junction to the top of the package.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		0	10	μA
Supply current (quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 0.62V		650	850	μA
MOSFET						
Switch leakage	SW_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
	SW_{LKG_LS}	V_{EN} = 0V, V_{SW} = 12V		0	30	
HS on-state resistance	$R_{DS_ON_HS}$	V_{EN} = 2V @ 25°C		8.6		mΩ
LS on-state resistance	$R_{DS_ON_LS}$	V_{EN} = 2V @ 25°C		2.5		mΩ
Current Limit						
Current limit threshold	V_{LIM}		1.15	1.2	1.25	V
I_{CS} to I_{OUT} ratio	I_{CS}/I_{OUT}	I_{OUT} ≥ 2A	9	10	11	μA/A
Low-side negative current limit	I_{LIM_NEG}			-10		A
Negative current limit time out[6]	t_{NCL_Timer}			200		ns
Switching Frequency						
Switching frequency [6]	f_{SW}	MODE = GND, I_{OUT} = 0A, V_{OUT} = 1V	480	600	720	kHz
		MODE = 30.1kΩ, I_{OUT} = 0A, V_{OUT} = 1V	680	800	920	kHz
		MODE = 60.4 kΩ, I_{OUT} = 0A, V_{OUT} = 1V	850	1000	1150	kHz
Minimum on time [5]	T_{ON_MIN}	V_{FB} = 500mV			50	ns
Minimum off time [5]	T_{OFF_MIN}	V_{FB} = 500mV			180	ns
Over-Voltage and Under-Voltage Protection						
OVP threshold	V_{OVP}		113%	116%	119%	V_{REF}
UVP threshold	V_{UVP}		77%	80%	83%	V_{REF}
Feedback Voltage and Soft Start						
Feedback voltage	V_{REF}	T_J = -40°C to +125°C	594	600	606	mV
		T_J = 0°C to +70°C	597	600	603	mV
TRK/REF sourcing current	I_{TRACK_Source}	$V_{TRK/REF}$ = 0V		42		μA
TRK/REF sinking current	I_{TRACK_Sink}	$V_{TRK/REF}$ = 1V		12		μA
Soft-start time	t_{SS}	C_{TRACK} = 1nF, T_J = +25°C	0.75	1	1.25	ms
Error Amplifier						
Error amplifier offset	V_{OS}		-3	0	3	mV
Feedback current	I_{FB}	V_{FB} = REF		50	100	nA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable and UVLO						
Enable input rising threshold	VIH_{EN}		1.17	1.22	1.27	V
Enable hysteresis	V_{EN-HYS}			200		mV
Enable input current	I_{EN}	V_{EN} = 2V		0		µA
Soft shutdown discharge FET	R_{ON_DISCH}			80	150	Ω
VIN UVLO						
VIN under-voltage lockout threshold rising	VIN_{Vth_Rise}	V_{CC} = 3.3V	2.1	2.4	2.7	V
VIN under-voltage lockout threshold falling	VIN_{vth_Fall}		1.55	1.85	2.15	
VCC Regulator						
VCC under-voltage lockout threshold rising	VCC_{Vth_Rise}		2.65	2.8	2.95	V
VCC under-voltage lockout threshold falling	VCC_{vth_Fall}		2.35	2.5	2.65	V
VCC regulator	V_{CC}		2.88	3.00	3.12	V
VCC load regulation		Icc = 25mA		0.5		%
Power Good						
Power good high threshold	$PG_{Vth_Hi_Rise}$	FB from low to high	89.5%	92.5%	95.5%	V_{REF}
Power good low threshold	$PG_{Vth_Lo_Rise}$	FB from low to high	113%	116%	119%	V_{REF}
	$PG_{Vth_Lo_Fall}$	FB from high to low	77%	80%	83%	V_{REF}
Power good low to high delay	PG_{Td}	T_J = 25°C	0.63	0.9	1.17	ms
Power good sink current capability	V_{PG}	I_{PG} = 10mA			0.5	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			3	µA
Power good low-level output voltage	V_{OL_100}	V_{IN} = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor @ 25°C		650	800	mV
	V_{OL_10}	V_{IN} = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor @ 25°C		750	900	mV
Thermal Protection						
Thermal shutdown (5)	T_{SD}			160		°C
Thermal shutdown hysteresis (5)				30		°C

NOTE:
5) Guaranteed by design.
6) Guaranteed by design over temperature.

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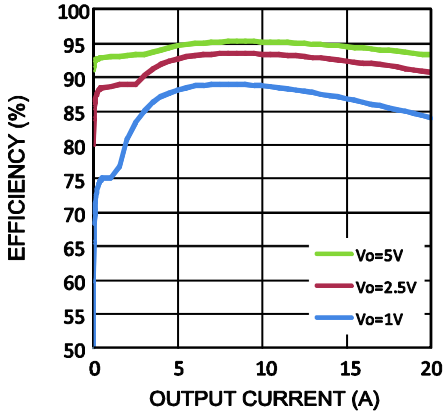
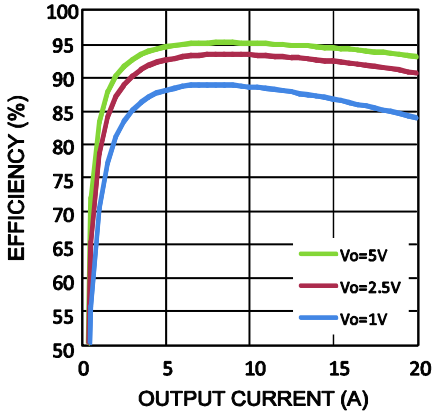
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = 25˚C, V_{OUT} = 1V, F_S = 800kHz unless otherwise noted.

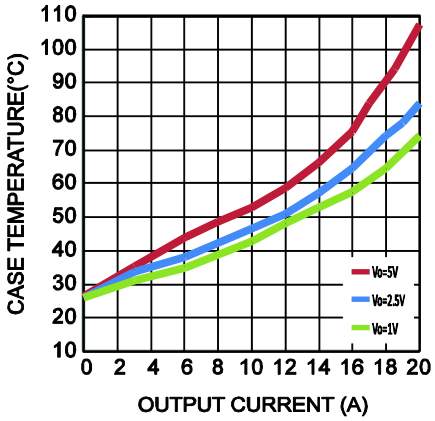
Efficiency
Pulse Skip, 0.4μH, 800kHz



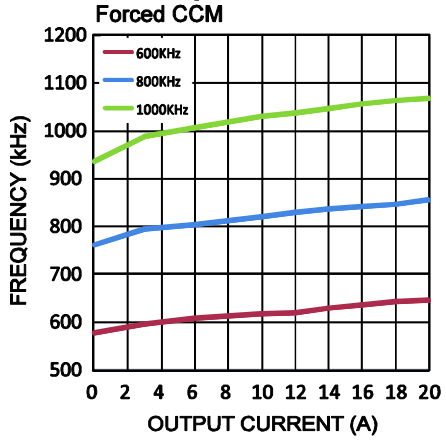
Efficiency
Forced CCM, 0.4μH, 800kHz



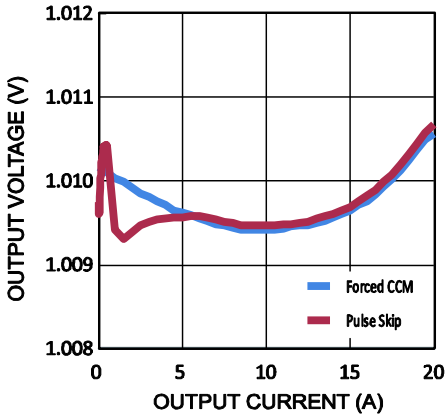
Thermal Results
800kHz, No Air-Flow



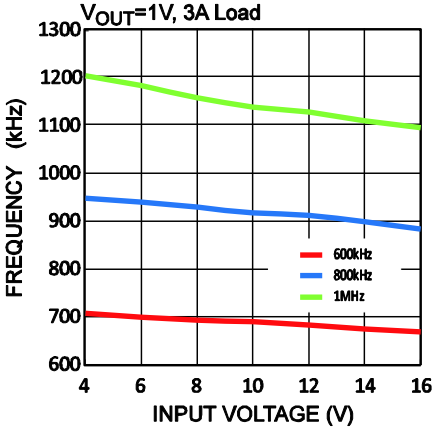
Switching Frequency vs. Output Current
Forced CCM



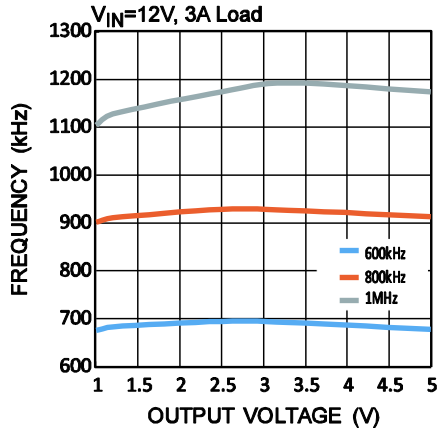
Output Voltage Load Regulation



Switching Frequency vs. Input Voltage
V_{OUT}=1V, 3A Load



Switching Frequency vs. Output Voltage
V_{IN}=12V, 3A Load



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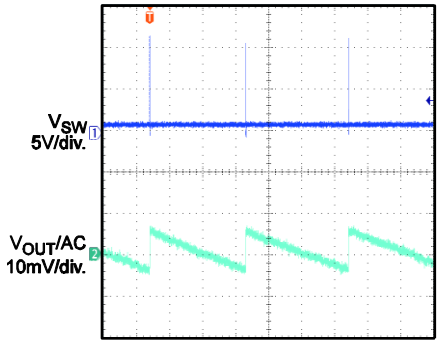
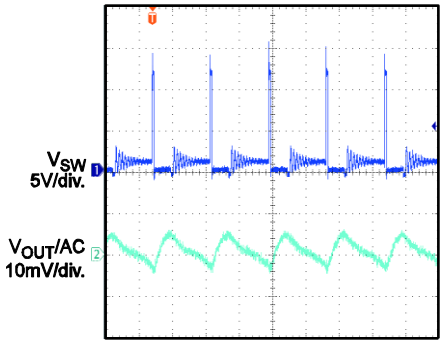
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25˚C, V_{OUT} = 1V, F_S = 800kHz unless otherwise noted.

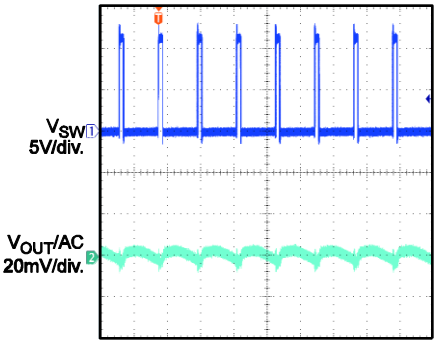
Steady State
I_{OUT} = 0A, Pulse Skip



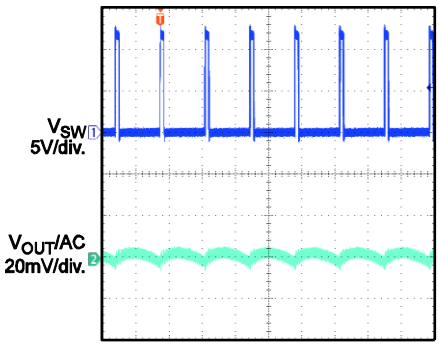
Steady State
I_{OUT} = 0.5A, Pulse Skip



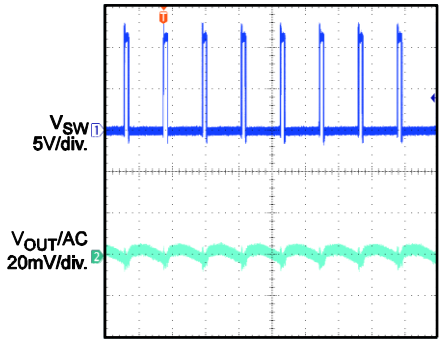
Steady State
I_{OUT} = 20A, Pulse Skip



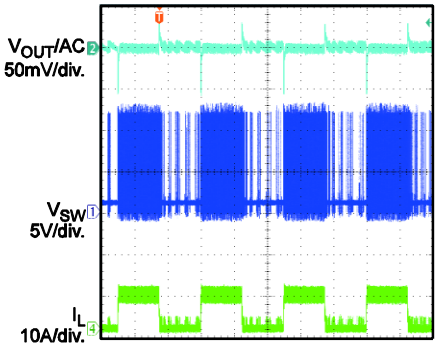
Steady State
I_{OUT} = 0A, Forced CCM



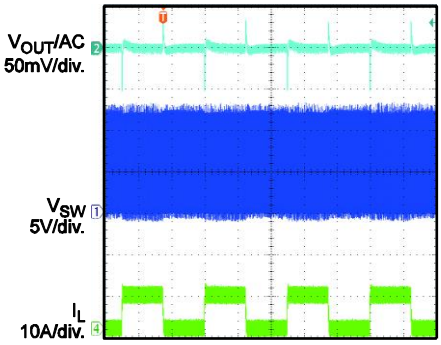
Steady State
I_{OUT} = 20A, Forced CCM



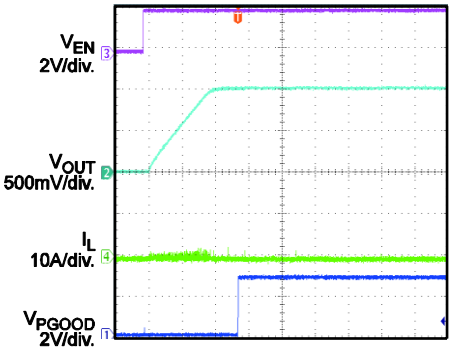
Load Transient
I_{OUT} =0A~8A, Pulse Skip



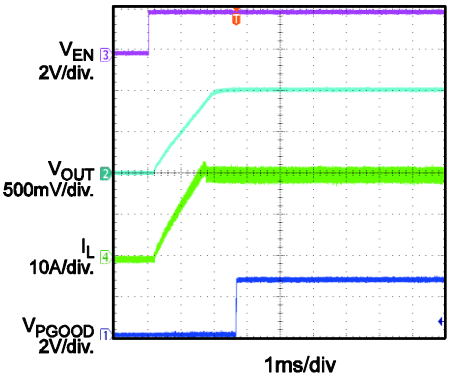
Load Transient
I_{OUT}=0A~8A, Forced CCM



Power Up through EN
I_{OUT} = 0A, Pulse Skip



Power Up through EN
I_{OUT} = 20A, Pulse Skip



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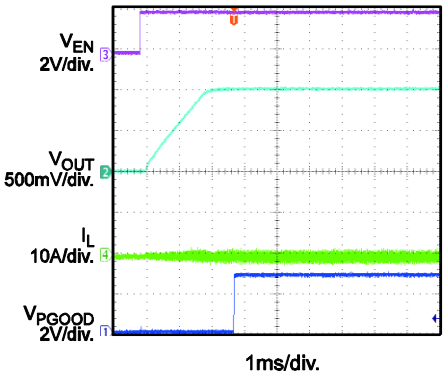
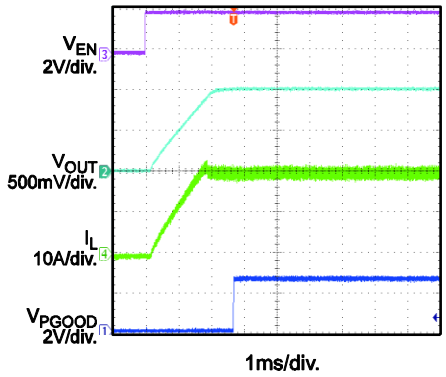
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25˚C, V_{OUT} = 1V, F_S = 800kHz unless otherwise noted.

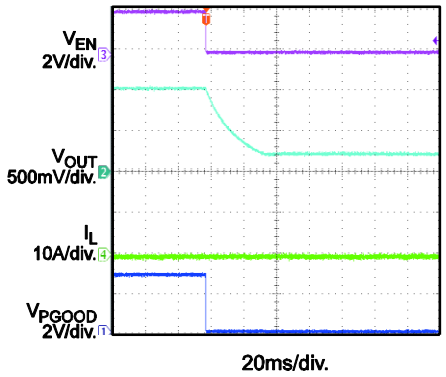
Power Up through EN
I_{OUT} = 0A, Forced CCM



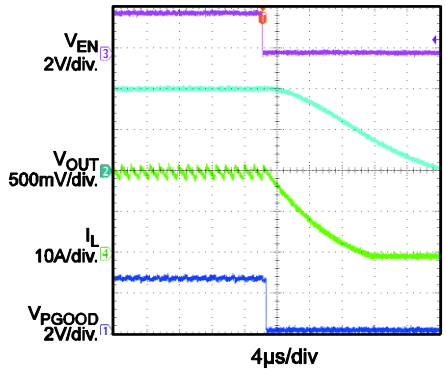
Power Up through EN
I_{OUT} = 20A, Forced CCM



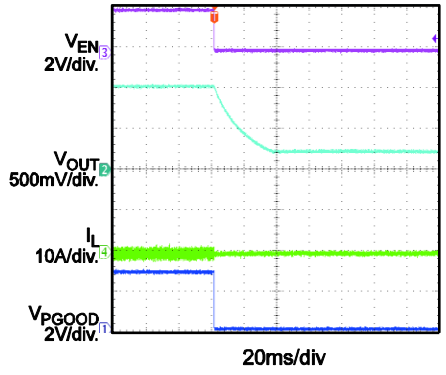
Power Down through EN
I_{OUT}=0A, Pulse Skip



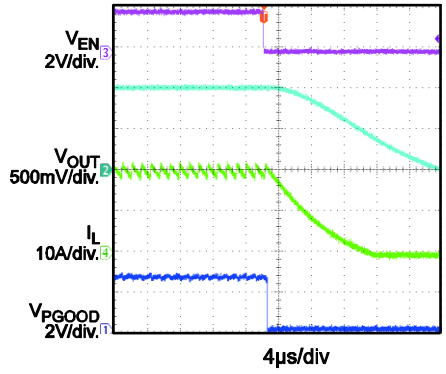
Power Down through EN
I_{OUT}=20A, Pulse Skip



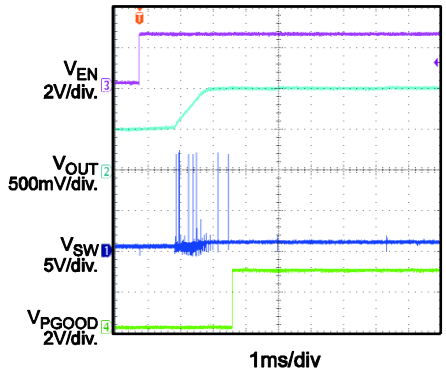
Power Down through EN
I_{OUT}=0A, Forced CCM



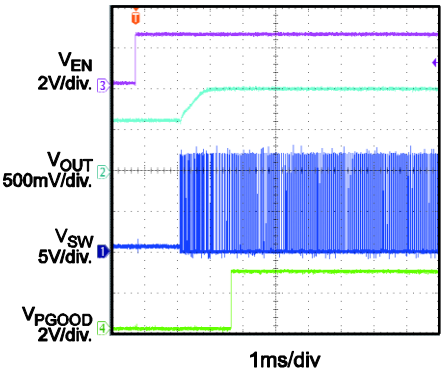
Power Down through EN
I_{OUT}=20A, Forced CCM



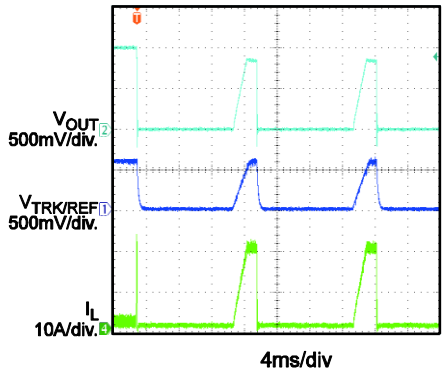
Pre-bias Start-Up
Pulse skip



Pre-bias Start-Up
Forced CCM



Over-Current
Protection Entry



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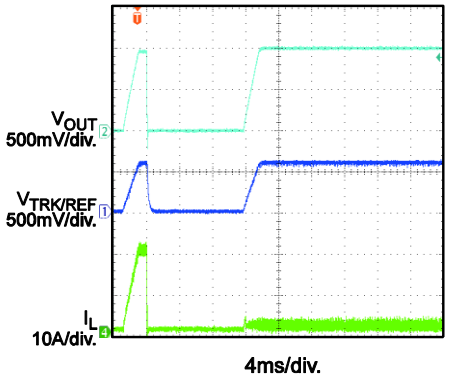
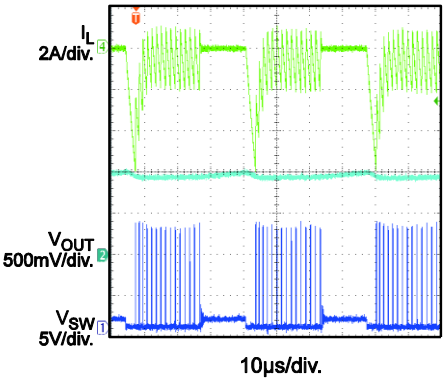
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25˚C, V_{OUT} = 1V, F_S = 800kHz unless otherwise noted.

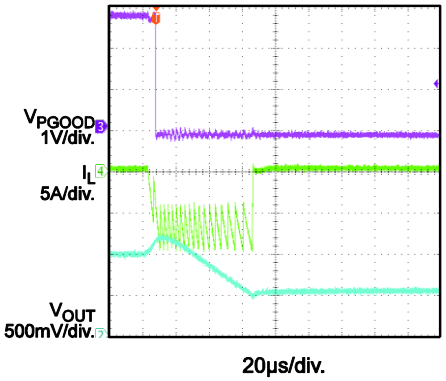
Over-Current
Protection Recovery



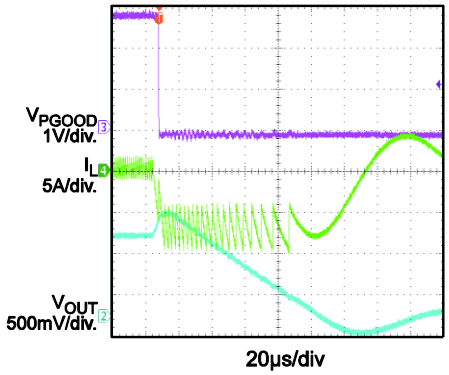
OSM Operation
Pulse Skip Mode



Over-Voltage Protection
Pulse Skip Mode



Over-Voltage Protection
Forced CCM



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PIN FUNCTIONS

QFN-21 PIN #	Name	Description
1	BST	**Bootstrap.** Connect a capacitor between SW and BS to form a floating supply across the high-side switch driver.
2	AGND	**Analog ground.** Select AGND as the control circuit reference point.
3	CS	**Current limit.** Connect a resistor to AGND to set the current limit trip point. See equation 4 for additional details.
4	MODE	**Operation mode selection.** Program MODE to select CCM, pulse skip mode, and the operating switching frequency. See Table 1 for additional details.
5	TRK/REF	**External tracking voltage input.** The output voltage tracks this input signal. Decouple TRK/REF with a ceramic capacitor placed as close to it as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. The capacitance of this capacitor determines the soft-start time. See Equation 2 and 3 for additional details.
6	RGND	**Differential remote sense negative input.** Connect RGND to the negative side of the voltage sense point directly. Short RGND to GND if the remote sense is not used.
7	FB	**Feedback (differential remote sense positive input).** An external resistor divider from the output to RGND tapped to FB sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces.
8	EN	**Enable.** EN is an input signal that turns the regulator on or off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. Connect EN to VIN through a pull-up resistor or a resistive voltage divider for automatic start-up. Do not float EN.
9	PGOOD	**Power good output.** PGOOD is an open-drain signal. A pull-up resistor connected to a DC voltage is required to indicate a logic high signal if the output voltage is within regulation. There is a delay of about 1ms between the time FB ≥ 92.5% and PGOOD pulling high.
10, 21	VIN	**Input voltage.** VIN supplies power for the internal MOSFET and regulator. Input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
11-18	PGND	**System ground.** PGND is the reference ground of the regulated output voltage. Therefore, care must be taken during PCB layout. Use wide PCB traces to make the connection.
19	VCC	**Internal 3V LDO output.** The driver and control circuits are powered from the VCC voltage. Decouple VCC with a ceramic capacitor at least 1µF placed as close to it as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
20	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW low during the off-time. Use wide PCB traces to make the connection.

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BLOCK DIAGRAM

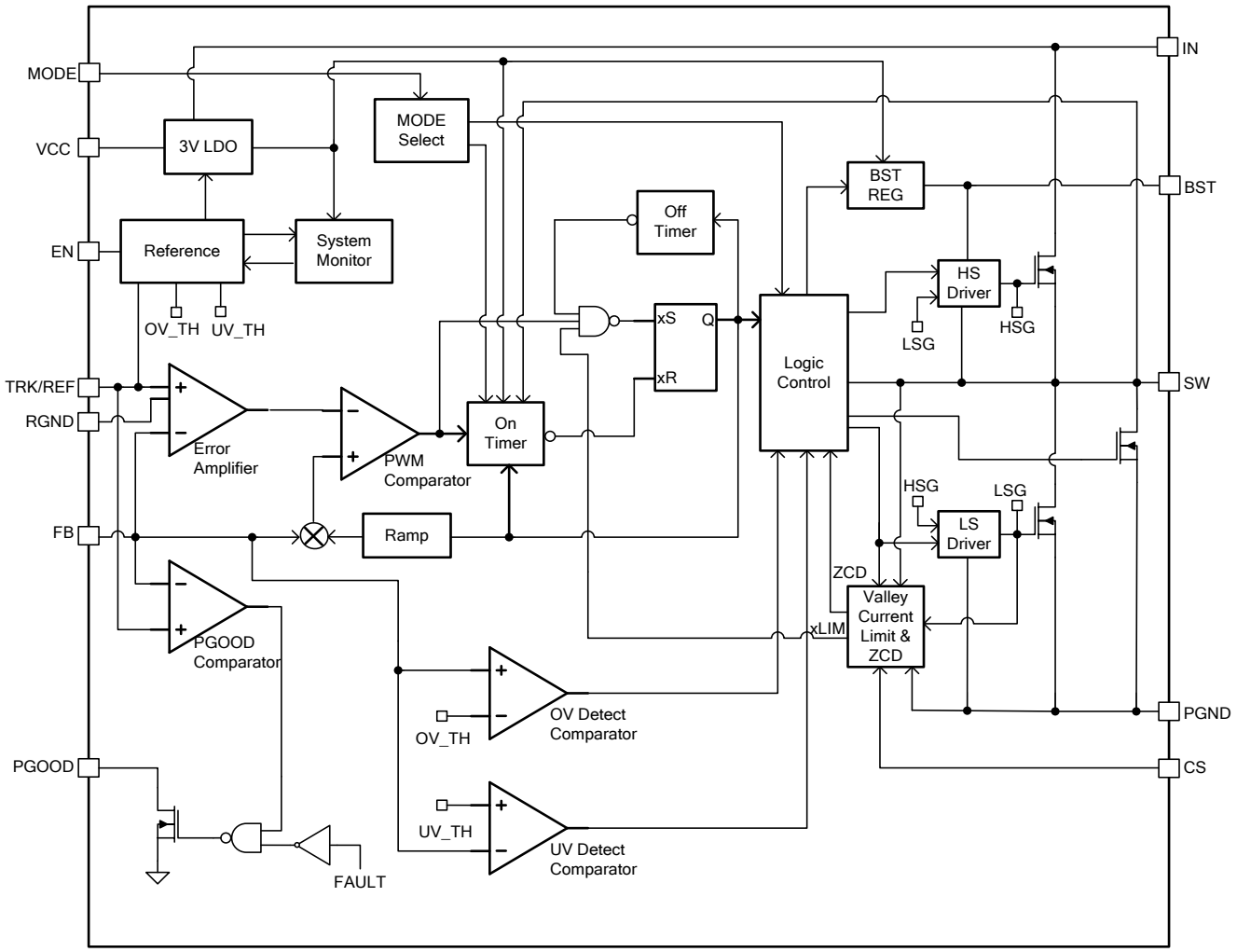

Figure 1: Functional Block Diagram

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OPERATION

COT Control

The MPQ8633B employs a constant-on-time (COT) control to achieve a fast load transient response. Figure 2 shows the details of the control stage of the MPQ8633B.

The operational amplifier (AMP) corrects any error voltage between FB and VREF. The MPQ8633B can use AMP to provide excellent load regulation over the entire load range in either forced continuous conduction mode (CCM) or pulse skip mode.

The dedicated RGND pin helps provide the feature of the differential output voltage remote sense. The pair of the remote sense trace should be kept in low impedance to achieve the best performance.

The MPQ8633B has an internal RAMP compensation to support a low ESR MLCC output capacitor solution. The adaptive internal RAMP is optimized so that the MPQ8633B is stable in the entire operating input and output voltage ranges with a proper design of the output L/C filter.

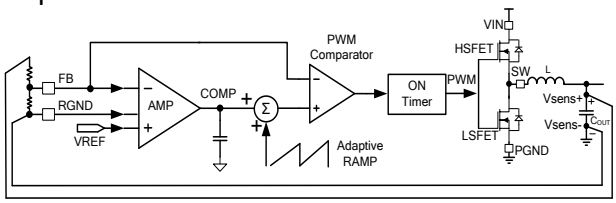

Figure 2: COT Control

PWM Operation

Figure 3 shows how the PWM signal is generated. AMP corrects any error between FB and REF and generates a fairly smooth DC voltage (COMP). The internal RAMP is superimposed onto COMP, which is compared with the FB signal. Whenever FB drops below the superimposed COMP, the integrated high-side MOSFET (HS-FET) is turned on. The HS-FET remains on for a fixed turn-on time. The fixed on time is determined by the input voltage, output voltage, and selected switching frequency. After the on period elapses, the HS-FET turns off. It turns on again when FB drops below the superimposed COMP. By repeating this operation, the MPQ8633B regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss. A dead short occurs between VIN and PGND if both the HS-FET and the LS-FET are turned on at the same time. This is called a shoot-through. To avoid a shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on period or the LS-FET off and the HS-FET on period.

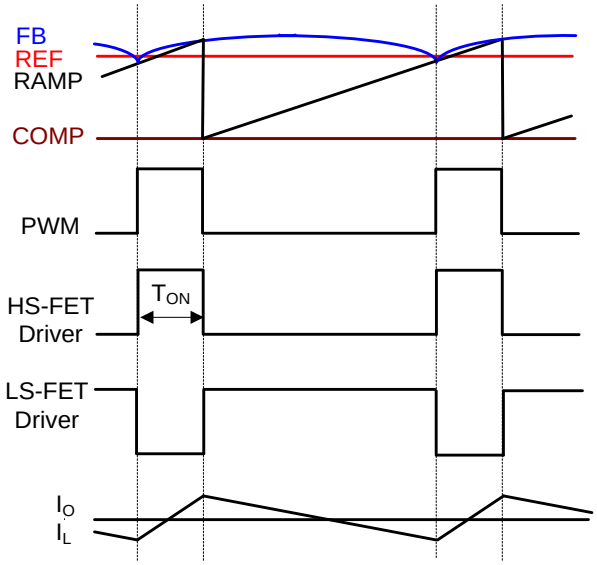

Figure 3: Heavy-Load Operation (PWM)

CCM Operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps (see Figure 3). The MPQ8633B can also be configured to operate in forced CCM operation when the output current is low (see the Mode Selection section on page 14 for details).

In CCM operation, the switching frequency is fairly constant (PWM mode), hence the output ripple remains almost constant throughout the entire load range.

Pulse Skip Operation

In light-load condition, the MPQ8633B can be configured to work in pulse skip mode to optimize efficiency. When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the MPQ8633B transitions from CCM to pulse skip mode if the MPQ8633B is configured in this

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way (see the Mode Selection section on page 14 for details).

Figure 4 shows pulse skip mode operation at light-load condition. When FB drops below the superimposed COMP, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until the inductor current reaches zero. In pulse skip mode operation, FB does not reach superimposed COMP when the inductor current approaches zero. The LS-FET driver turns into tri-state (high-Z) when the inductor current reaches zero. A current modulator takes over the control of the LS-FET and limits the inductor current to less than -1mA. Therefore, the output capacitors discharge slowly to PGND through the LS-FET. At light-load condition, the HS-FET is not turned on as frequently in pulse skip mode as it is in forced CCM. As a result, the efficiency in pulse skip mode is improved greatly compared to that in forced CCM operation.

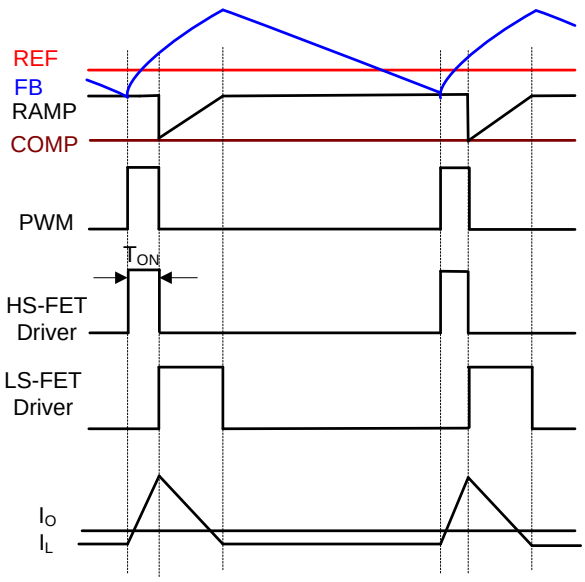

Figure 4: Pulse Skip in Light Load

As the output current increases from light load, the time period the current modulator regulates in becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches critical levels when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

Where F_{SW} is the switching frequency.

The MPQ8633B enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

The MPQ8633B can be configured to operate in forced CCM, even in light-load condition (see Table 1).

Mode Selection

The MPQ8633B provides both forced CCM operation and pulse skip mode operation in light-load condition. The MPQ8633B has three options for switching frequency selection. Selecting the operation mode under light-load condition and the switching frequency is done by choosing the resistance value of the resistor connected between MODE and AGND or VCC (see Table 1).

Table 1: MODE Selection

MODE	Light-Load Mode	Switching Frequency
VCC	Pulse skip	600kHz
243kΩ (±20%) to GND	Pulse skip	800kHz
121kΩ (±20%) to GND	Pulse skip	1000kHz
GND	Forced CCM	600kHz
30.1kΩ (±20%) to GND	Forced CCM	800kHz
60.4kΩ (±20%) to GND	Forced CCM	1000kHz

Soft Start (SS)

The minimum soft-start time is limited at 1ms. It can be increased by adding a SS capacitor between TRK/REF and RGND.

The total SS capacitor value can be determined with Equation (2) and (3):

$$C_{SS}(nF) = \frac{t_{ss}(ms) \times 36\mu A}{0.6(V)} \quad (2)$$

$$C_{SS} = C_{SS1} + C_{SS2} \quad (3)$$

where C_{SS2} is recommended to be minimum of 22nF.

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Output Voltage Tracking and Reference

The MPQ8633B provides an analog input pin (TRK/REF) to track another power supply or accept an external reference. When an external voltage signal is connected to TRK/REF, it acts as a reference for the MPQ8633B output voltage. The FB voltage follows this external voltage signal exactly, and the soft-start settings are ignored. The TRK/REF input signal can be in the range of 0.3V to 1.4V. During the initial start-up, the TRK/REF must reach at least 600mV first to ensure proper operation. After that, it can be set to any value between 0.3V and 1.4V.

Pre-Bias Start-Up

The MPQ8633B is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the HS-FET and LS-FET until the voltage on the TRK/REF capacitor exceeds the sensed output voltage at FB. Before the TRK/REF voltage reaches the pre-biased FB level, if the BST voltage (from BST to SW) is lower than 2.3V, the LS-FET is turned on to allow the BST voltage to be charged through VCC. The LS-FET is turned on for very narrow pulses, so the drop in the pre-biased level is negligible.

Output Voltage Discharge

When the MPQ8633B is disabled through EN, output voltage discharge mode is enabled. This causes both the HS-FET and the LS-FET to latch off. A discharge FET connected between SW and PGND is turned on to discharge the output voltage. The typical switch on resistance of this FET is about 80Ω. Once the FB voltage drops below 10%*REF, the discharge FET is turned off.

Current Sense and Over-Current Protection (OCP)

The MPQ8633B features an on-die current sense and a programmable positive current limit threshold.

The current limit is active when the MPQ8633B is enabled. During the LS-FET on state, the SW current (inductor current) is sensed and mirrored to CS with the ratio of G_{CS}. By using a resistor (R_{CS}) from CS to AGND, the V_{CS} voltage is proportional to the SW current cycle-by-cycle. The HS-FET is only allowed to turn on when V_{CS} is below the internal OCP voltage threshold (V_{OCP}) during the LS-FET on state to limit the SW valley current cycle-by-cycle.

Calculate the current limit threshold setting from R_{CS} with Equation (4):

$$R_{CS}(\Omega) = \frac{V_{OCP}}{G_{CS} \times (I_{LIM} - \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{2 \times L \times f_s})} \quad (4)$$

Where V_{OCP} = 1.2V, G_{CS} = 10µA/A, and I_{LIM} is the desired output current limit (A).

The OCP hiccup is active 3ms after the MPQ8633B is enabled. Once OCP hiccup is active, if the MPQ8633B detects the over-current condition for 31 consecutive cycles, or if FB drops below the under-voltage protection (UVP) threshold, it enters hiccup mode. In hiccup mode, the MPQ8633B latches off the HS-FET immediately, and latches off the LS-FET after ZCD is detected. Meanwhile, the TRK/REF capacitor is also discharged. After about 11ms, the MPQ8633B attempts to soft start automatically. If the over-current condition still remains after 3ms of running, the MPQ8633B repeats this operation cycle until the over-current condition disappears, and the output voltage rises back to the regulation level smoothly.

Negative Inductor Current Limit

When the LS-FET detects a -10A current, the MPQ8633B turns off the LS-FET for 200ns to limit the negative current.

Output Sinking Mode (OSM)

The MPQ8633B employs output sinking mode (OSM) to regulate the output voltage to the targeted value. When the FB voltage is higher than 104%*REF but is below the OVP threshold, OSM is triggered. During OSM operation, the LS-FET remains on until it reaches the -9A current limit. The LS-FET is then turned off momentarily for 200ns before turning on again. The MPQ8633B repeats this operation until FB drops below 102%*REF. The MPQ8633B exits OSM after 15 consecutive cycles of forced CCM.

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Over-Voltage Protection (OVP)

The MPQ8633B monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an over-voltage condition. This provides latch-off OVP mode.

If the FB voltage exceeds 116% of the REF voltage, the MPQ8633B enters latch-off OVP mode. The HS-FET latches off and PGOOD latches low until VCC or EN is recycled (turned off and turned on again). Meanwhile, the LS-FET remains on until it reaches the low-side negative current limit (NOCP). The LS-FET is then turned off momentarily for 200ns before turning on again. The MPQ8633B repeats this operation to attempt to bring down the output voltage. When the FB voltage drops below 50% of the REF voltage, the LS-FET is turned off for pulse skip mode and continues turning on for forced CCM operation. If FB rises higher than 116% of the REF voltage again, the LS-FET turns on again with NOCP until FB drops back below 50% of the REF voltage. The MPQ8633B needs EN or VIN to recycle to clear the OVP fault.

The OVP function is enabled after TRK/REF reaches 600mV.

Over-Temperature Protection (OTP)

The MPQ8633B has over-temperature protection (OTP). The IC monitors the junction temperature internally. If the junction temperature exceeds the threshold value (typically 160°C), the converter shuts off and discharges the TRK/REF capacitors. This is a non-latch protection. There is a hysteresis of about 30°C. Once the junction temperature drops to about 130°C, a soft start is initiated. The OTP function is effective once the MPQ8633B is enabled.

Output Voltage Setting and Remote Output Voltage Sensing

First, choose a value for R_{FB1}. Then R_{FB2} can be determined with Equation (5):

$$R_{FB2}(k\Omega) = \frac{V_{REF}}{V_O - V_{REF}} \times R_{FB1}(k\Omega) \quad (5)$$

To optimize the load transient response, a feed-forward capacitor (C_{FF}) is recommended to be placed in parallel with R_{FB1}. R_{FB1} and C_{FF} add an extra zero to the system, which improves loop response. R_{FB1} and C_{FF} are selected so that the zero formed by R_{FB1} and C_{FF} is located around 5kHz to 40kHz. Calculate this zero with Equation (6):

$$f_Z = \frac{1}{2\pi \times R_{FB1} \times C_{FF}} \quad (6)$$

Power Good (PGOOD)

The MPQ8633B has a power good (PGOOD) output. PGOOD is the open-drain of a MOSFET. Connect PGOOD to VCC or another external voltage source less than 3.6V through a pull-up resistor (typically 10kΩ). After applying the input voltage, the MOSFET turns on, so PGOOD is pulled to GND before TRK/REF is ready. After the FB voltage reaches 92.5% of the REF voltage, PGOOD is pulled high after a 0.8ms delay.

When the FB voltage drops to 80% of the REF voltage, or exceeds 116% of the nominal REF voltage, PGOOD is latched low. PGOOD can only be pulled high again after a new SS.

If the input supply fails to power the MPQ8633B, PGOOD is clamped low, even though PGOOD is tied to an external DC source through a pull-up resistor. The relationship between the PGOOD voltage and the pull-up current is shown in Figure 5.

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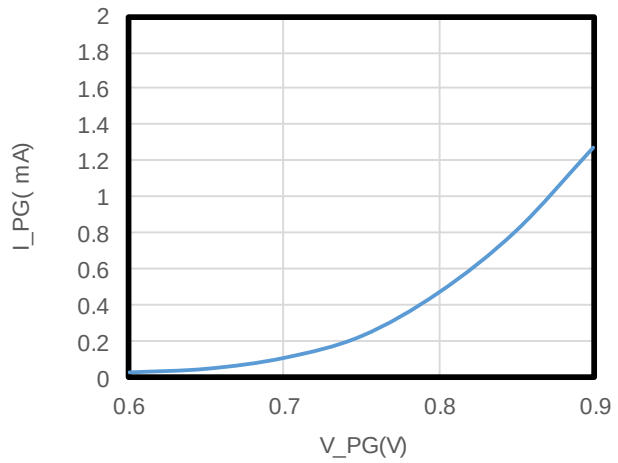

Figure 5: PGOOD Clamped Voltage vs. Pull-Up Current

Enable (EN) Configuration

The MPQ8633B turns on when EN goes high; the MPQ8633B turns off when EN goes low. EN cannot be left floating for proper operation. EN can be driven by an analog or digital control logic signal to enable or disable the MPQ8633B.

The MPQ8633B provides accurate EN thresholds, so a resistor divider from VIN to AGND can be used to program the input voltage, at which the MPQ8633B is enabled. This is highly recommended for applications where there is no dedicated EN control logic signal to avoid possible UVLO bouncing during power-up and power-down. The resistor divider values can be determined with Equation (7):

$$V_{IN_START}(V) = VIH_{EN} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (7)$$

Where VIH_{EN} is 1.22V, typically.

R_{UP} and R_{DOWN} should be chosen so that V_{EN} does not exceed 3.6V when VIN reaches the maximum value.

EN can also be connected to VIN directly through a pull-up resistor (R_{UP}). R_{UP} should be chosen so that the maximum current going to EN is 50μA. R_{UP} can be calculated with Equation (8):

$$R_{UP}(K\Omega) = \frac{V_{INMAX}(V)}{0.05(mA)} \quad (8)$$

Enable (EN) Thresholds

The MPQ8633B has two EN thresholds. One is the LDO EN rising threshold, and the other is the EN input rising threshold. During power-up, once EN reaches the LDO EN rising threshold (typically 0.7V), the internal LDO is enabled, and V_{CC} starts to increase. Once EN reaches the EN input rising threshold, the device is enabled and starts to switch.

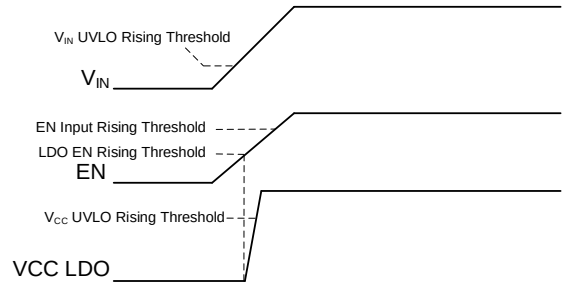

Figure 6: Power-Up Sequence with Internal LDO and Two EN Thresholds

Power Sequence with External VCC Bias

The MPQ8633B supports using an external 3.3V VCC bias (see Figure 7). When the external VCC bias is used, it is recommended to apply the external VCC bias before the V_{IN} UVLO rising threshold or LDO EN rising threshold is reached. If the external VCC bias is applied after the V_{IN} UVLO rising threshold and LDO EN rising threshold are reached, the LDO must output and provide power to the load, which is supposed to be supplied by the external VCC.

Depending on the load condition of the external VCC, the LDO might be overloaded until the external VCC bias is applied. It is recommended to power off the external VCC bias after the V_{IN} UVLO falling threshold or LDO EN falling threshold is reached.

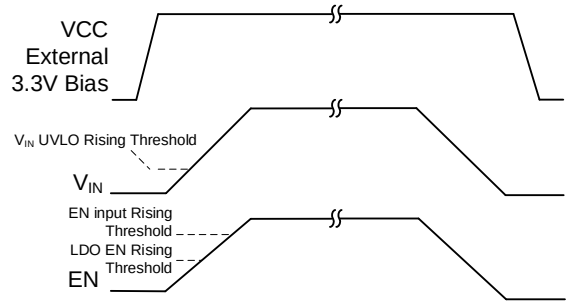

Figure 7: Power-Up Sequence with External VCC Bias

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APPLICATION INFORMATION

Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During layout, place the input capacitors as close to VIN as possible.

The capacitance can vary significantly with temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over a wide temperature range and offer very low ESR.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (9):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (9)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (10):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (10)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current. The input capacitor value determines the converter input voltage ripple. If there is an input voltage ripple requirement in the system, select an input capacitor that meets the specification.

Estimate the input voltage ripple with Equation (11):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (12)$$

Output Capacitor

The output capacitor maintains the DC output voltage. Use POSCAP or ceramic capacitors. Estimate the output voltage ripple with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (13)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

For simplification, the output ripple can be approximated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (15)$$

Inductor

The inductor supplies a constant current to the output load while being driven by the switching input voltage. A larger value inductor results in less ripple current and lower output ripple voltage, but also has a larger physical size, a higher series resistance, and a lower saturation current. Generally, select an inductor value that allows the inductor peak-to-peak ripple current to be 30% to 40% of the maximum switch current limit. Also design for a peak inductor current that is below the maximum switch current limit. Calculate the inductance value with Equation (16):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (16)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (17):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (17)$$

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best performance, refer to Figure 8 and follow the guidelines below.

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MPQ8633B.
3. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.
4. Place as many PGND vias as possible as close to PGND as possible to minimize both parasitic impedance and thermal resistance.
5. Place the VCC decoupling capacitor close to the device.
6. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
7. Place the BST capacitor as close to BST and SW as possible with 20 mil or wider traces to route the path. It is recommended to use a bootstrap capacitor 0.1µF to 1µF.
8. Place the REF capacitor close to TRK/REF to RGND.
9. Place via at least 10mm away from the positive side of the first input decoupling capacitor close to the IC if it must be placed on the PGOOD pad.
10. Place C_{OL} between the output sense lines and close to the device. It is recommended to use a 1nF to 100nF capacitor.
11. Do not place vias on the $V_{OSENSE+/-}$ trace.
12. Use a 10Ω to 49.9Ω resistor for R_{PG} and a 1nF capacitor for C_{PG}.
13. It is recommended for the feed-forward resistor (R_{FF}) to be 1/10 of the top feedback resistor (R_{FB1}).

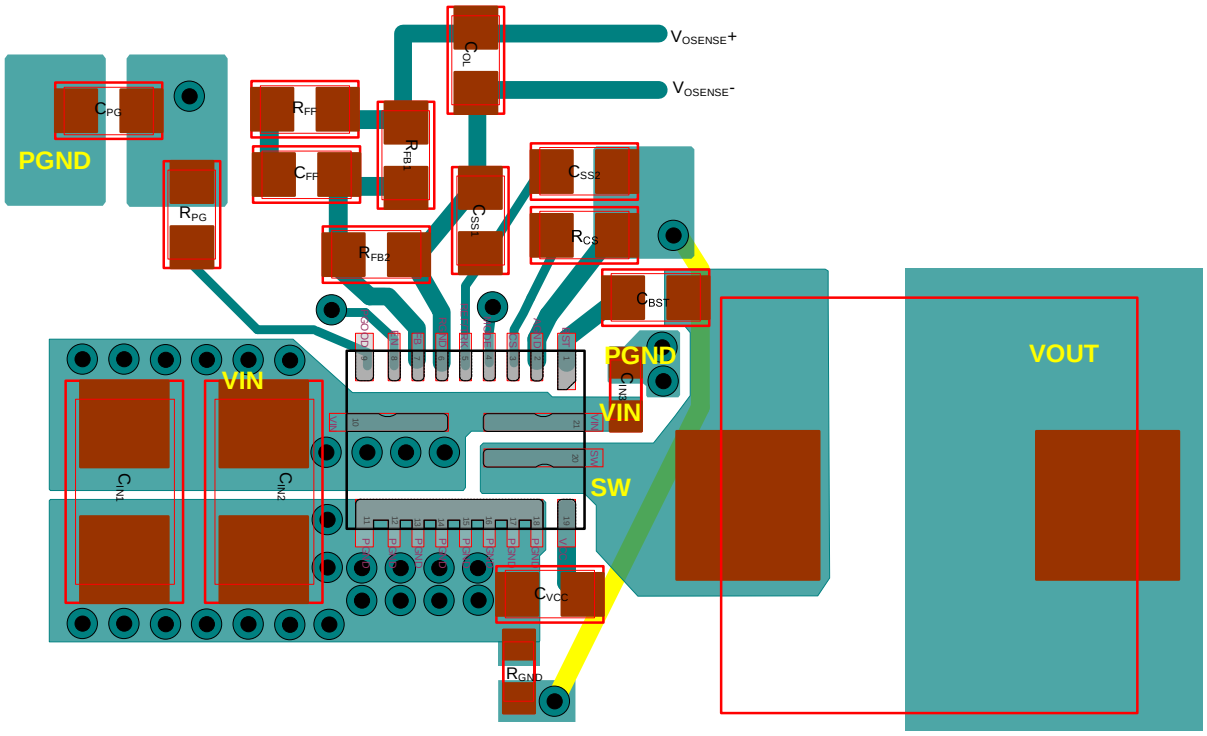

Figure 8: Recommended PCB Layout

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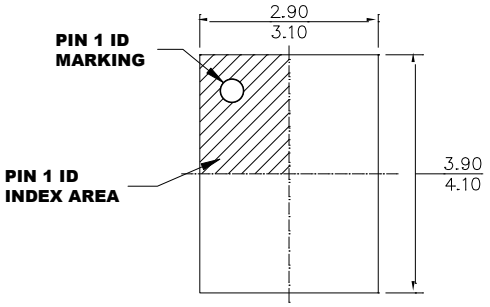
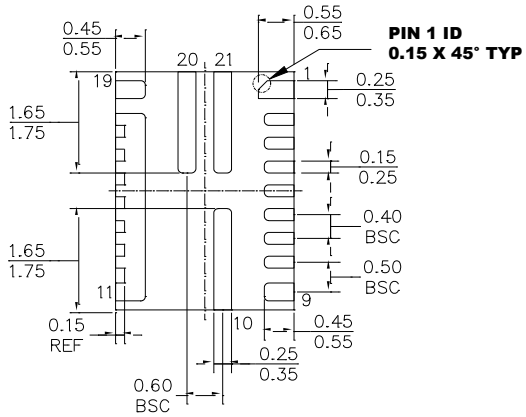
PACKAGE INFORMATION

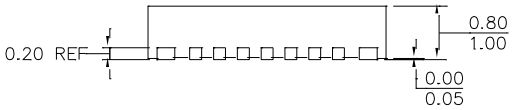
QFN-21 (3mmx4mm)



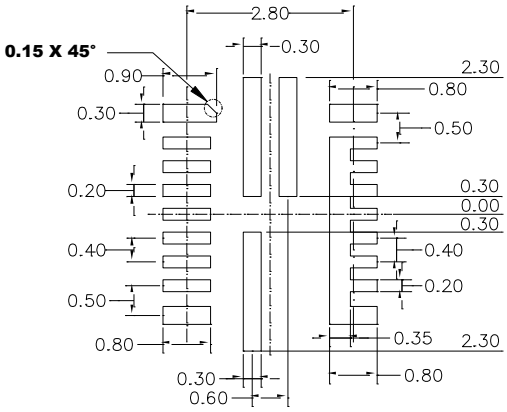
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERN OF PIN1,9,10,11,19,20 AND 21 HAVE THE SAME WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	07/27/2016	Initial Release	-
1.01	08/03/2017	Updated and edited the Electrical Characteristics table	All
1.02	03/01/2018	Updated the PG low level output voltage parameter	6
		Updated the PG Clamped Voltage vs. Current curve	15
1.03	11/2/2018	Added more applications to the Applications section	1
		Updated the plot scale for V_{OUT} Load Regulation	7
		Added Equation (3)	14
1.1	3/26/2024	Updated Typical Application section (designs on PGOOD, VCC, FB, and RGND): • Added R_{PG} and C_{PG} to PGOOD • Added R_{GND} to VCC • Added R_{FF} to FB • Added C_{OL} to from R_{FB1} to RGND	2
		Updated Absolute Maximum Ratings section: • Deleted $V_{SW(DC)}$, V_{SW} (25ns), V_{SW} (25ns), and V_{BST} • Added V_{IN} - V_{SW} (DC), V_{IN} - V_{SW} (25ns), V_{SW} (DC), V_{SW} (25ns), and V_{BST}, V_{BST} - V_{SW} (25ns) • Updated Recommended Operating Conditions: ○ $V_{IN(DC)}$ - $V_{SW(DC)}$, $V_{SW(DC)}$ • Updated Thermal Resistance (5) to Thermal Resistance (4) • Deleted the original note 4; note 5 became note 4	4
		Updated Notes 6 and 7 to Notes 5 and 6, respectively	5–6
		Updated the Output Voltage Setting and Remote Output Voltage Sensing section by changing the fz range from “20~60kHz” to “5kHz to 40kHz”	16
		• Added the Enable (EN) Thresholds section and the Power Sequence with External VCC Bias section • Added Figure 6 and Figure 7	17
		Updated the PCB layout Guidelines section: • Deleted step 10: “Place the OSENSE capacitor in between the output sense lines and close to the device.” • Added step 10. “Place C_{OL} between the output sense lines and close to the device. It is recommended to use a 1nF to 100nF capacitor." • Added step 11: “Do not place vias on the $V_{OSENSE+/-}$ trace.” • Added step 12: “Use a 10Ω to 49.9Ω for resistor for R_{PG} and a 1nF capacitor for C_{PG}." • Added step 13: “It is recommended for the feed-forward resistor (R_{FF}) to be 1/10 of the top feedback resistor (R_{FB1}).” • Updated Figure 6 to Figure 8 and made additional changes	20

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