NB650/NB650H

High-Effeciency, Fast-Transient, 6A, 28V Synchronous Step-Down Converters with 2-Bit VID

The Future of Analog IC Technology

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO NB650A

DESCRIPTION

The NB650/NB650H is fully-integrated, high-frequency, synchronous, rectified, step-down, switch-mode converters with dynamic-output–voltage control. It offers a very compact solution to achieve 6A of continuous output current over a wide input supply range, and has excellent load and line regulation. The NB650/NB650H operates at high efficiency over a wide output-current–load range.

Constant-On-Time control mode provides fast transient response and eases loop stabilization.

2-bit VID inputs support changing the output voltage on-the-fly.

Full protection features include short-circuit protection, over-current protection, over-voltage protection, under-voltage protection, and thermal shut down.

The NB650/NB650H requires a minimal number of readily-available standard external components, and is available in a space-saving 3mm×4mm QFN17 package.

FEATURES

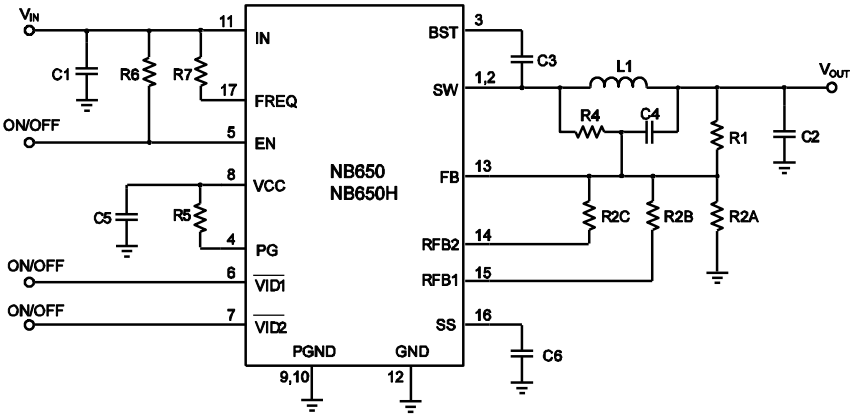
- Wide 4.5V-to-28V Operating Input Range
- 6A Output Current
- Internal 50mΩ High-Side, 18mΩ Low-Side Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- 1% Reference Voltage
- Programmable Soft-Start Time
- 2-bit VID Input
- Soft Shutdown
- Frequency Programmable from 150kHz to 1MHz
- SCP, OCP, OVP, UVP, and Thermal Shutdown
- Optional OCP Protection: Latch-Off Mode (NB650) and Hiccup Mode (NB650H)
- Output Adjustable from 0.6V to 13V
- Available in QFN17 (3mm×4mm) Package

APPLICATIONS

- Notebook Systems and I/O Power
- Networking Systems
- Digital Set Top Boxes
- Flat-Panel Televisions and Monitors
- Distributed Power Systems

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance. “MPS” and “The Future of Analog IC Technology” are Registered Trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION （FOR NOTEBOOK）



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

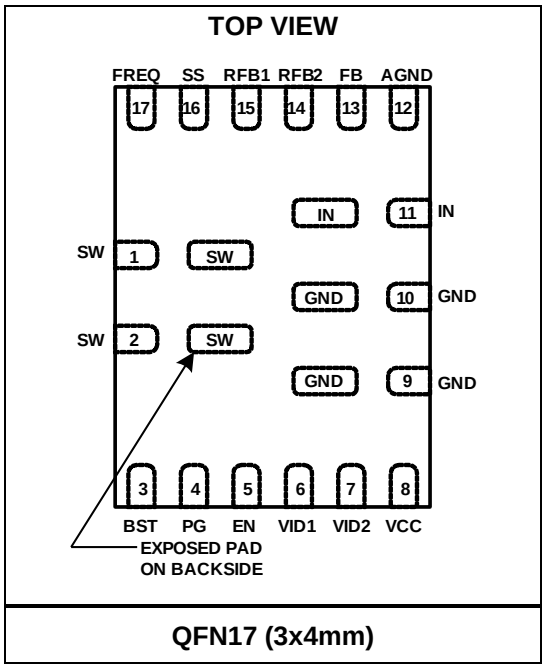
NOT RECOMMENDED FOR NEW DESIGNS, REFER TO NB650A

ORDERING INFORMATION

Part Number	Package	Top Marking
NB650GL*	QFN17 (3 x 4mm)	NB650
NB650HGL**		NB650H

* For Tape & Reel, add suffix –Z (e.g. NB650GL–Z)
** For Tape & Reel, add suffix –Z (e.g. NB650HGL–Z)

PACKAGE REFERENCE



QFN17 (3x4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 28V
V_{SW} ..... -0.3V to V_{IN} + 0.3V
V_{SW} ..... -3V to V_{IN} + 3V for <30ns
V_{BST} ..... V_{SW} + 6V
All Other Pins..... -0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
QFN17 ....2.4W
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.5V to 22.5V
Output Voltage V_{OUT}..... 0.6V to 13V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}
QFN17(3 x 4mm)	52	11 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		0		μA
Input Supply Current (Quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} =0.65V		400		μA
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	1	μA
Current Limit	I_{LIMIT}	t_{ON}>200ns	8	10		A
One-Shot On Time	t_{ON}	R_{FREQ}=200kΩ, V_{OUT}=1.2V		200		ns
Minimum Off Time	t_{OFF}	R_{FREQ}=200kΩ		100		ns
Fold-back Off Time(5)	t_{FB}	ILIM=1		1.2		μs
OCP hold-off time(5)	t_{OC}	ILIM=1		50		μs
Feedback Voltage	V_{FB}		594	600	606	mV
Feedback Current	I_{FB}	V_{FB} = 600mV		10	100	nA
Soft Start Charging Current	I_{SS}	V_{SS}=0V		10		μA
Soft Stop Charging Current	I_{SS}	V_{SS}=0.6V		10		μA
EN Input Low Voltage	VIL_{EN}				0.4	V
EN Input High Voltage	VIH_{EN}		2			V
EN Input Current	I_{EN}	V_{EN} = 2V		1.5		μA
		V_{EN} = 0V		0		
OVP Feedback Threshold	V_{FB-OV}			0.8		V
UVP Feedback Threshold(5)	V_{FB-UV}			0.4		V
VID Inputs Low Voltage	VIL_{VID}				0.4	V
VID Inputs High Voltage	VIH_{VID}		2			V
VID Inputs Current	I_{VID}			0		μA
Equivalent FB Slew Rate During VID On-The-Fly(5)	SR_{FB}			±20		mV/μs
VID Switch On Resistance(5)	VID_{RDS-ON}			100		Ω
Power Good Rising Threshold	PG_{Vth-Hi}			0.9		V_{FB}
Power Good Falling Threshold	PG_{Vth-Lo}			0.85		V_{FB}
Power Good Delay	PG_{Td}			0.5		ms
Power Good Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
Power Good Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V			10	nA
Standby Mode Delay Time(5)	$t_{STANDBY}$			12		μs
V_{IN} Under Voltage Lockout Threshold Rising	$INUV_{Vth}$			4		V
V_{IN} Under Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			800		mV
Thermal Shutdown(5)	T_{SD}			150		°C

Note:

5) Not tested. Not guaranteed.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.

Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

PIN FUNCTIONS

QFN17 Pin #	Name	Description
1,2	SW	Switch Output. Connect using wide PCB traces.
3	BST	Bootstrap. Requires a capacitor between SW and BST to form a floating supply across the high-side switch driver.
4	PG	Power Good. Output is an open drain and is high if the output voltage exceeds 90% of the nominal voltage. There is a delay from FB≥90%×V_{ref} to PG goes high.
5	EN	EN=1 to enable. For automatic start-up, connect to VIN with a 100kΩ resistor.
6,7	$\overline{VID1}$ $\overline{VID2}$	VID inputs. Control signals for the output-voltage scaling. Acts as the control signals for the internal VID switches. Usually uses an external resistor in parallel with the low-side FB resistor. Changing the VID ON/OFF state changes the FB divider scaling and result in different output voltages.
8	VCC	Internal LDO output. The power supply of the internal control circuits. Decouple with 1μF capacitor.
9,10	GND	System Ground. The reference ground of the regulated output voltage. Layout requires extra care.
11	IN	Supply Voltage. Operates from a 4.5V-to-28V input rail. Requires C1 to decouple the input rail. Connect using wide PCB traces.
12	AGND	Analog Ground.
13	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage.
14,15	RFB2 RFB1	Drain of the internal VID switches. Typically uses an external resistor in parallel with the low-side FB resistor along with the internal VID switch to change the ON/OFF state of the VID switching to change the FB divider scaling and result in different output voltages.
16	SS	Soft-Start. Connect an external capacitor to program the soft-start time for the switch-mode regulator.
17	FREQ	Frequency Set during CCM. The input voltage and the frequency-set resistor between the IN and FREQ pin determines the ON period. For best results, use an ON period longer than 200ns.

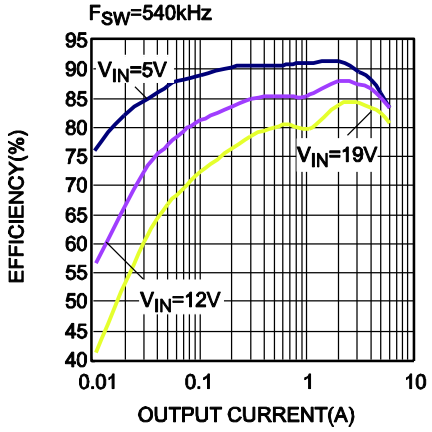
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT} =1.05V, L=1µH, T_A=+25°C, unless otherwise noted.

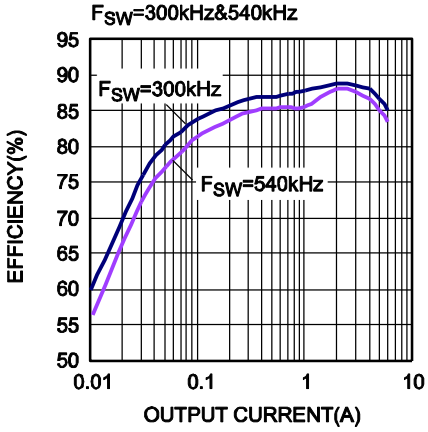
Efficiency

F_{SW}=540kHz



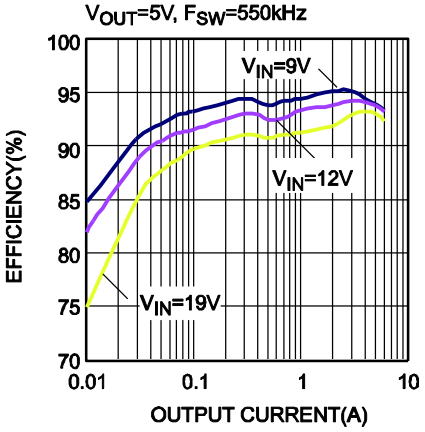
Efficiency

F_{SW}=300kHz&540kHz

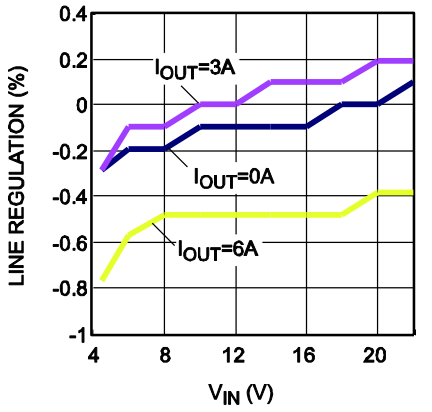


Efficiency

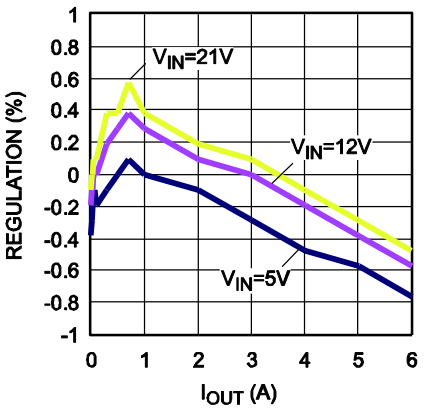
V_{OUT}=5V, F_{SW}=550kHz



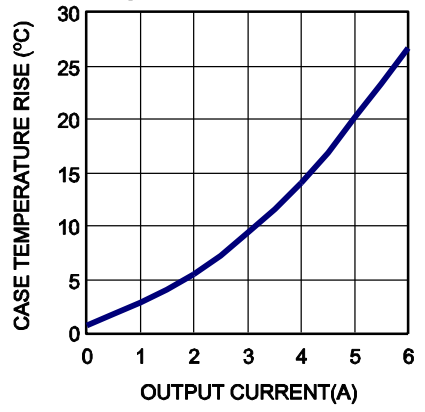
Line Regulation



Load Regulation

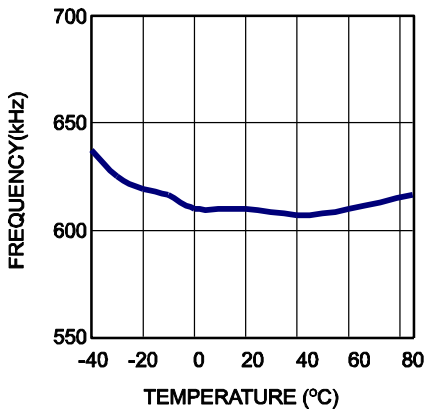


Case Temperature Rise vs. Output Current



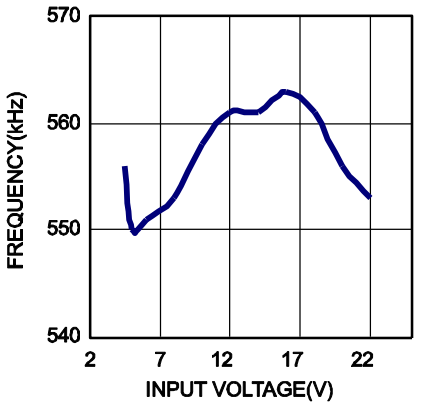
Frequency vs. Temperature

I_{OUT}=6A

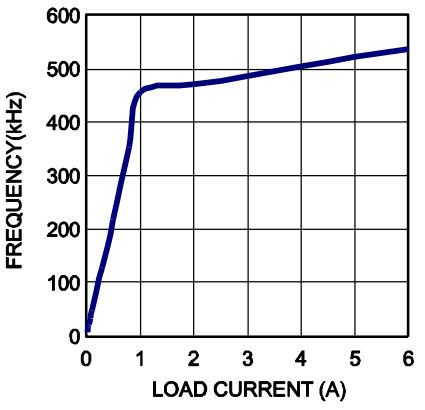


Frequency vs. V_{IN}

I_{OUT}=6A



Frequency vs. Load Current

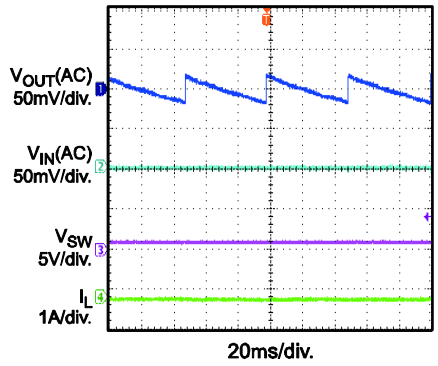


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

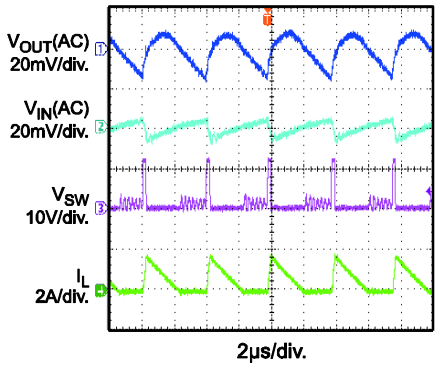
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT} =1.05V, L=1µH, T_A=+25°C, unless otherwise noted.

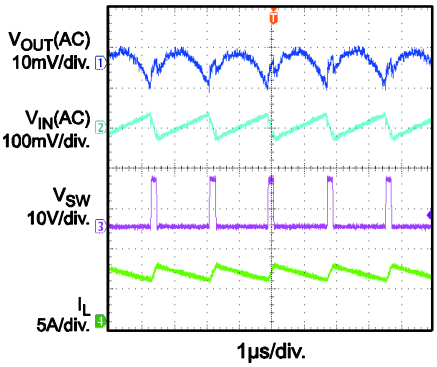
Input & Output Ripple
I_{OUT} = 0A



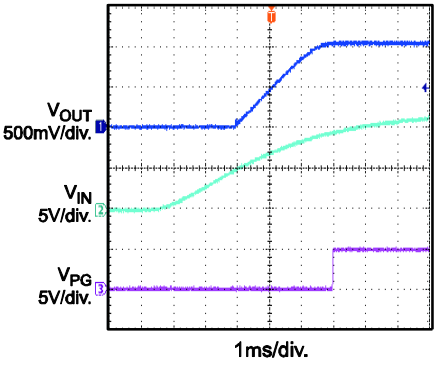
Input & Output Ripple
I_{OUT} = 0.5A



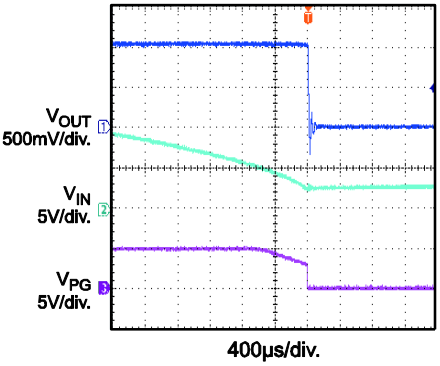
Input & Output Ripple
I_{OUT} = 6A



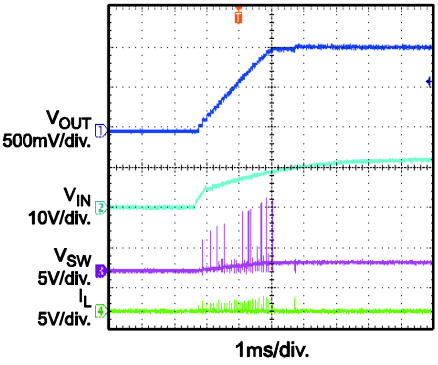
Power Good Through V_{IN} Start-Up
I_{OUT} = 6A



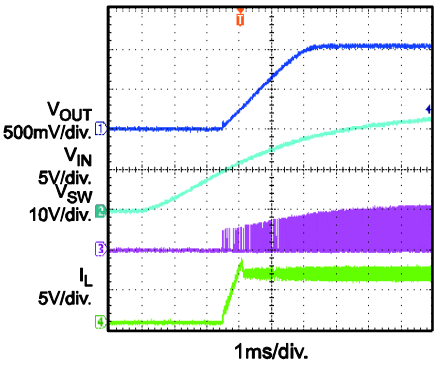
Power Good Through V_{IN} Shutdown
I_{OUT} = 6A



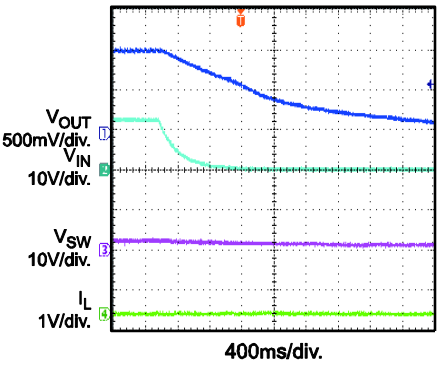
Start-Up Through V_{IN}
I_{OUT} = 0A



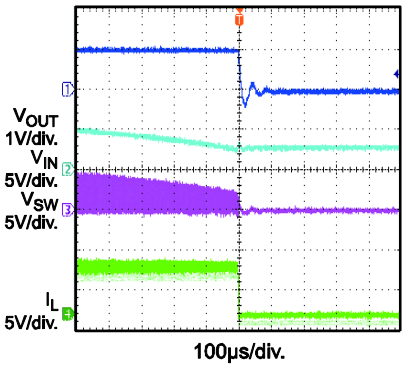
Start-Up Through V_{IN}
I_{OUT} = 6A



Shutdown Through V_{IN}
I_{OUT} = 0A



Shutdown Through V_{IN}
I_{OUT} =6A

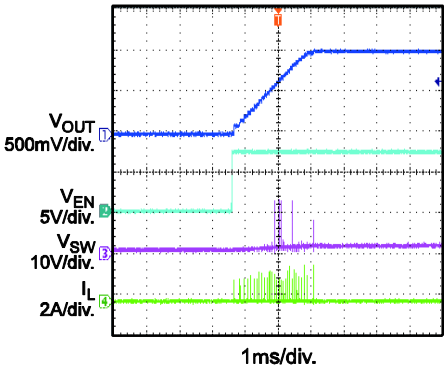


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

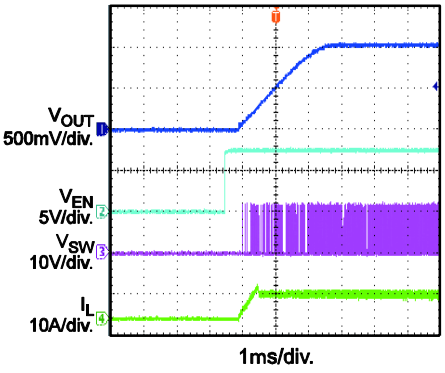
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT} =1.05V, L=1µH, T_A=+25°C, unless otherwise noted.

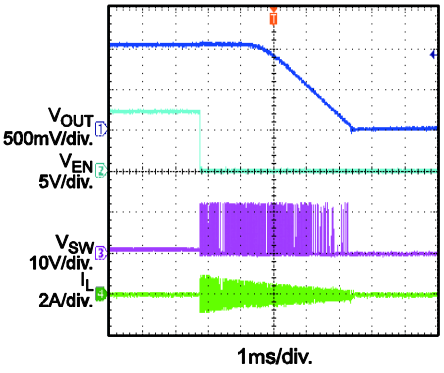
Start-Up Through EN
I_{OUT} = 0A



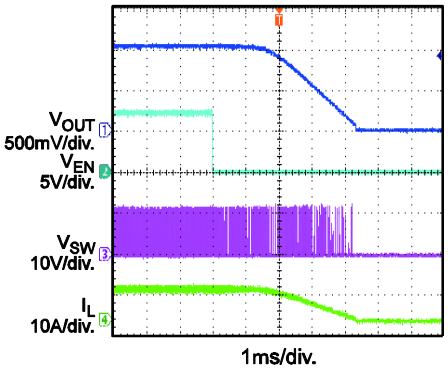
Start-Up Through EN
I_{OUT} = 6A



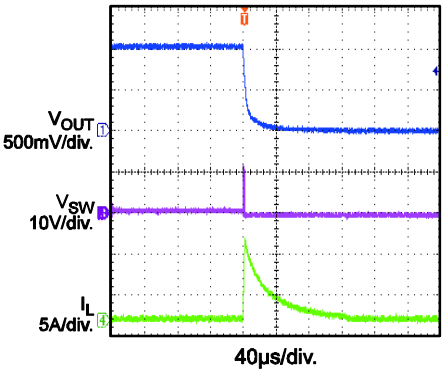
Shutdown Through EN
I_{OUT} = 0A



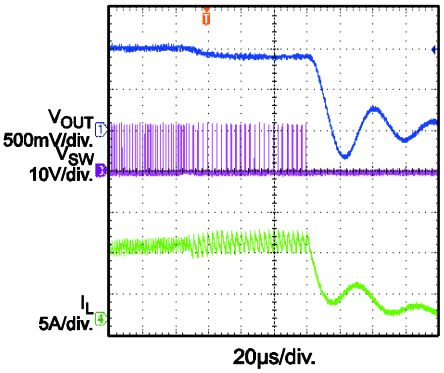
Shutdown Through EN
I_{OUT} = 6A



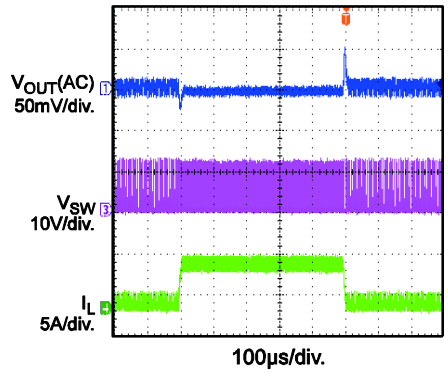
Short Circuit Protection
NB650, Latch-Off Version



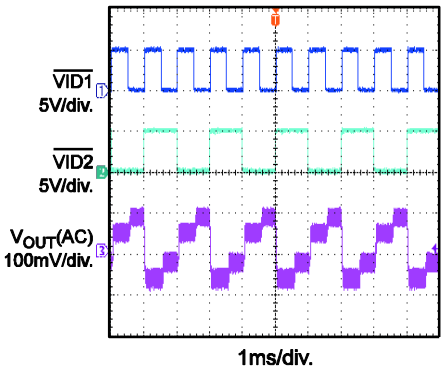
OCP Protection
NB650, Latch-Off Version



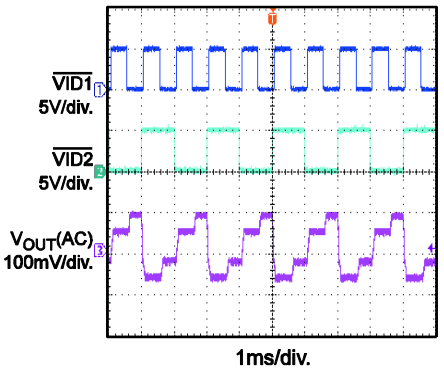
Transient
I_{OUT} = 0.6A-5.4A@2.5A/µs,
F_{SW} = 530kHz, C_{OUT} = 3x22µF



VID On-the-fly
I_{OUT} = 0.3A□
F_{VID1} = 1kHz, F_{VID2} = 0.5kHz,
V_{OUT} = 1.05V/1.1V/1.15V/1.2V



VID On-the-fly
I_{OUT} = 6A□
F_{VID1} = 1kHz, F_{VID2} = 0.5kHz,
V_{OUT} = 1.05V/1.1V/1.15V/1.2V



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

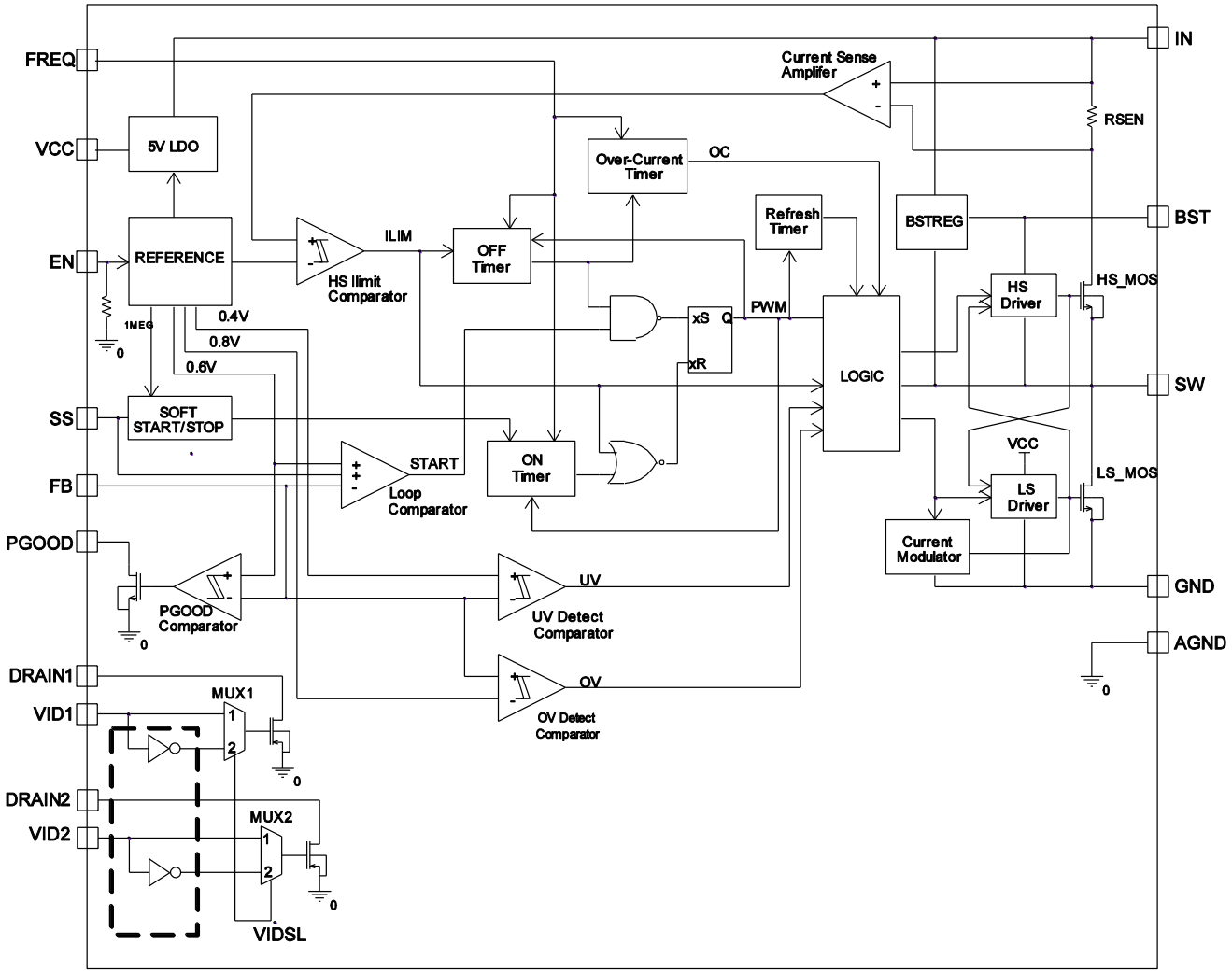


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

OPERATION

PWM Operation

The NB650/NB650H is a fully-integrated, synchronous, rectified, step-down, switch-mode converter with dynamic output voltage control. It offers a very compact solution to achieve a 6A continuous output current over a wide input supply range, with excellent load and line regulation. The NB650/NB650H operates at high efficiency over a wide output current load range.

Constant-on-time (COT) provides a fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the feedback voltage (V_{FB}) falls below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The input voltage and the frequency-set resistor determine the ON as follows:

$$t_{ON}(ns) = \frac{9.6 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} + t_{DELAY1}(ns) \quad (1)$$

Where t_{DELAY1} is the 20ns delay of a comparator in the t_{ON} module.

For best results, select $t_{ON} \geqslant$120ns.

After the ON period elapses, the HS-FET turns off to enter the OFF state. The part turns ON again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is OFF to minimize conduction loss. There is a dead short between input and GND (shoot-through) if both HS-FET and LS-FET turn on at the same time. An internally-generated dead-time (DT) between HS-FET OFF and LS-FET ON, or LS-FET OFF and HS-FET OFF avoids shoot-through.

Heavy-Load Operation

As shown in Figure 2, the HS-FET and LS-FET repeatedly turn on/off when the output current is high, and the inductor current never goes to zero. It's called continuous-conduction-mode (CCM) operation. In CCM operation, the switching frequency (f_{SW}) is fairly constant.

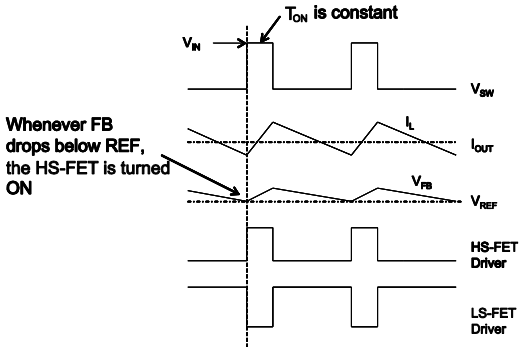


Figure 2: Heavy-Load Operation

Light-Load Operation

When the load current decreases, the NB650/NB650H automatically reduces the switching frequency to maintain high efficiency. Figure 3 shows the light-load operation. V_{FB} does not reach V_{REF} when the inductor current approaches zero. As the output current drops from heavy-load condition, the inductor current also decreases and eventually approaches zero. The LS-FET driver enters a tri-state (high-Z) whenever the inductor current reaches zero. A current modulator takes control of the LS-FET and limits the inductor current to less than 600μA to slowly discharge the output capacitors to GND through LS-FET as well as R1 and R2A, R2B and R2C. The HS-FET does not turn ON as frequently as in heavy-load condition. As a result, the efficiency at light-load condition increases greatly. This operation mode is also called skip mode.

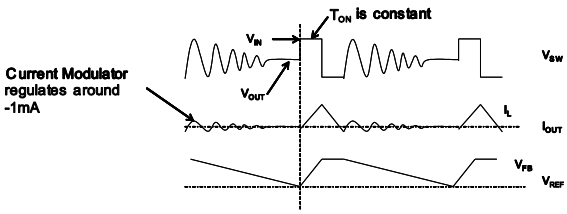


Figure 3: Light-Load Operation

As the output current increases from the light-load condition, the time period within which the current modulator regulates becomes shorter.

As the part exits light-load mode, the HS-FET turns on more frequently to increase the switching frequency. The output current reaches critical when the current modulator time is zero. The

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

following equation determines the critical level of the output current:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (2)$$

When the output current exceeds the critical level, light load mode turns into PWM mode, and the switching frequency stays fairly constant over the output current range.

Switching Frequency

The NB650/NB650H uses constant-on-time (COT) control, and has no dedicated internal oscillator. The input voltage is feed-forwarded to the on-time one-shot timer through the resistor R_{FREQ}. The duty ratio is kept as V_{OUT}/V_{IN}. Hence, the switching frequency is fairly constant over the input voltage range. The switching frequency can be set as follows:

$$f_{SW}(kHz) = \left[\left(\frac{9.6 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} + t_{DELAY1}(ns) \right) \times \frac{V_{IN}(V)}{V_{OUT}(V)} + t_{DELAY2}(ns) \right]^{-1} \times 10^6 \quad (3)$$

Where t_{DELAY2} is another comparator delay of about 40ns.

Frequency vs. R_{FREQ}

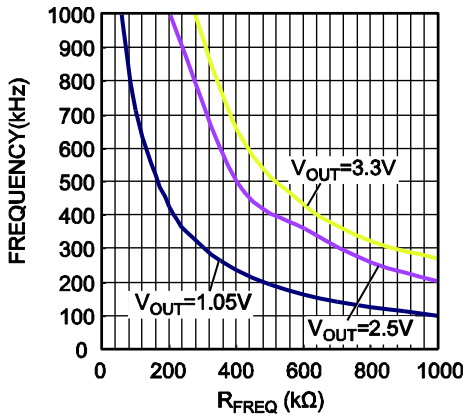


Figure 4: Plot of V_{OUT} as a Function of R_{FREQ} and the Frequency

NB650/NB650H is optimized to operate at high switching frequencies at high efficiency. Higher switching frequencies allow for smaller LC filter components to reduce system PCB space.

Jitter and FB Ramp Slope

Figure 5 and Figure 6 show jitter in both PWM and skip modes. When there is noise in the V_{FB} downward slope, the ON time of HS-FET deviates from its intended level and produces jitter. There is a relationship between a system's stability and the steepness of the V_{FB} ripple's downward slope: The steepness of the V_{FB} ripple's slope dominates in noise immunity. The magnitude of the V_{FB} ripple doesn't directly affect the noise immunity.

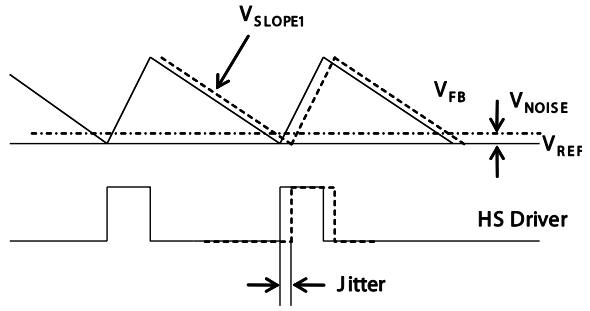


Figure 5: Jitter in PWM Mode

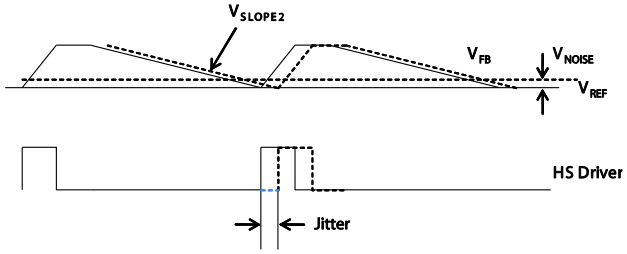


Figure 6: Jitter in Skip Mode

Ramp with Large ESR Cap

When using POSCAPs or other types of capacitors with larger ESR as output capacitors. the ESR ripple dominates the output ripple, and the slope on the FB is ESR-related. Figure 7 shows an equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit. The application section includes design steps for large ESR capacitors.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

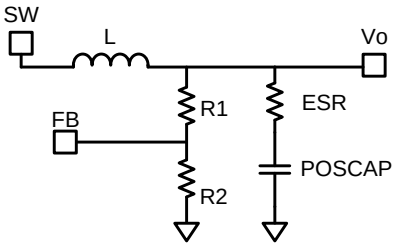


Figure 7: Simplified Circuit in PWM Mode without External Ramp Compensation

To realize the stability without the use of an external ramp, select an ESR value as follows:

$$R_{ESR} \geq \frac{\frac{t_{SW}}{0.7\times\pi}+\frac{t_{ON}}{2}}{C_{OUT}} \quad (4)$$

Where t_{SW} is the switching period.

Ramp with Small ESR Capacitor

The ESR ripple when using ceramic output capacitors is not high enough to stabilize the system and requires an external compensation ramp. The application section includes a description of designing with small ESR capacitors.

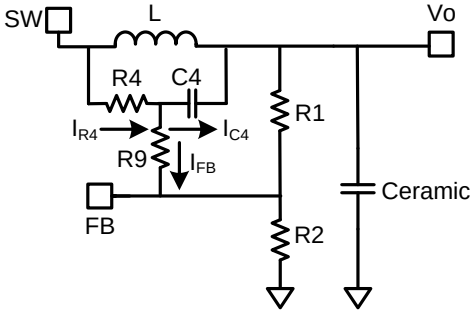


Figure 8: Simplified Circuit in PWM Mode with External Ramp Compensation

Figure 7 shows a simplified equivalent circuit in PWM mode with the HS-FET OFF and an external ramp compensation circuit (R4, C4). The external ramp is derived from the inductor ripple current. If one chooses C4, R9, R1 and R2 to meet the following condition:

$$\frac{1}{2\pi\times f_{SW}\times C_4} < \frac{1}{5}\times\left(\frac{R_1\times R_2}{R_1+R_2}+R_9\right) \quad (5)$$

Where:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (6)$$

And R2 is the equivalent resistor from FB to GND that varies with VID input, the ramp on the V_{FB} can then be estimated as:

$$V_{RAMP} = \frac{V_{IN}-V_O}{R_4\times C_4}\times t_{ON}\times\frac{R_1 // R_2}{R_1 // R_2 + R_9} \quad (7)$$

Usually R9 is set to 0Ω, then equation 7 can be simplified as:

$$V_{RAMP} = \frac{(V_{IN}-V_O)\times\tau_{ON}}{R4\times C4} \quad (8)$$

The downward slope of the V_{FB} ripple then follows

$$V_{SLOPE1} = \frac{-V_{RAMP}}{t_{off}} = \frac{-V_{OUT}}{R_4\times C_4} \quad (9)$$

As shown in equation 8, if there is instability in PWM mode, we can reduce either R4 or C4. If C4 can not be reduced further due to limitations from equation 5, then we can only reduce R4. For a stable PWM operation, the V_{slope1} should be designed as follows.

$$-V_{slope1} \geq \frac{\frac{t_{SW}}{0.7\times\pi}+\frac{t_{ON}}{2}-R_{ESR}C_{OUT}}{2\times L\times C_{OUT}}V_{OUT}+\frac{Io\times10^{-3}}{t_{SW}-t_{on}} \quad (10)$$

Where I_O is the load current.

In skip mode, the downward slope of the V_{FB} ripple is almost the same with or without the external ramp. Figure 9 shows the simplified circuit of the skip mode when both HS-FET and LS-FET are off.

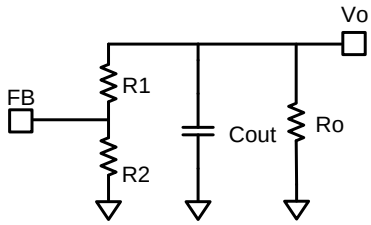


Figure 9: Simplified Circuit in Skip Mode

The downward slope of the V_{FB} ripple in skip mode can be determined as:

$$V_{SLOPE2} = \frac{-V_{REF}}{((R_1+R_2)//Ro)\times C_{OUT}} \quad (11)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

Where R_O is the equivalent load resistor.

As described in Figure 6, V_{SLOPE2} in skip mode is smaller than V_{SLOPE1} in PWM mode, so the jitter in the skip mode is larger. For less jitter during ultra-light–load conditions, select smaller V_{FB} resistors, though at the cost of light-load efficiency.

VID Input

Typically, R1 and R2 set the output voltage with V_{FB}=0.6V. R2, in this case, is a combination of R2A, R2B, and R2C depends on the VID, which is active low. The NB650/NB650H can dynamically track VID codes as they change. As a result, the converter output voltage can change without the need to reset either the controller or the value of R1 and R2A. As shown in Figure 1, R2B and R2C are parallel with R2A. The equivalent value of R2 can change due to different VID codes. One can get four V_{OUT} values depending on the VID codes with the details in the application information. The VID logic and equivalent R2s are shown in Table 1.

Table 1: VID Logic

$\overline{VID2}$	$\overline{VID1}$	R2
1	1	$R_2 = R_{2A}$
1	0	$R_2 = R_{2A} // R_{2B}$
0	1	$R_2 = R_{2A} // R_{2C}$
0	0	$R_2 = R_{2A} // R_{2B} // R_{2C}$

Enable Control

The NB650/NB650H has a dedicated Enable control pin (EN). Pulling this pin high or low enables or disables the IC. Tie EN to V_{IN} through a resistor for automatic start-up.

Soft Start/Stop

The NB650/NB650H employs a soft-start/stop (SS) mechanism to ensure smooth output during power-up and power shutdown. When the EN pin goes high, an internal current source (10μA) charges up the SS capacitor. The SS capacitor voltage then acts as the V_{REF} voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage reaches the same level as the REF voltage, it continues ramping up while the REF voltage becomes the reference to the PWM comparator. At this point, the soft-start finishes and it enters steady-state operation.

When the EN pin goes low, a 10μA internal current source discharges the SS capacitor. Once the SS voltage reaches the REF voltage, acts as the reference to the PWM comparator.

The output voltage decreases smoothly with the SS voltage until it reaches zero level. Determine the SS capacitor as follows:

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (12)$$

If the output capacitors have large capacitance values, avoid setting a short SS time. Use a minimum value of 4.7nF if the output capacitance value exceeds 330μF.

Power Good

The NB650/NB650H has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to V_{CC} or another voltage source through a resistor (e.g. 100kΩ). The MOSFET turns ON after the application of the input voltage so that the PG pin is pulled to GND before the SS is ready. After the FB voltage reaches 90% of the reference voltage, the PG pin is pulled high after a delay.

The PG delay is determined as follows:

$$t_{PG}(ms) = \frac{4 \times t_{SS}(ms)}{9} \quad (13)$$

When the FB voltage drops to 90% of the reference voltage, the PG pin is pulled low.

Over-Current Protection and Short-Circuit Protection

The NB650/NB650H has cycle-by-cycle over-current limit control. The inductor current is monitored during the ON state. Once the inductor current hits the current limit, the HS-FET turns off. At the same time, the over-current protection (OCP) timer starts. The OCP timer is set as 50μs. If the current limit is hit for every cycle within that 50μs period, then OCP will trigger.

When the output is shorted to ground, the device hits its current limit and the FB voltage is less than 0.4V. The device treats this as a dead-short

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

on the output and triggers OCP immediately. This is short circuit protection (SCP).

Under OCP/SCP condition, NB650 will latch off. The converter needs power cycle to restart. NB650H will try to recover from OCP/SCP fault with hiccup mode. That means in OCP/SCP protection, the NB650H will disable the output power stage, discharge soft-start capacitor and then automatically try to start again. If the over-current condition still holds after soft-start ends, the NB650H repeats this operation cycle till over-current fault is removed and output rises back to regulation level.

Over/Under-Voltage Protection

The NB650/NB650H monitors the output voltage through the FB voltage to detect overvoltage and under voltage on the output. When the FB voltage exceeds 0.8V, the over-voltage protection (OVP) triggers. Once OVP triggers, the LS-FET is always on while the HS-FET is always off. The device needs to power cycle to power up again. Under-voltage protection (UVP) triggers when the FB voltage is below 0.4V. Usually, UVP accompanies hitting the current limit, which results in SCP.

UVLO Protection

The NB650/NB650H has under-voltage lockout (UVLO) protection. When V_{IN} exceeds the UVLO-rising threshold voltage, the NB650/NB650H powers up. It shuts off when V_{IN} falls below the UVLO-falling threshold voltage. This is non-latch protection.

Thermal Shutdown

The NB650/NB650H employs thermal shutdown by internally monitoring the temperature of the junction. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. This is non-latch protection. There is about 25°C hysteresis. Once the junction temperature drops to around 125°C, it initiates a soft-start.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage-Large ESR Caps

A resistor divider from the output voltage to the FB pin sets the output voltage. Changing the VID codes for the NB650/NB650H accomplishes the same thing.

When there is no external ramp, the output voltages are set by feedback resistors R1 and R2A, R2B and R2C. First, choose R1 within 5kΩ-to-100kΩ to ensure stable operation. V_{OUT1}, V_{OUT2}, V_{OUT3} and V_{OUT4} are the voltages at different VID codes, arranged from low to high. Then determine R2A, R2B and R2C as follows:

$$R2A = \frac{V_{REF}}{V_{OUT1} - \frac{1}{2}\Delta V_{OUT} - V_{REF}} \times R1 \quad (14)$$

$$R2B = \frac{1}{\frac{V_{OUT2} - \frac{1}{2}\Delta V_{OUT2} - V_{REF}}{V_{REF}} \times \frac{1}{R1} - \frac{1}{R2A}} \quad (15)$$

$$R2C = \frac{1}{\frac{V_{OUT3} - \frac{1}{2}\Delta V_{OUT3} - V_{REF}}{V_{REF}} \times \frac{1}{R1} - \frac{1}{R2A}} \quad (16)$$

V_{OUT4} can be calculated as:

$$V_{OUT4} = \frac{V_{REF} \times (R1 + R2A // R2B // R2C)}{R2A // R2B // R2C} + \frac{1}{2}\Delta V_{OUT4} \quad (17)$$

Where ΔV_{OUTx} is the output ripple determined by equation 30**.**

Setting the Output Voltage-Small ESR Caps

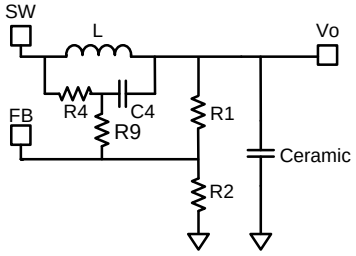


Figure 10: Simplified Ceramic Capacitor Circuit

When using a low-ESR ceramic capacitor on the output, add an external voltage ramp to FB through resistor R4 and capacitor C4. The ramp voltage, V_{RAMP}, influences the output voltage besides the resistor divider shown in Figure 10. Equation 7 calculates V_{RAMP}.

Choose R1 within 5kΩ-to-100kΩ. The value of R2 then is determined as follows:

$$R2A = \frac{V_{FB(AVG)}}{(\frac{1}{R1} + \frac{1}{R4 + R9}) \times (V_{OUT1} - V_{FB(AVG)})} \quad (18)$$

$$R2B = \frac{1}{\frac{V_{OUT2} - V_{FB(AVG)}}{V_{FB(AVG)}} \times (\frac{1}{R1} + \frac{1}{R4 + R9}) - \frac{1}{R2A}} \quad (19)$$

$$R2C = \frac{1}{\frac{V_{OUT3} - V_{FB(AVG)}}{V_{FB(AVG)}} \times (\frac{1}{R1} + \frac{1}{R4 + R9}) - \frac{1}{R2A}} \quad (20)$$

And V_{OUT4} also can be calculated with equation 17.

The $V_{FB(AVG)}$ is the average value on FB. $V_{FB(AVG)}$ varies with the V_{IN}, V_O, and load condition; its value in skip mode is lower than in PWM mode, which means the load regulation is strictly related to the $V_{FB(AVG)}$. Also the line regulation is related to the $V_{FB(AVG)}$; use a lower V_{RAMP} that meets the conditions of equation 10 for better load or line regulation.

For PWM operation, estimate $V_{FB(AVG)}$ from the following equation:

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2} V_{RAMP} \times \frac{R1//R2}{R1//R2 + R9} \quad (21)$$

Usually, R9 is set to 0Ω, and it can also be set following equation 22 for better noise immunity. Set the value to <(1/5)×R1//R2 to minimize its influence on V_{RAMP}.

$$R9 \le \frac{1}{2\pi \times C4 \times 2f_{SW}} \quad (22)$$

Using equations 18 through 20 to calculate the output voltage can be complicated. Furthermore, as V_{RAMP} changes due to changes in V_{OUT} and V_{IN}, V_{FB} also varies. To improve the output voltage accuracy and simplify the R2A, R2B and R2C calculations, add a DC-blocking capacitor (C_{DC}) to filter the DC influence from R4 and R9. Figure 11 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. The addition of this capacitor simplifies the R2A, R2B and R2C calculations, as per equations 23-25.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

$$R2A = \frac{V_{REF} + \frac{1}{2}V_{RAMP}}{\frac{1}{R1} \times (V_{OUT1} - V_{REF} - \frac{1}{2}V_{RAMP})} \quad (23)$$

$$R2B = \frac{1}{\frac{1}{R1} \times \frac{(V_{OUT2} - V_{REF} - \frac{1}{2}V_{RAMP})}{V_{REF} + \frac{1}{2}V_{RAMP}} - \frac{1}{R2A}} \quad (24)$$

$$R2C = \frac{1}{\frac{1}{R1} \times \frac{(V_{OUT3} - V_{REF} - \frac{1}{2}V_{RAMP})}{V_{REF} + \frac{1}{2}V_{RAMP}} - \frac{1}{R2A}} \quad (25)$$

Select C_{DC}>10×C4 for better DC blocking, but select a value less than 0.47µF when considering start up performance. For larger C_{DC} values for better FB noise immunity, combine with reduced R1 and R2 to limit the C_{DC} to a reasonable value without affecting system start-up. Note that even with C_{DC}, the load and line regulation are still related to V_{RAMP}.

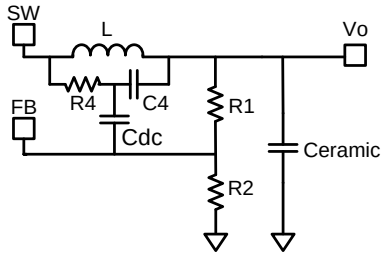


Figure 11: Simplified Circuit with Ceramic DC-Blocking Capacitor

Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use ceramic capacitors for best performance. The capacitance varies significantly over temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over temperature.

In the layout, place the input capacitors as close to the IN pin as possible.

The capacitors must also have a ripple current rating greater than the maximum input ripple

For POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp current of the converter. The input ripple current can be estimated as:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (26)$$

The worst-case condition occurs at:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (27)$$

For simplification, choose an input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If the system requires a specific input voltage ripple, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated as:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (28)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (29)$$

Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic or POSCAP capacitors. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (30)$$

Where R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (31)$$

The output voltage ripple caused by ESR is very small, and therefore requires an external ramp to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4 following equations 5, 9 and 10.
voltage generated from the ESR is high enough to stabilize the system. Therefore, an external

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

ramp is not needed. A minimum ESR value of 12mΩ is required to ensure stable operation of the converter. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (32)$$

Inductor

The inductor supplies constant current to the output load while being driven by the switching input voltage. A larger value inductor results in less ripple current, which results in lower output ripple voltage. However, a larger value inductor is physically larger, has a higher series resistance, and/or lower saturation current. To determine the inductor value, allow the inductor peak-to-peak ripple current to reach approximately 30% to 40% of the maximum switch current limit. Make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated as:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (33)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated as:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (34)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

TYPICAL APPLICATION

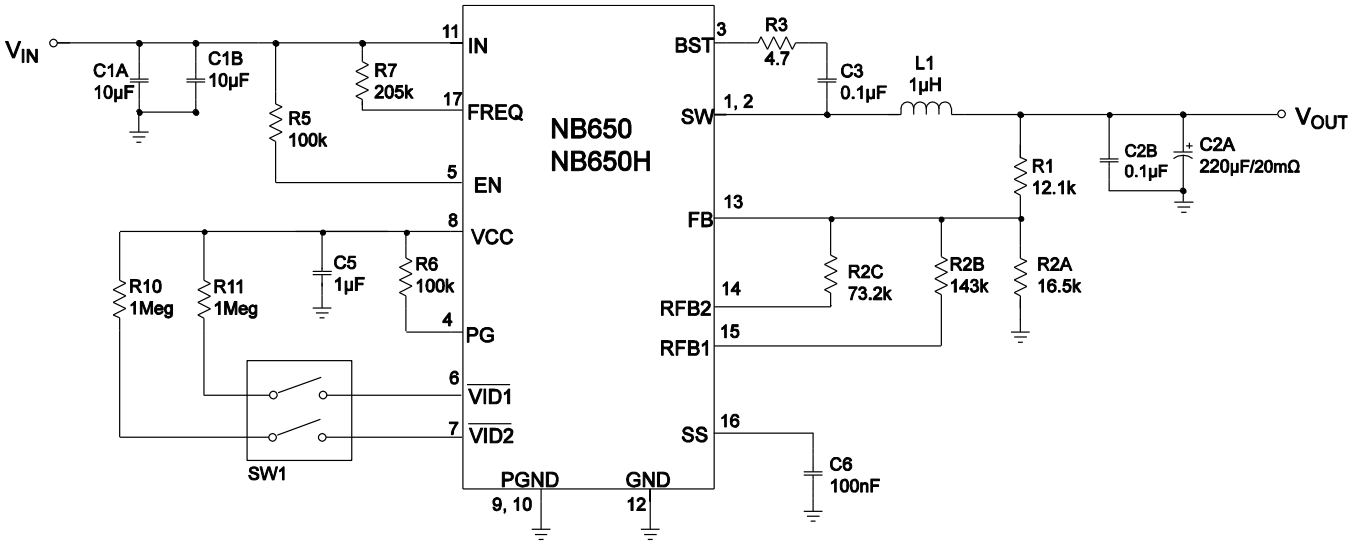


Figure 12: Typical Application Circuit with No External Ramp
V_{IN} = 12V, V_{OUT} = 1.05/1.15/1.20V, I_{OUT} = 6A, f_{SW} = 550kHz

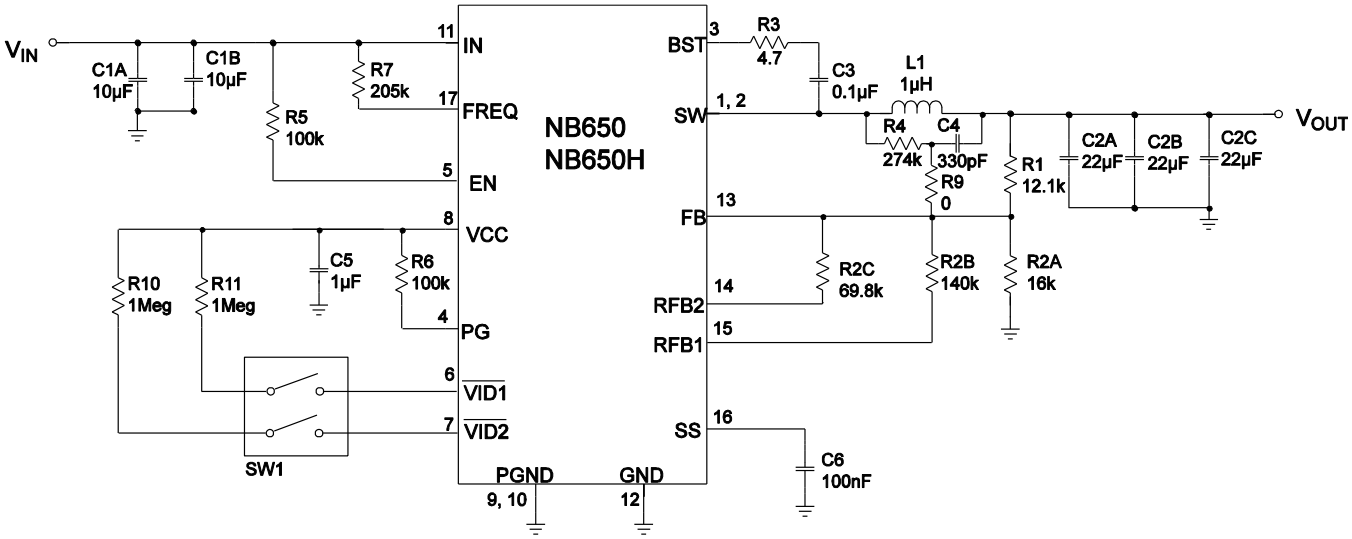


Figure 13: Typical Application with Low-ESR Ceramic Capacitor
V_{IN} = 12V, V_{OUT} = 1.05/1.10/1.15/1.20V, I_{OUT} = 6A, f_{SW} = 550kHz

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

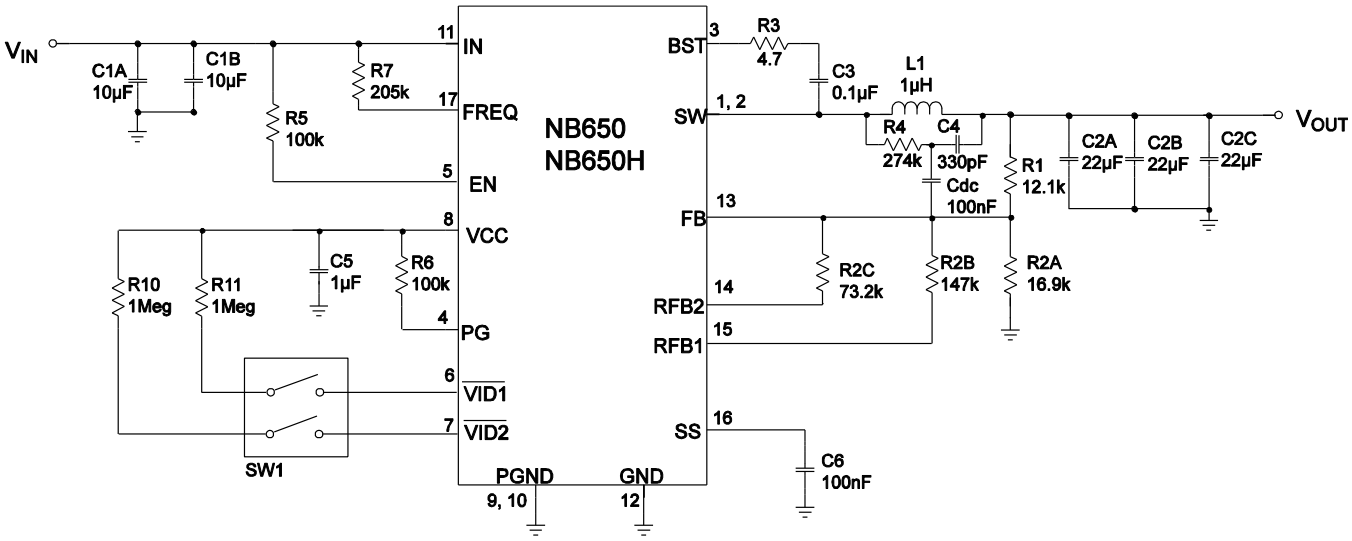


Figure 14: Typical Application Circuit with Low-ESR Ceramic Capacitor and DC-Blocking Capacitor
V_{IN} =12V, V_{OUT} = 1.05/1.10/1.15/1.20V, I_{OUT} = 6A, f_{SW} = 550kHz

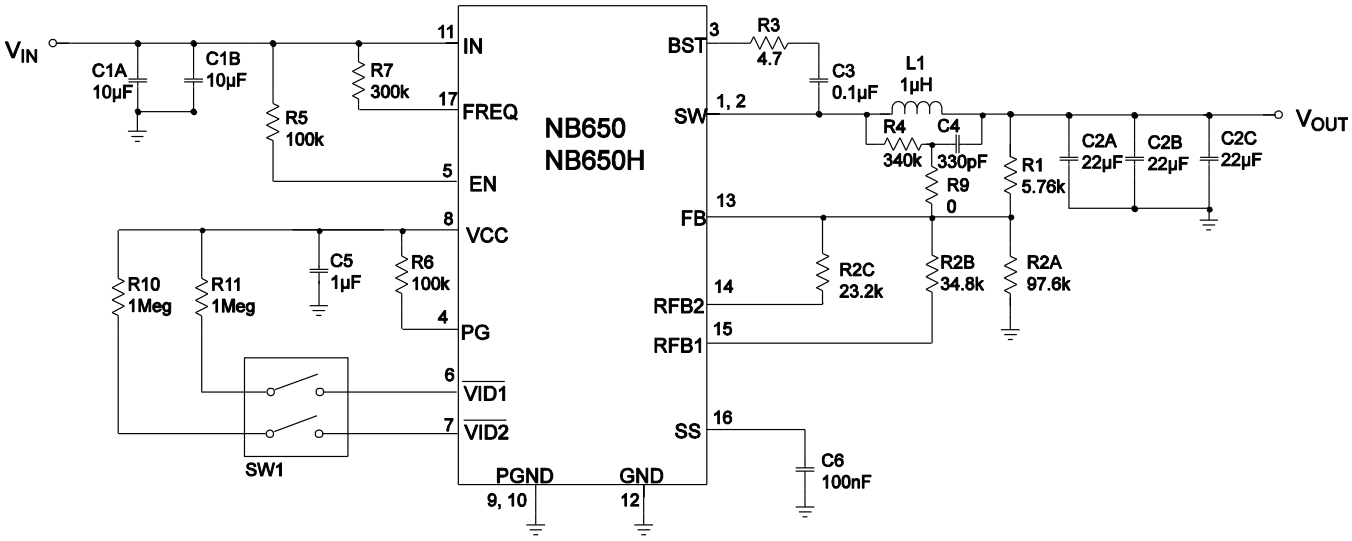
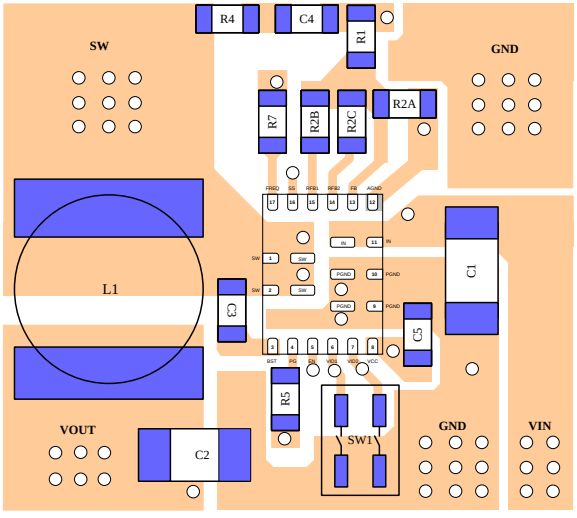


Figure 15: Typical Application Circuit
V_{IN} = 19V, V_{OUT} = 0.65/0.75/0.80/0.90V, I_{OUT} = 6A

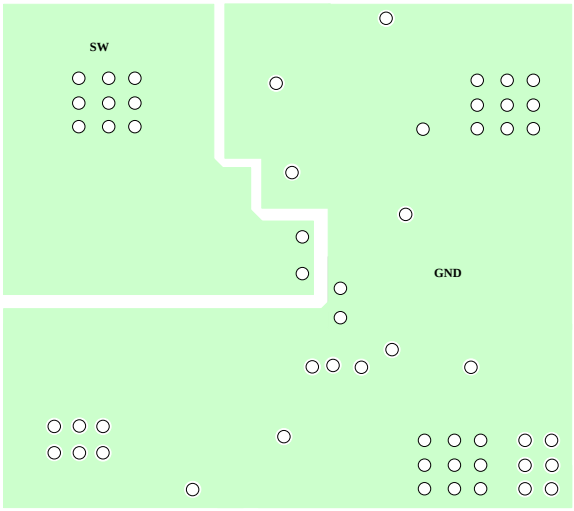
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

LAYOUT RECOMMENDATIONS

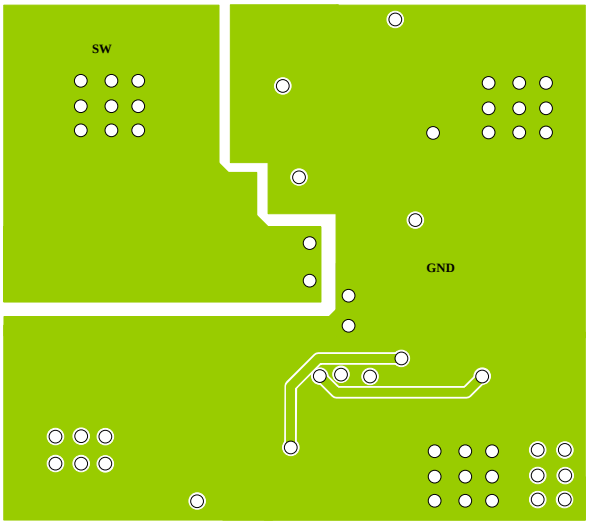
1. Place the high current paths (GND, IN, and SW) as close to the device as possible with direct, short, and wide traces.
2. Use a 0.1µF input decoupling capacitor to connect the IN and GND pins. Put the input decoupling capacitor and input capacitors as close to the IN and GND pins as possible.
3. Put the V_{CC} decoupling capacitor as close to the V_{CC} and GND pins as possible.
4. Keep the switching node SW short and away from the feedback network.
5. Place the external feedback resistors next to the FB pin. Make sure that there is no via on the FB trace.
6. Keep the BST voltage path (BST, $C_{BST,}$ and SW) as short as possible.
7. Connect the bottom IN and SW pads to large copper areas to achieve better thermal performance.
8. Use a four-layer layout to achieve better thermal performance.



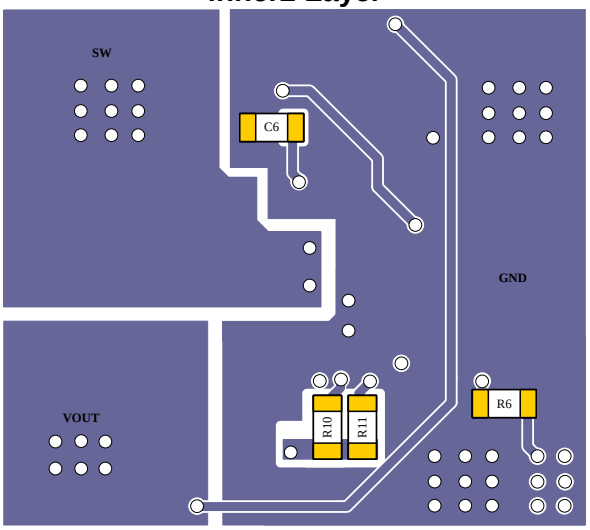
Top Layer



Inner1 Layer



Inner2 Layer



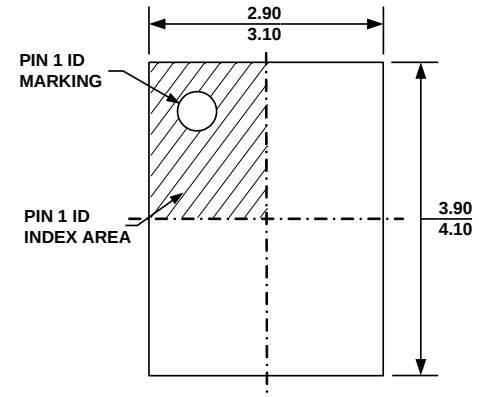
Bottom Layer

Figure 16: PCB Layout Guide

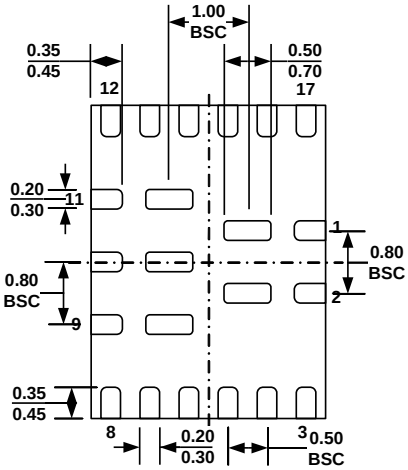
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
Preliminary Specifications Subject to Change © 2023 MPS. All Rights Reserved.

PACKAGE INFORMATION

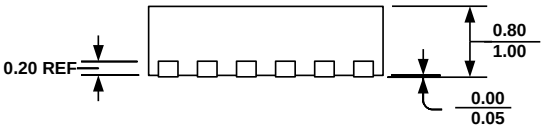
QFN17 (3 x 4mm)



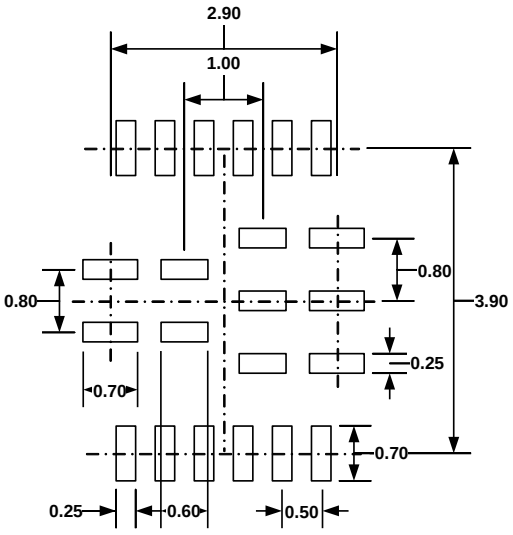
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.