MPQ4482-Q

All-In-One QC3.0 USB Charging Port, Support 36Vin, 5V@3A Type-C AEC-Q100 Qualified

DESCRIPTION

The MPQ4482-Q integrates a monolithic step-down switch-mode converter with a single USB current-limit switch and a Type-C 5V@3A mode configuration channel for the USB port. It achieves a 3A output current over a wide input supply range with excellent load and line regulation.

The output of the USB switch is current-limited. The USB port supports QC3.0 mode. It is backward compatible with DCP schemes for battery charging specification (BC1.2), the divider mode, and 1.2V/1.2V mode, without requiring outside user interaction. The USB port also supports USB Type-C 5V@3A DFP mode.

Fault protections include hiccup current limiting, and thermal shutdown (TSD).

The MPQ4482-Q requires a minimal number of readily available, external components. It is available in a QFN-22 (4mmx4mm) package.

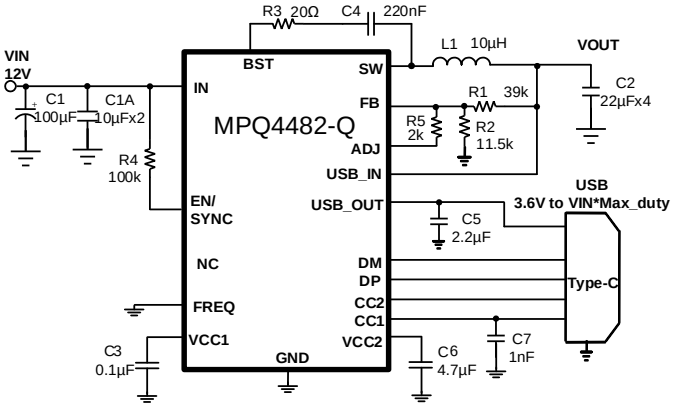
FEATURES

- DP/DM Support Quick Charge 3.0 Mode-Class A
- Backward Compatible for DCP Schemes: BC1.2 Short mode, Divider Mode, 1.2V/1.2V Mode
- Supports USB Type-C 5V@3A DFP Mode
- I/O pins (DP, DM, CC1 and CC2) Support Short to Battery Protection
- USB_OUT Short to Battery Protection when VBUS is Enabled
- Wide 4V to 36V Operating Input Range
- 450kHz/280kHz Selectable Frequency
- 3A Output Current
- Line Drop Compensation
- Accurate USB Current Limit
- Forced CCM Operation
- Frequency Sync from 250kHz to 2.2MHz (Recommended: <15% of SYNC IN Duty Cycle)
- Load Shedding vs. Temperature
- Hiccup Current Limit for Buck and USB
- ±8KV HBM ESD Rating for CC1, CC2 and USB_OUT to GND
- ±2.5kV HBM ESD Rating for DM, DP to GND
- Available in a QFN-22 (4mmx4mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

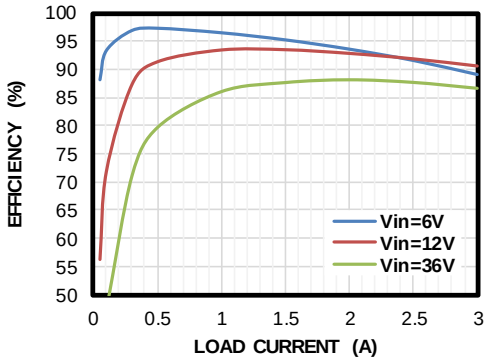
- Automotive QC3.0 Charging Ports
- Automotive USB Type-C Charging Ports

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 5.1V, f_{SW} = 450kHz, L = 10µH, DCR = 69mΩ



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ4482GR-Q-AEC1	QFN-22 (4mmx4mm)	*See Below*	1

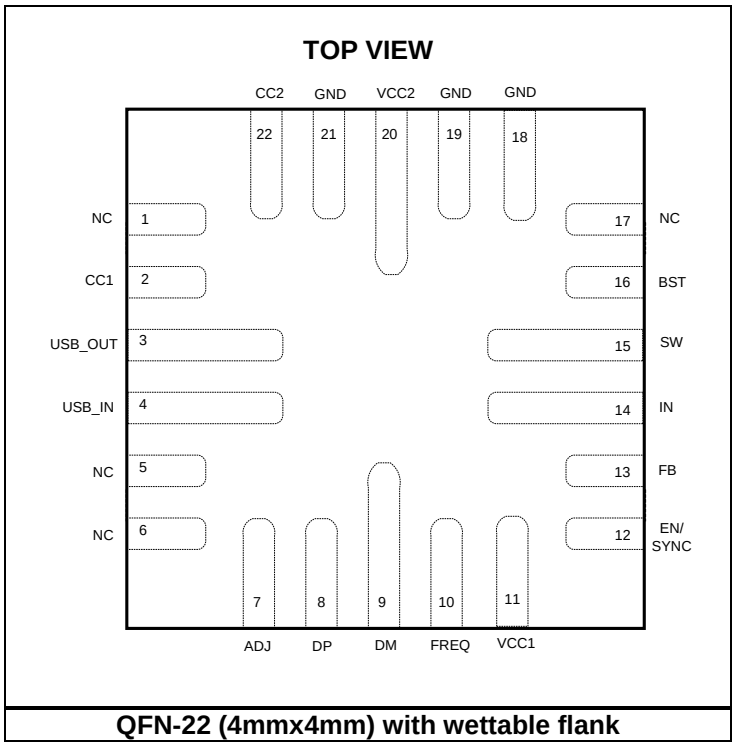
* For Tape & Reel, add suffix –Z (e.g. MPQ4482GR-Q-AEC1–Z).

TOP MARKING

MPSYWW
MP4482
LLLLLL
Q

MPS: MPS prefix
Y: Year code
WW: Week code
MP4482: Part number
LLLLLL: Lot number
Q: Part number suffix

PACKAGE REFERENCE



QFN-22 (4mmx4mm) with wettable flank

PIN FUNCTIONS

QFN 4x4 Pin #	Name	Description
1, 5, 6, 17	NC	**No connection**. Can tie to GND**.**
2	CC1	**Configuration channel.** CC1 detects connections and configures the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.
3	USB_OUT	**USB bus voltage output.**
4	USB_IN	**USB bus voltage input**
7	ADJ	**Line drop compensation pin.** ADJ sinks a current from FB to ground to regulate the buck output voltage.
8	DP	**D+ data line to USB connector**. DP is the input/output used for handshaking with portable devices.
9	DM	**D- data line to USB connector.** DM is the input/output used for handshaking with portable devices.
10	FREQ	**Frequency select pin.** Float or connect this pin to VCC1 to set the buck's switching frequency to 280kHz. Short this pin to ground to set the switching frequency to 450kHz.
11	VCC1	**Internal 4.8V LDO regulator output.** Decouple VCC1 with a 0.1µF to 0.22µF capacitor. Select a capacitor that does not exceed 0.22µF.
12	EN/SYNC	**On/Off Control Input.** Internally pulled to ground by a 500kΩ resistor. Apply an external CLK on this pin to sync up the switching frequency.
13	FB	**Feedback.** To set the output voltage, connect FB to the tap of an external resistor divider from the output to GND. To prevent current limit runaway during a short-circuit fault condition, the frequency fold-back comparator lowers the oscillator frequency when the FB voltage drops below 400mV
14	IN	**Supply voltage.** The MPQ4482-Q operates from a 4V to 36V input rail. Requires C1 to decouple the input rail. Connect using a wide PCB trace.
15	SW	**Switch output.** Use a wide PCB trace to make the connection.
16	BST	**Bootstrap.** A 220nF capacitor is connected between SW and BST to form a floating supply across the high-side switch driver. A 20Ω resistor placed between the SW and BST capacitor is recommended to reduce SW voltage spikes.
18, 19, 21	GND	**Power ground.**
20	VCC2	**Internal 3.6V LDO regulator output.** Decouple with a 4.7µF capacitor.
22	CC2	**Configuration channel.** CC2 detects connections and configures the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage V_{IN} ..... -0.4V to +40V
V_{SW} ..... –0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{USB_IN, USB_OUT} ..... –0.3V to +20V
CC1, CC2, DM, DP ..... –0.3V to +18V
V_{BST} ..... V_{SW} + 5.5V
$V_{EN/SYNC}$ ..... -0.3V to +6V (2)
V_{VCC2} ..... -0.3V to +4V
All other pins ..... –0.3V to +4.5V
Continuous power dissipation (T_A = 25°C) (3) (5)
QFN-22 (4mmx4mm) 4.3W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... –65°C to +150°C

ESD Rating

Human-body model (HBM):
±8kV HBM ESD Rating for CC1, CC2 and USB_OUT to GND;
±2.5kV HBM ESD rating for DM, DP to GND; other pins pass ±2kV
Charged-device model (CDM) .....
.....all pins pass ±2kV

Recommended Operating Conditions (4)

Operation input voltage range ..... 6V to 36V
Output voltage range ..... 3.6V to 12V or VINxMax_duty
Output current 3A
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-22 (4mmx4mm)			
EVQ4482-Q-R-00A (5)	29	7	°C/W
JESD51-7 (6)	44	9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) See the EN Control section on page 12 for more details on the EN pin's ABS Max rating.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EVQ4482-Q-R-00A, 4-layer PCB, 57mmx57mm
6) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (Shutdown)	I_{IN}	V_{EN} = 0V,T_J = 25°C			1	μA
		V_{EN} = 0V,T_J = -40°C to +125°C			8	
Buck_Supply current (Quiescent)	$I_{Q\_CL\_VBUSDIS}$	CC pin float, V_{FB} = 1V		600	900	μA
Overall_Supply current (Quiescent)	I_Q	CC1 to ground with 5.1kΩ, V_{FB} = 1V		800	1200	μA
EN rising threshold	V_{EN_Rising}		1.15	1.4	1.65	V
EN falling threshold	$V_{EN\_Falling}$		1.05	1.25	1.45	V
EN input current	I_{EN1}	V_{EN} = 2V		4.5	6	μA
	I_{EN2}	V_{EN} = 0		0	0.2	
Thermal shutdown (7)	T_{STD}			165		°C
Thermal hysteresis (7)	T_{STD_HYS}			20		°C
VCC1 regulator	V_{CC1}	I_{CC} = 0mA	4.6	4.8	5.1	V
VCC1 load regulation	V_{CC1_LOG}	I_{CC} = 5mA		1.5	5	%
VCC2 regulator	V_{CC2}	I_{CC} = 0mA	3.3	3.6	3.7	V
Step-Down Converter						
V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO}		3.3	3.5	3.7	V
V_{IN} under-voltage lockout falling threshold	V_{UVLO_Fall}		3.1	3.3	3.5	V
HS switch-on resistance	R_{DSON_HS}			85	150	mΩ
LS switch-on resistance	R_{DSON_LS}			55	105	mΩ
Feedback voltage	V_{FB}		780	796	812	mV
Feedback current	I_{FB}	V_{FB} = 820mV		10	100	nA
Sync frequency range	f_{SYNC}		0.25		2.2	MHz
Oscillator frequency	f_{SW1}	FREQ = GND	350	440	530	kHz
	f_{SW2}	FREQ = Float	210	280	350	kHz
Fold-back frequency	f_{FB}	V_{FB} < 400mV		100		kHz
Maximum duty cycle	D_{MAX}		94.5	96		%
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to+125°C			5	
High-side current limit (7)	I_{LIMIT}	Over 40% duty cycle	4.8	6.8	8.8	A
Minimum on time (7)	t_{ON_MIN}			70		ns
Soft start time	t_{SS}	Output from 10% to 90%	0.4	1.5	2.55	ms
USB Switch						
Under-voltage lockout rising threshold	V_{USB_UVR}		2.6	2.8	3	V
Under-voltage lockout hysteresis threshold	V_{USB_UVHYS}			370		mV

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switch on resistance	R_{DSON_SW}			20	45	mΩ
Output discharge resistance	R_{DIS_USB}		150	200	250	Ω
USB output voltage	V_{USB_OUT1}	Default	-3%	5.1	+3%	V
	V_{USB_OUT2}	QC 3.0, T_J = 25°C	-1.5%	9	+1.5%	V
	V_{USB_OUT3}	QC 3.0, T_J = 25°C	-1.5%	12	+1.5%	V
Current limit	I_{Limit1}	V_{OUT} drop 10%	3.18	3.55	3.93	A
USB_OUT soft start time	T_{SS}	V_{OUT} = 5V, from 10% to 90%	0.2	0.45	0.7	ms
USB input OVP rising	V_{USB_OV}	V_{OUT} = 5V	5.5	5.75	6	V
USB input OVP recovery threshold	$V_{OV\_Recovery}$	V_{OUT} = 5V	5.25	5.45	5.65	V
Hiccup mode on time	T_{HICP_ON2}	V_{OUT} =5V, OC		2		ms
Hiccup mode off time	T_{HICP_OFF}	V_{OUT} = 5V, V_{BUS} connected to GND		2		s
Line drop compensation	$V_{IN\_5\_C}$	V_{OUT} = 5V, I_{OUT} = 3A		260	400	mV
BC1.2 DCP Mode						
DP and DM short resistance	R_{DP/DM_Short}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = 25°C			40	Ω
		V_{DP} = 0.8V, I_{DM} = 1mA, T_J = -40°C to +125°C			45	
Divider Mode						
DP/DM output voltage	$V_{DP/DM\_Divider}$	V_{OUT} = 5V	2.5	2.7	2.85	V
DP/DM output impedance	$R_{DP/DM\_Divider}$	T_J = 25°C	20	25	30	kΩ
		T_J = -40°C to +125°C	18	25	32	
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$	V_{OUT} = 5V	1.1	1.2	1.3	V
DP/DM output impedance	$R_{DP/DM\_1.2V}$		200	300	400	kΩ
USB Type-C 5V@3A Mode – CC1 and CC2						
CC voltage to enable VCONN	V_{Ra}				0.75	V
CC voltage to enable Vbus	V_{Rd}		0.85		2.45	V
CC voltage at 5.1kΩ Rd	V_{CC_Rd}	CC pin pull-down by 5.1kΩ	1.31	1.683	2.04	V
CC detach threshold	V_{OPEN}		2.75			V
CC voltage falling debounce timer	$T_{CC\_debounce}$	VBUS enable deglitch	100	150	200	ms
CC voltage rising debounce timer	$T_{PD\_debounce}$	VBUS disable deglitch	5	10	20	ms

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{CONN} output power	P_{VCONN}	VCONN comes from buck output with some series resistance	1			W
V_{BUS} to ground impedance	R_{BUS}	Type-C detach, after output discharge turn-off	72.4			kΩ
Quick Charge 3.0 Mode						
Data detect voltage	V_{DAT_REF}		0.25	0.3	0.4	V
Output voltage select ref	V_{SEL_REF}		1.8	2	2.2	V
DP output impendence	R_{DP_QC}		300	400	1500	kΩ
DM output impendence	R_{DM_QC}		13	20	27	kΩ
DM low glitch time (7)	t_{Glitch_DM}			10		ms
DP high glitch time	t_{Glitch_DP}		800		1600	ms
Output voltage change glitch time	$t_{Glitch\_V\_Change}$		20	40	60	ms
Bus voltage step	$V_{BUS\_CONT\_STEP}$		150	200	250	mV
Time for VBUS to discharge to 5V when DP < 0.6V (7)	t_{V_UNPLUG}				500	ms

Notes:

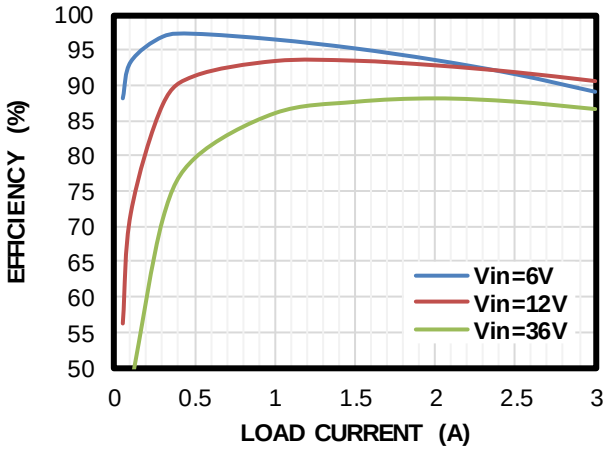
7) Guaranteed by engineering sample characterization

TYPICAL CHARACTERISTICS

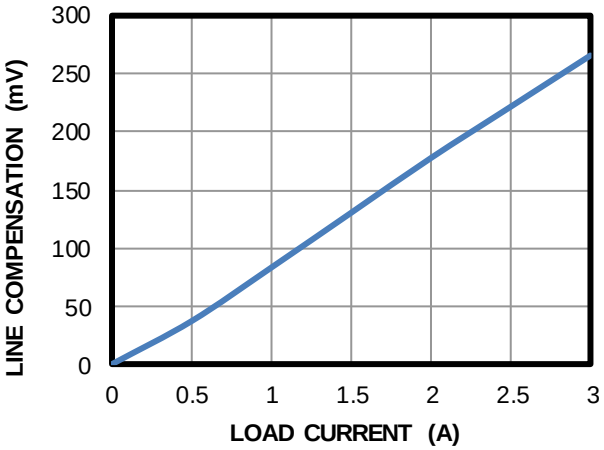
V_{IN} = 12V, V_{OUT} = 5.1V, L = 10µH, f_{SW} = 450kHz, Type-C mode, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current

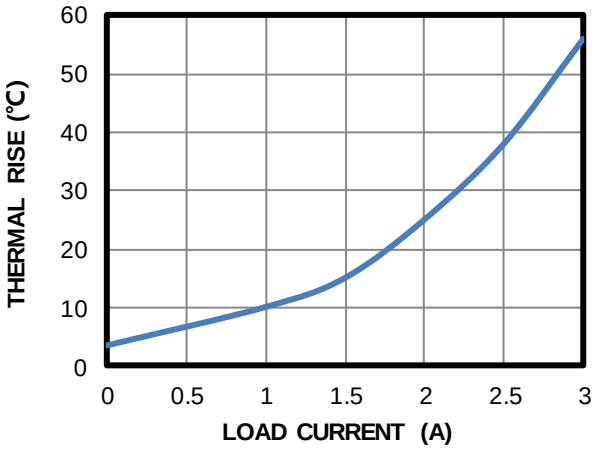
V_{OUT} = 5.1V, Fs = 450kHz, L = 10µH, DCR = 69mΩ



Line Drop Compensation vs. Load Current



Case Temperature Rise vs. Load Current

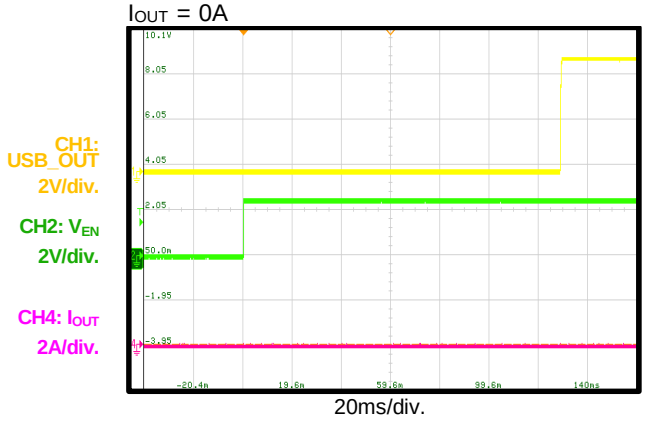


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.1V, L = 10µH, f_{SW} = 450kHz, Type-C mode, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

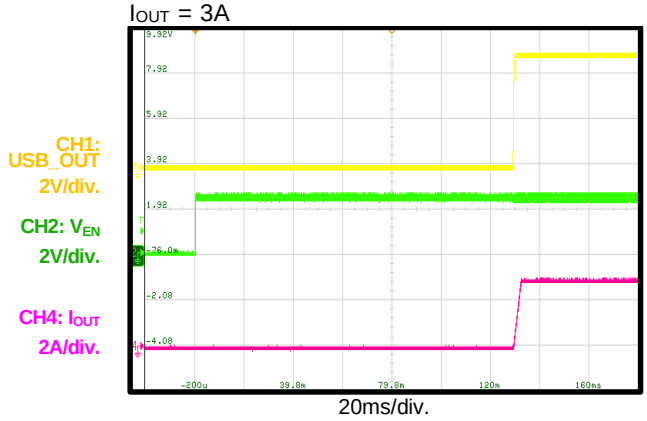
EN On

I_{OUT} = 0A



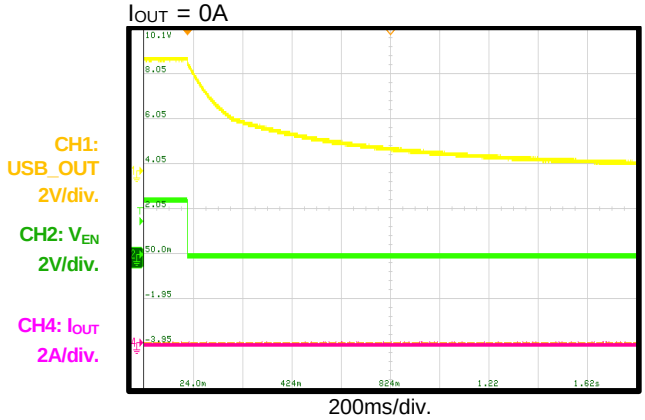
EN On

I_{OUT} = 3A



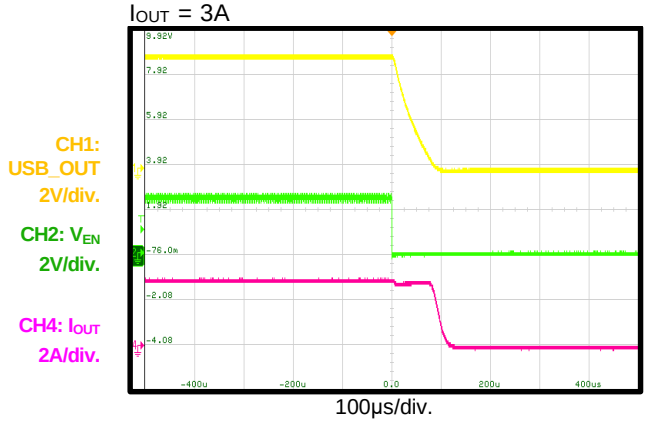
EN Off

I_{OUT} = 0A



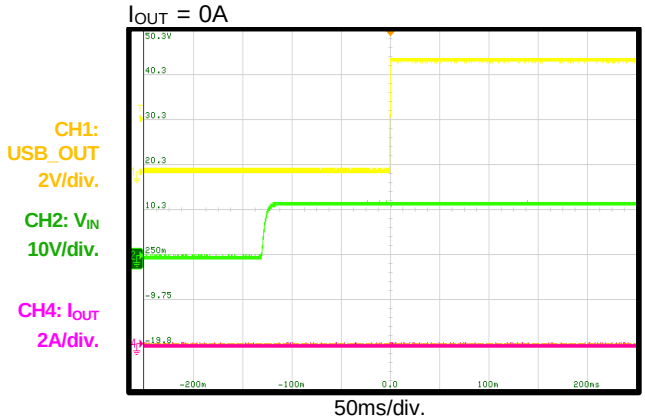
EN Off

I_{OUT} = 3A



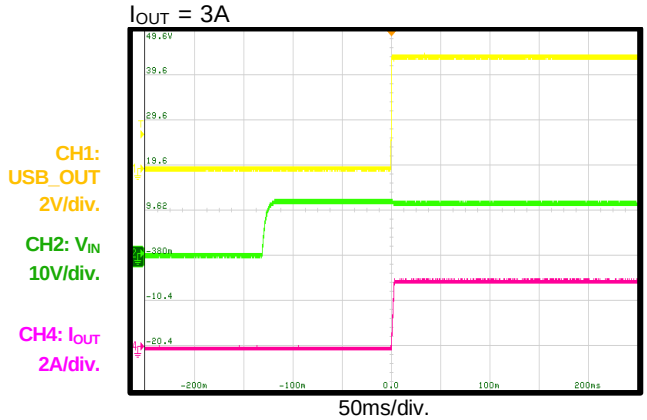
Power-On

I_{OUT} = 0A



Power-On

I_{OUT} = 3A

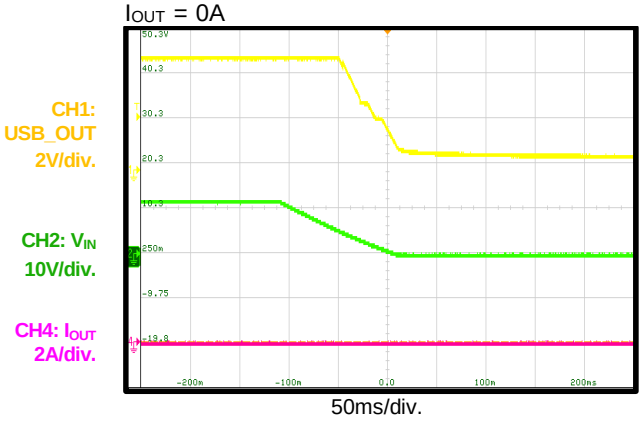


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.1V, L = 10µH, f_{SW} = 450kHz, Type-C mode, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

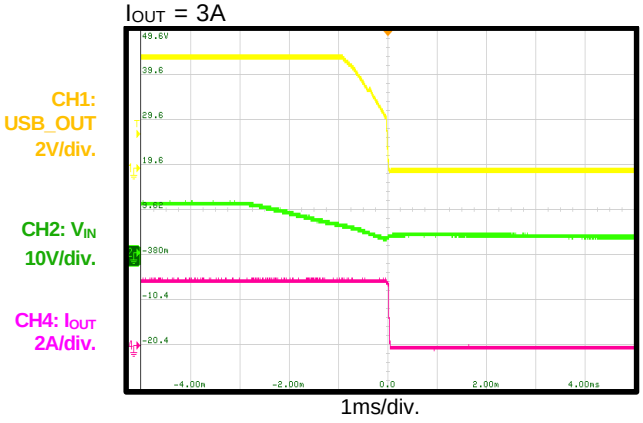
Power-Off

I_{OUT} = 0A



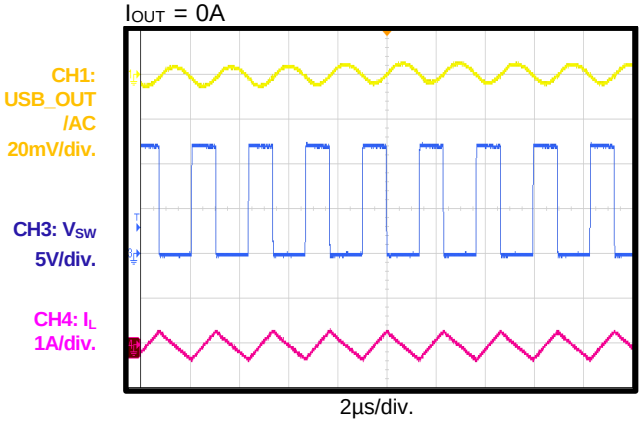
Power-Off

I_{OUT} = 3A



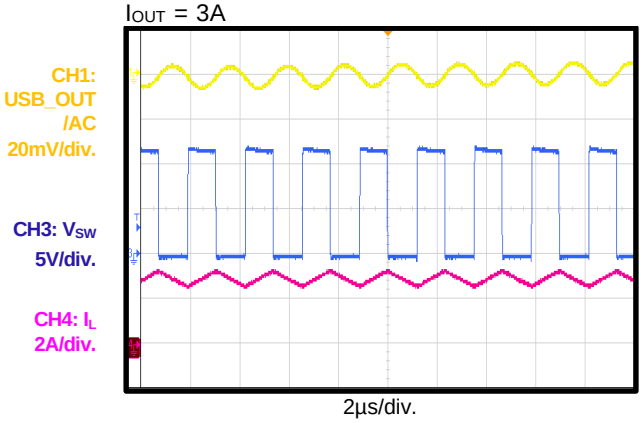
USB_OUT Ripple

I_{OUT} = 0A



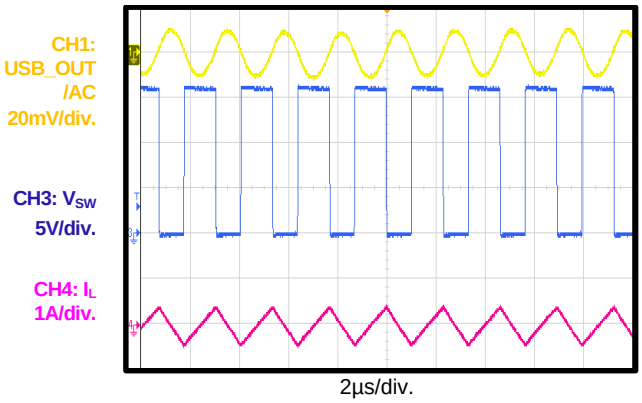
USB_OUT Ripple

I_{OUT} = 3A



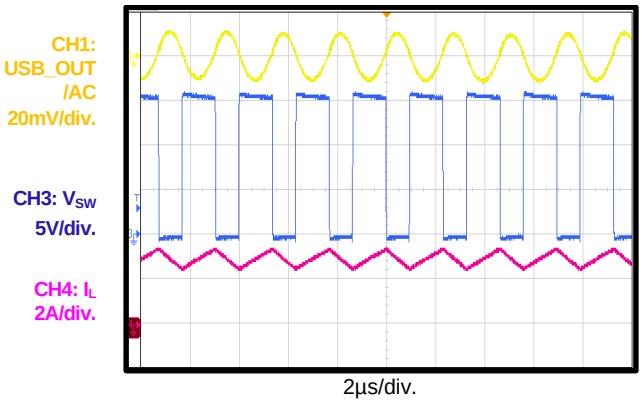
USB_OUT Ripple

V_{IN} = 16V, USB_OUT = 9 V, I_{OUT} = 0A



USB_OUT Ripple

V_{IN} = 16V, USB_OUT = 9V, I_{OUT} = 3A

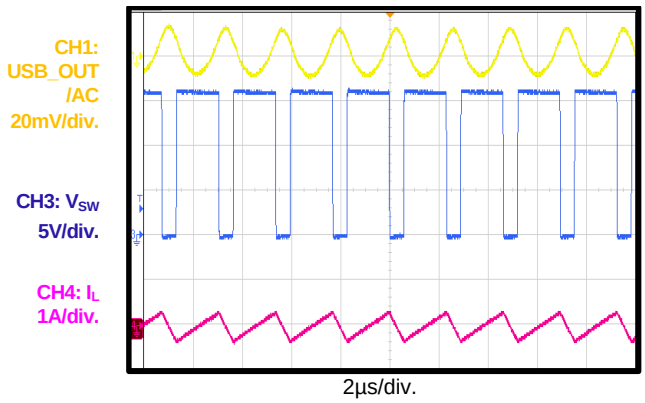


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.1V, L = 10µH, f_{SW} = 450kHz, Type-C mode, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

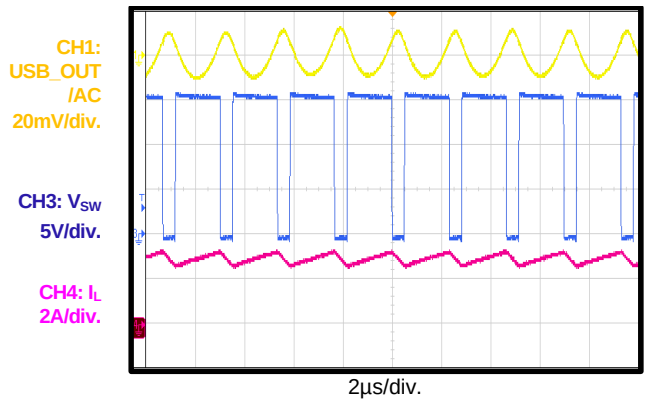
USB_OUT Ripple

V_{IN} = 16V, USB_OUT = 12V, I_{OUT} = 0A

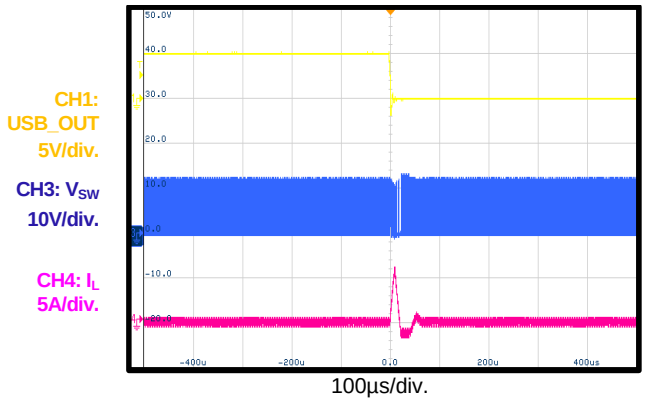


USB_OUT Ripple

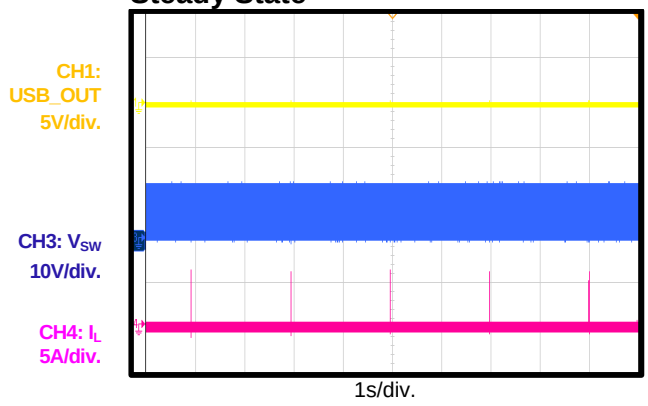
V_{IN} = 16V, USB_OUT = 12V, I_{OUT} = 3A



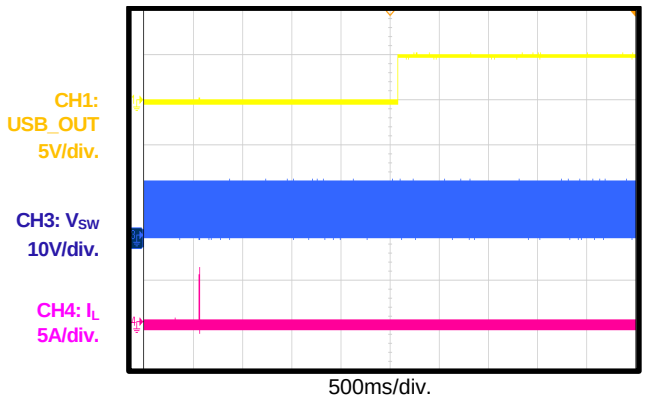
USB_OUT Short to USB_GND Entry



USB_OUT Short to USB_GND Steady State

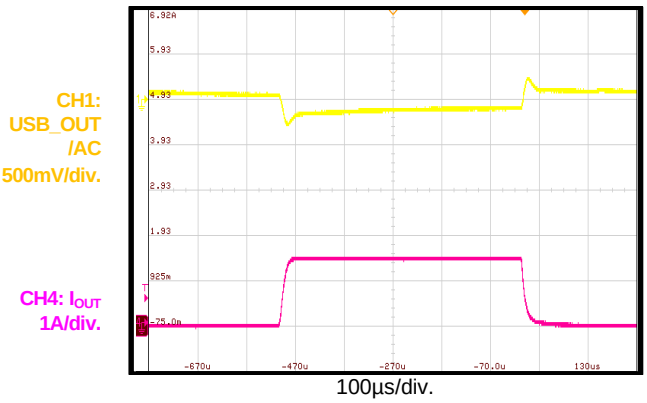


USB_OUT Short to USB_GND Recovery



Load Transient

0 <-> 1.5A/800mA/µs

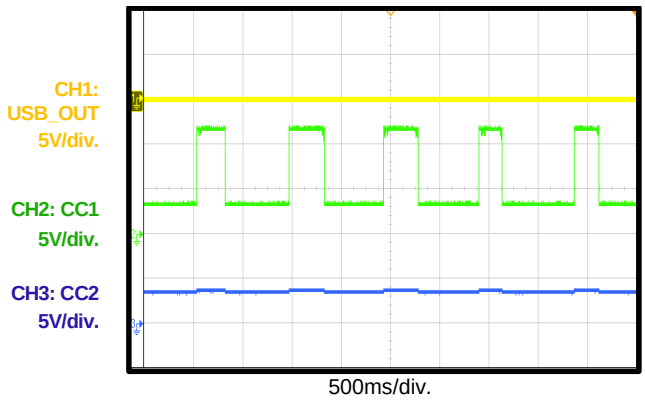


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.1V, L = 10µH, f_{SW} = 450kHz, Type-C mode, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

CC1 Short to Battery

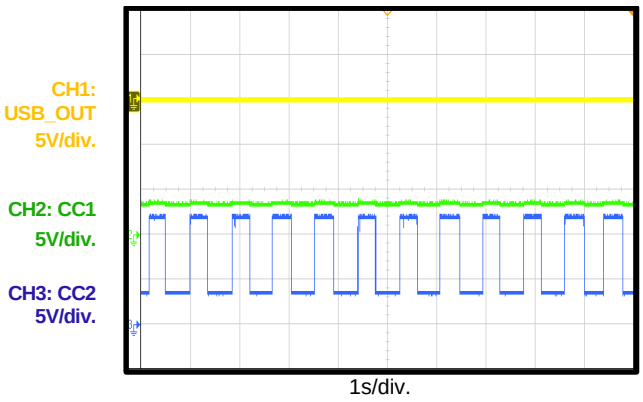
$V_{BATTERY}$ = 12V, CC2 Float



500ms/div.

CC2 Short to Battery

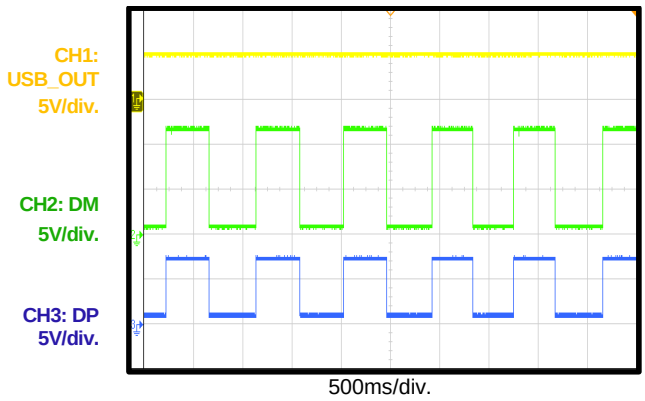
$V_{BATTERY}$ = 12V, CC1 Float



1s/div.

DM Short to Battery

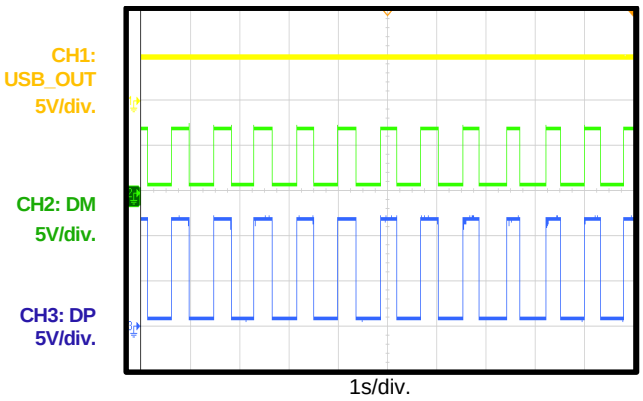
$V_{BATTERY}$ = 12V



500ms/div.

DP Short to Battery

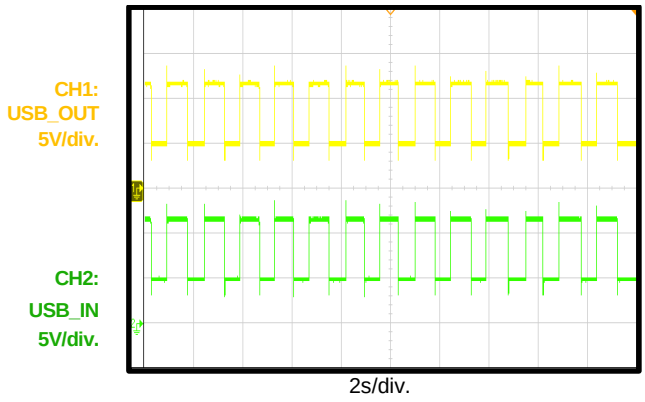
$V_{BATTERY}$ = 12V



1s/div.

USB_OUT Short to Battery

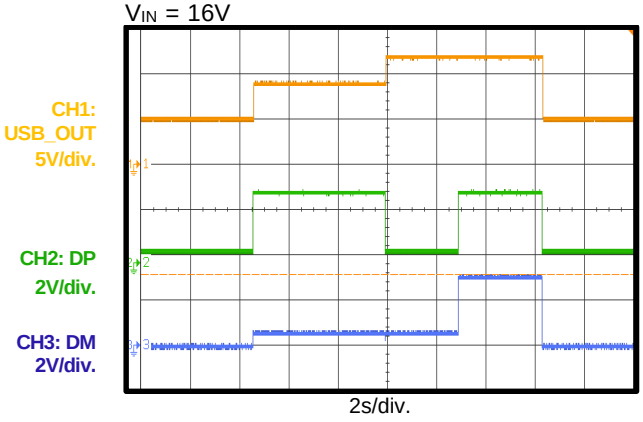
$V_{BATTERY}$ = 12V



2s/div.

Mode Transition from 5V -> 9V -> 12V -> 5V

V_{IN} = 16V



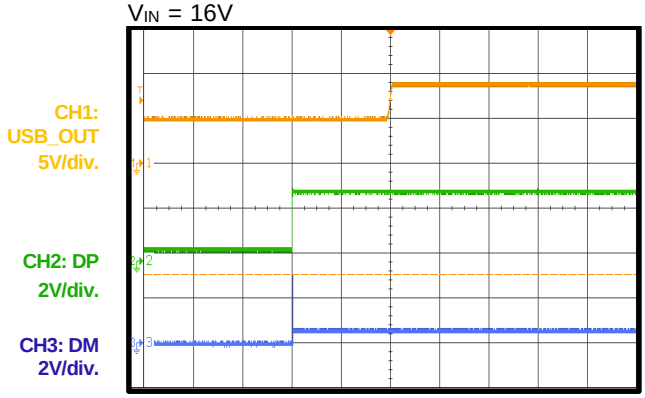
2s/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.1V, L = 10µH, f_{SW} = 450kHz, Type-C mode, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

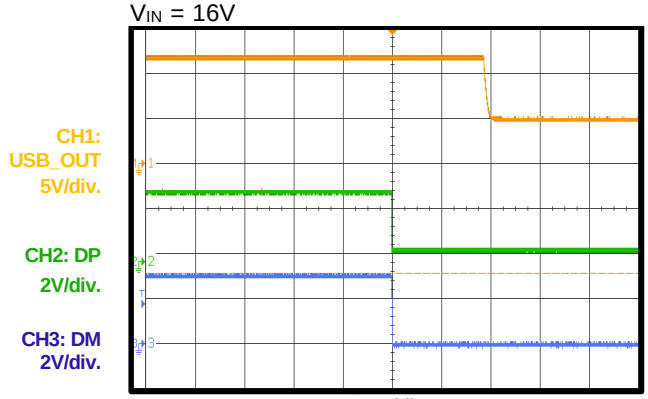
Mode Transition from 5V -> 9V Zoom In

V_{IN} = 16V



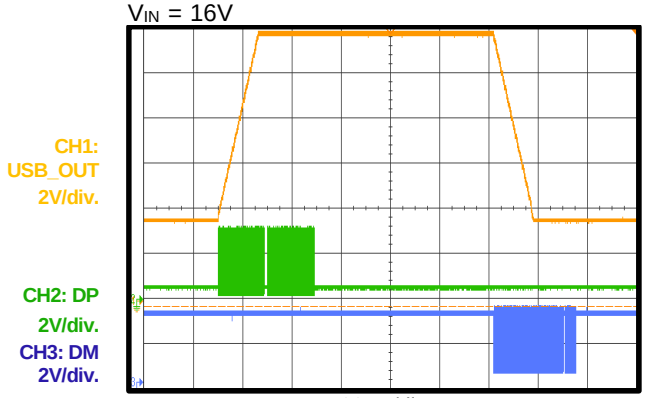
Mode Transition from 12V -> 5V Zoom In

V_{IN} = 16V



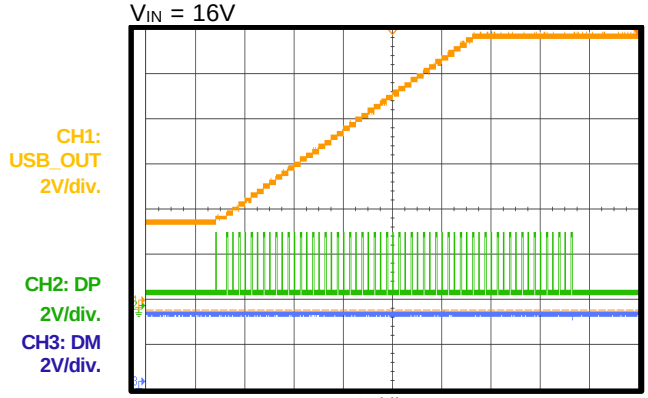
Continuous Mode from 3.6V -> 12V ->3.6V

V_{IN} = 16V



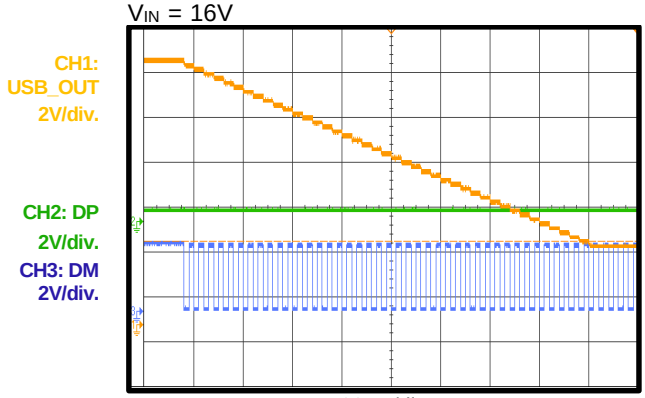
Continuous Mode from 3.6V -> 12V Zoom In

V_{IN} = 16V



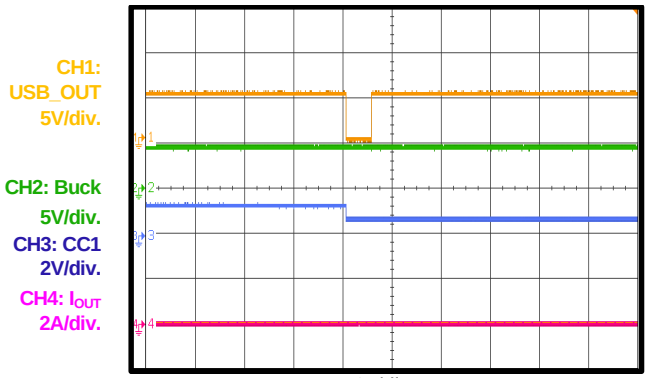
Continuous Mode from 12V -> 3.6V Zoom In

V_{IN} = 16V



Load Shedding Entry

USB_OUT = 5V

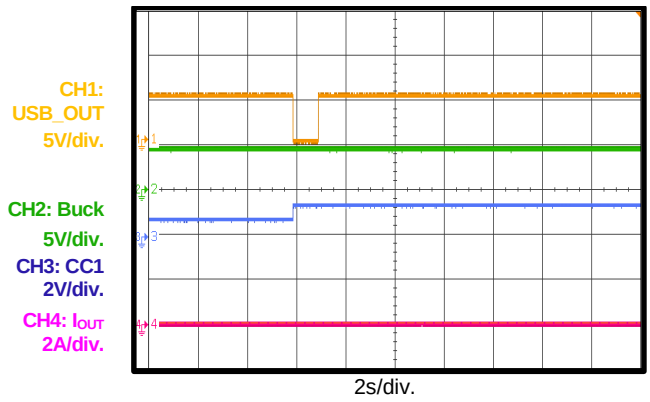


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.1V, L = 10µH, f_{SW} = 450kHz, Type-C mode, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

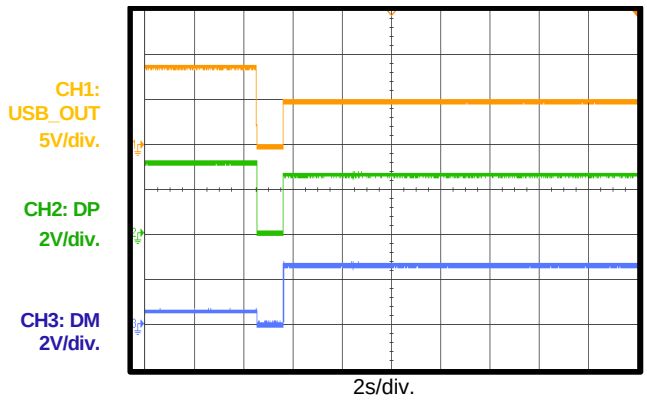
Load Shedding Recovery

USB_OUT = 5V



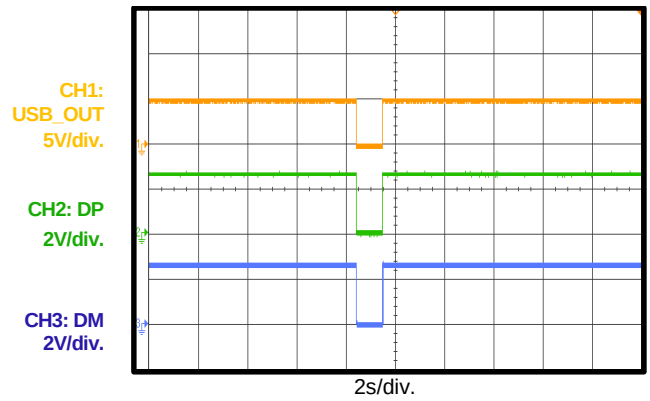
Load Shedding Entry

V_{IN} = 16V, USB_OUT = 9V



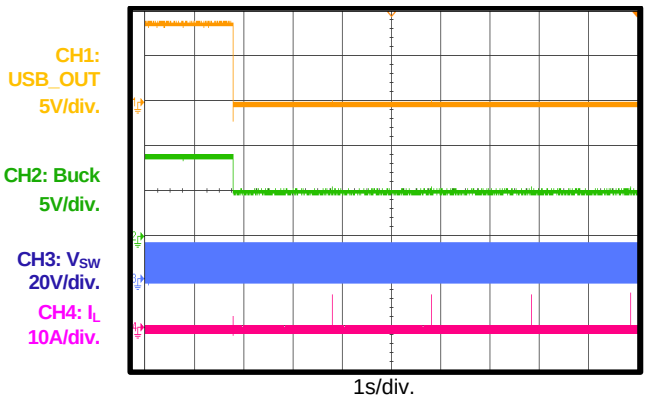
Load Shedding Recovery

V_{IN} = 16V, USB_OUT = 9V



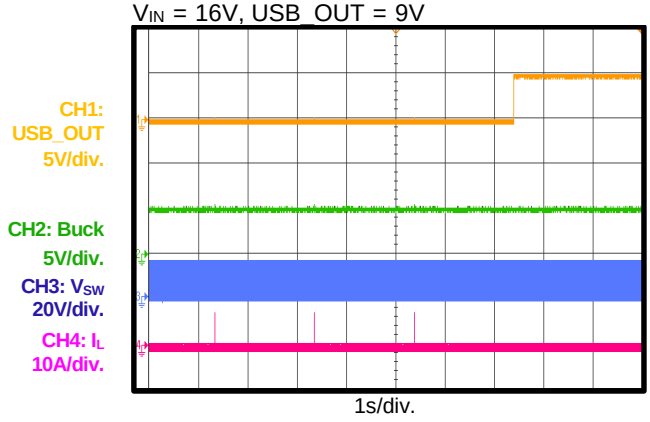
USB_OUT Short to USB_GND Entry

V_{IN} = 16V, USB_OUT = 9V



USB_OUT Short to USB_GND Recovery

V_{IN} = 16V, USB_OUT = 9V



FUNCTIONAL BLOCK DIAGRAM

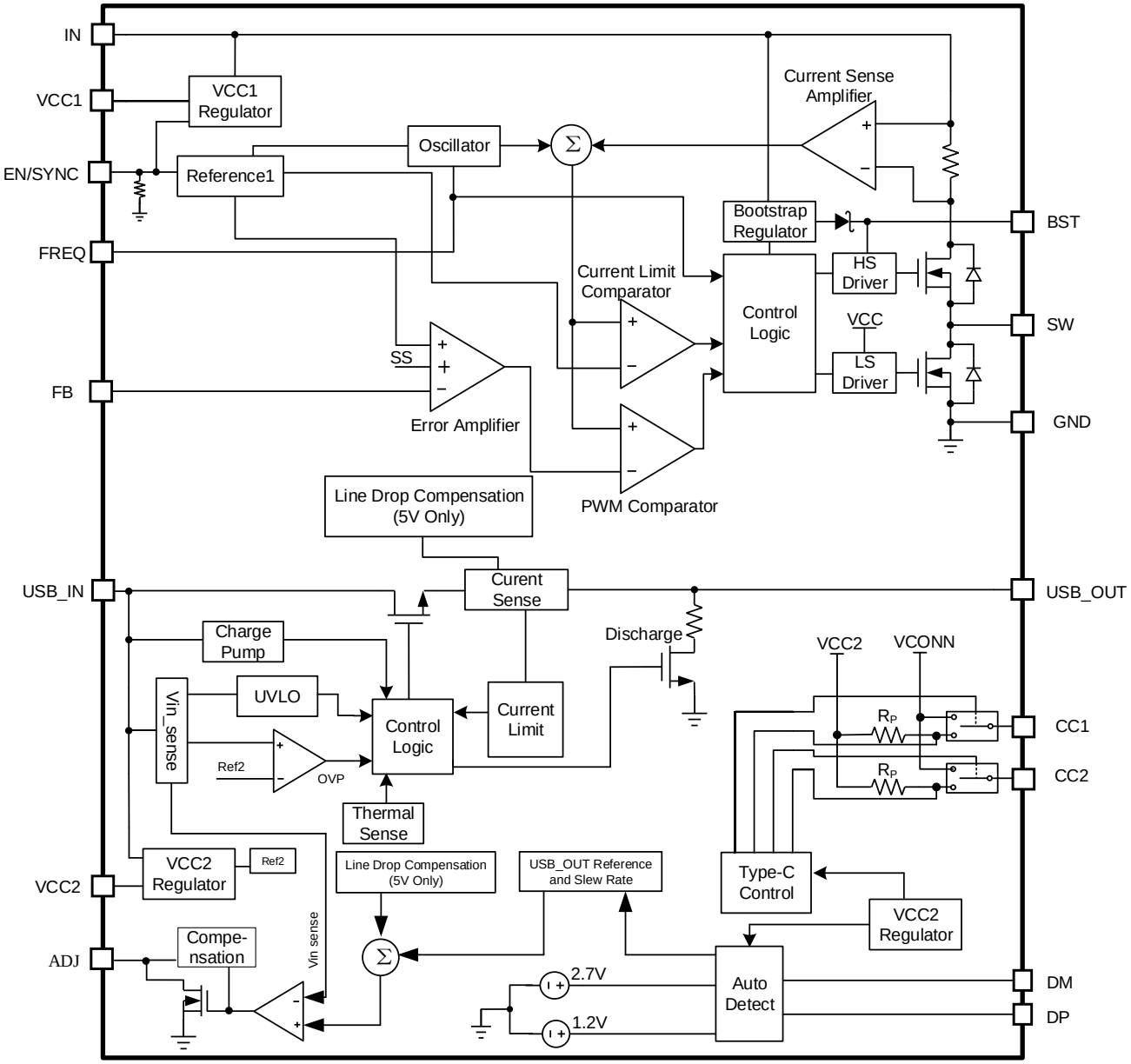


Figure 1: Functional Block Diagram

OPERATION

Buck Converter

The MPQ4482-Q integrates a monolithic synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs and a USB current-limit switch with charging port auto detection. It offers a compact solution to achieve 3A of continuous output current over a wide input supply range with excellent load and line regulation.

The MPQ4482-Q operates in a fixed-frequency, peak current control mode to regulate the output voltage. The internal clock initiates the PWM cycle, which turns on the integrated high-side power MOSFET. The high-side MOSFET remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle begins.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage (V_{FB}) against the internal 0.8V reference (V_{REF}) and outputs a COMP voltage. This COMP voltage controls the power MOSFET current. The optimized, internal compensation network minimizes the external component count and simplifies the control loop design.

Internal VCC1 Regulator

The 4.8V internal regulator powers most of the internal circuitries of the buck converter. This regulator takes the V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 4.8V, the output of the regulator is in full regulation. If V_{IN} is below 4.8V, the output decreases with the V_{IN}. The VCC requires an external 0.1µF ceramic decoupling capacitor.

Internal VCC2 Regulator

The 3.6V internal regulator powers most of the USB switch's internal circuitries. The VCC2 requires an external 4.7µF ceramic decoupling capacitor.

EN/SYNC Control

The MPQ4482-Q has an enable control pin (EN). Pull EN high to enable the IC; pull EN low to disable the IC. An internal 500kΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

EN/SYNC is clamped internally using a 6.5V series Zener diode (see Figure 2). Connect the EN/SYNC input through a pull-up resistor to any voltage connected to VIN. The pull-up resistor limits the EN/SYNC input current below 100µA. For example, when 12V is connected to VIN, $R_{PULLUP} \geq (12V - 6.5V) / 100\mu A = 55k\Omega$.

Connecting EN/SYNC directly to a voltage source without a pull-up resistor requires limiting the voltage amplitude below or equal to 6V to prevent damage to the Zener diode.

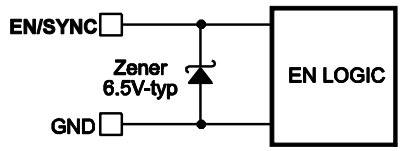


Figure 2: 6.5V-Type Zener Diode

To use the synchronous function, connect an external clock within the range 250kHz to 2.2MHz to EN/SYNC. The external clock should be connected at least 2ms after the output voltage is set. The internal clock rising edge is synchronized to the external clock rising edge when the external clock is connected. The pulse width of the external clock signal should be shorter than 1.7µs. The SYNC input signal typically has a 15% duty cycle when V_{IN} = 12V.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. The UVLO rising threshold is 3.5V, and its falling threshold is 3.3V.

Internal Soft Start (SS)

The soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage that ramps up from 0V to 5V. When SS is below V_{REF}, the error amplifier uses SS as the reference. When SS is above V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is internally set to 1.5ms.

If the output of the MPQ4482-Q is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side

switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

Buck Over-Current Protection (OCP)

The MPQ4482-Q has a cycle-by-cycle over-current limit when the inductor peak current exceeds the current-limit threshold, and V_{FB} drops below the under-voltage (UV) threshold (about 50% below the reference). Once UV triggers, the MPQ4482-Q enters hiccup mode to re-start the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4482-Q exits hiccup mode once the over-current condition is removed.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, M1, C4, L1 and C2 (see Figure 3). If the difference between V_{BST} and V_{SW} exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C4. To reduce SW spike voltage, place a 20Ω resistor between SW and the BST capacitor.

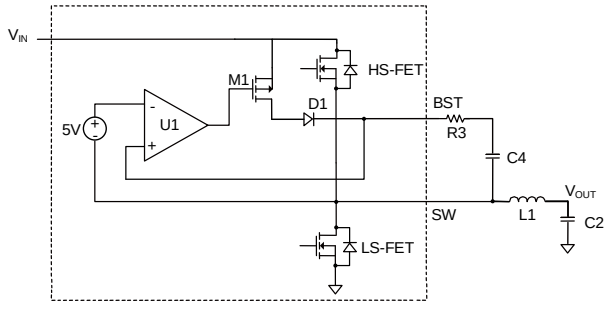


Figure 3: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip enables. The reference block starts by generating a stable reference voltage and current. Next, the internal regulator enables. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: when EN is low, when VIN is low, and thermal shutdown triggers. In shutdown, the signaling path is blocked to avoid any fault triggering. Then the COMP voltage and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

USB Charging Port Controller Section

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at insufficient supply voltage. If the input voltage exceeds the USB's SW UVLO threshold, the power MOSFET turns on with a controlled slew rate after a fixed delay.

Internal Soft Start

The internal soft start prevents the output voltage from overshooting during start-up and inrush current.

Line Drop Compensation

The MPQ4482-Q compensates for an output voltage drop, such as high impedance caused by a long trace, to maintain a 5.1V load-side voltage. The line drop compensation is only active when V_{IN} equals 5.1V. The line drop compensation is realized through the ADJ pin.

The MPQ4482-Q increases USB input voltage by 260mV at a 3A output current (see Figure 4).

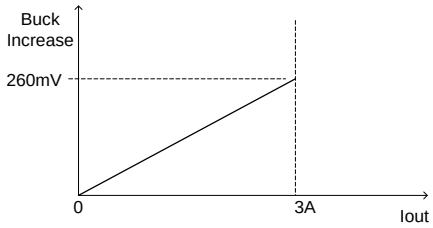


Figure 4: Increasing USB Input Voltage

The ADJ pin slowly sinks a controlled current. The line drop compensation amplitude linearly increases as the load current increases.

If the USB input voltage is below 5.1V in a no load condition, the ADJ pin sinks a current to regulate the upstream regulator's output voltage to 5.1V. If the USB input voltage exceeds 5.1V, the MPQ4482-Q does not regulate the input voltage. To maintain a 3.6V to 12V output voltage range, configure R1/R2 to let default output voltage to remain below 3.6V. It is

recommended to set the buck to 3.5V, meaning R1 is 39kΩ, and R2 is 11.5kΩ.

Figure 5 shows the typical schematic for ADJ usage. The ADJ pin sink current capability is 500uA. The feedback current through R1 must remain below 500uA. R1 can be calculated with Equation (1):

$$R1(k\Omega) > \frac{\Delta V(V)}{0.5} \quad (1)$$

Where ΔV is the output differential voltage value between the QC3.0 max voltage and the voltage buck sets.

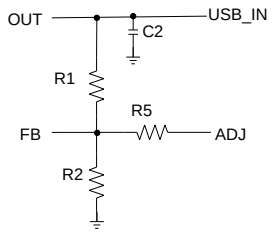


Figure 5: ADJ Configuration

To limit the maximum output current, V_{ADJ} can also be configured by inserting R5 between the FB pin and the ADJ pin. With R5, the maximum output voltage can be estimated with Equation (2):

$$V_{OUT\_Max}(V) = \frac{R_1 + R_2 // R_5}{R_2 // R_5} \times V_{FB}(V) \quad (2)$$

After adding R5, the maximum ADJ sink current can be calculated with Equation (3):

$$I_{ADJ\_Max}(\mu A) = \frac{V_{FB} - V_{OFFSET}(mV)}{R_5(k\Omega)} \quad (3)$$

Where V_{OFFSET} is about 100mV.

USB Input Over-Voltage and Discharge

To protect downstream devices from over-voltage, the MPQ4482-Q provides a USB input OVP discharge function. The device has a smart OVP threshold for different Vouts. IC dynamically sets the OVP threshold to 115% of the V_{OUT} target value.

An accurate and fast comparator monitors the over-voltage condition of the USB input. If the input voltage rises above the threshold, the USB discharge path turns on. When input voltage falls below 5.45V, the IC exits OVP mode.

Output Discharge

When the Type-C device plugs out, both input and output discharge resistors activate for 30ms, and then turn-off. After turn-off, the in and out to ground resistance is high (>72.4kΩ).

Over-Current Protection

Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power FET constant.

If an over-current (OC) condition lasts 2ms or the USB output voltage falls below 3V, the MPQ4482-Q enters hiccup mode.

In hiccup mode, the MPQ4482-Q turns off the power MOSFET. The hiccup signal resets the QC mode to 5V. ADJ changes V_{IN} to 5V. After two seconds (hiccup off-timer), the MPQ4482-Q restarts to check the OC state. If the OC remains, the MPQ4482-Q follows the previous operation. If the OC has been removed, the MPQ4482-Q recovers to normal operation in 5V mode.

USB Short-Circuit Protection

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold before the control loop can respond. If the current reaches an internal secondary current limit level (about 9A), a fast turn-off circuit activates to turn off the power FET. This limits the peak current through the switch to limit the input voltage drop. The fast-off response time is about 300ns. If fast-off works, the device enters hiccup mode directly. After the short-circuit condition is removed, the MPQ4482-Q recovers automatically.

Short to Battery Protection

The MPQ4482-Q provides USB_OUT, CC1, CC2, DP and DM short to battery protections when the IC is enabled and VBUS is on.

During USB output short to battery condition, the USB input rises up to trigger OVP. The USB input discharge path turns on. Meanwhile, the buck regulator discharges the buck output voltage by turning on the low-side switch periodically.

During DP, DM, CC1, or CC2 shorts to battery condition, the MPQ4482-Q can withstand the high voltage for the internal components. The ESD breakdown voltage exceeds the battery voltage.

If a CC1 or CC2 short to battery should occur when the Type-C port is connected but there is no sink, the device is unattached (see Figure 6).

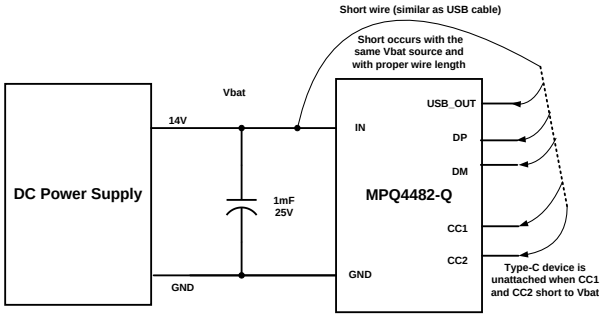


Figure 6: Short to Battery Set-Up

Auto Detection

The MPQ4482-Q integrates the USB-dedicated charging port auto-detect function. This function recognizes most mainstream portable devices. It supports the following charging schemes:

- USB Battery Charging Specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider mode
- 1.2V/1.2V mode
- USB Type-C 5V@3A mode
- Quick Charge 3.0 mode - Class A

The auto-detect function is a state machine that supports all of the DCP charging schemes above.

QC Mode Voltage Transition - Class A

If the downstream device supports the QC specification, the device requires an output voltage above 5V by DM and DP communication (see Table 1). If a higher USB bus voltage is required, the ADJ pin must be used. The ADJ pin is usually connected to the upstream voltage converter's feedback pin. After the handshake, ADJ adjusts V_{OUT} within the range 9V to 12V or another voltage 200mV step-by-step (see Figure 7). Due to smart controller mode, only one ADJ pin can be set to a different, high voltage that meets the QC specification. The output transition is smooth and does not have an undershoot or overshoot.

Table 1: QC Mode Definition

Portable Device		USB Bus Voltage
DP	DM	
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	3.6V to 12V/200mV step according to QC3.0
3.3V	3.3V	No action
0.6V	GND	5V

When the downstream device is removed, the output voltage automatically returns to a default 5V. The input to ground discharge resistor helps this procedure quickly.

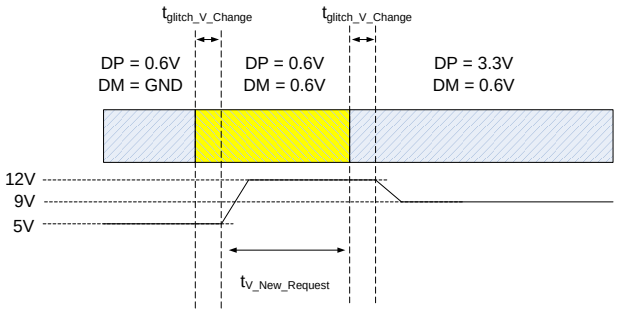


Figure 7: QC Mode Transition

USB Type-C Mode and VCONN

For the USB Type-C solution, two pins on the connector, CC1 and CC2, establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and sink is based on being able to detect terminations residing in the product being attached. To define the functional behavior of CC, a pull-up (Rp) and pull-down (Rd 5.1kΩ) termination model is used based on a pull-up resistor and pull-down resistor (see Figure 8).

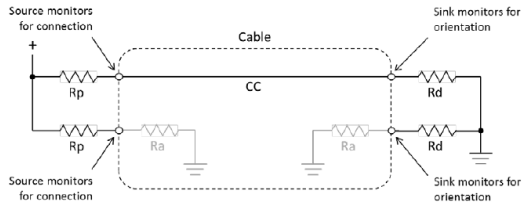


Figure 8: Current Source/Pull-Down CC Model

Initially, a Source exposes independent Rp terminations on its CC1 and CC2 pins, and a sink exposes independent Rd terminations on its CC1 and CC2 pins, the source-to-sink combination of this circuit configuration represents a valid connection. To detect this, the source monitors CC1 and CC2 for a voltage lower than its unterminated voltage. Rp is designated as a function of the pull-up termination voltage and the source's detection circuit. This indicates that either a sink, a powered cable, or a sink connected via a powered cable has been attached.

Two special termination combinations on the CC pins as seen by a source are defined for directly attached accessory modes: Ra/Ra for audio adapter accessory mode and Rd/Rd for debug accessory mode. V_{BUS} disables for those two cases.

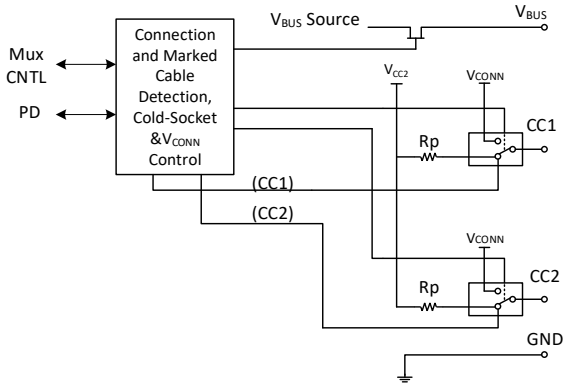


Figure 9: CC Pin Functional Block

1. The Source uses an FET to enable or disable power delivery across V_{BUS} when the source is initially disabled.

2. The Source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both pins to detect a sink. The presence of an Rd pull-down resistor on either pin indicates that a sink is being attached. The value of Rp indicates the initial USB Type-C current level supported by the host. The MPQ4482-Q's default Rp is 4.7kΩ and represents a 3A current level.

3. The source uses the CC pin pull-down function to detect and determine which CC pin is intended for supplying VCONN (when Ra is discovered).

4. Once a sink is detected, the source enables VBUS and VCONN.

5. The source dynamically adjusts the value of Rp to indicate a change in available USB Type-C current to a dink. (e.g at high temperatures, the MPQ4482-Q changes Rp to 12kΩ to indicate a 1.5A current ability).

6. The source monitors the continued presence of Rd to detect sink detaches. When a detach event is detected, the source removes. VBUS and VCONN return to step 2.

Type-C Load Shedding versus Temperature

When the sensed temperature exceeds 120°C, the USB port's CC pin pull-up resistance Rp changes to 12kΩ to advertise its source capability changes to 1.5A. The internal Rd detection threshold also changes from 0.4V to 1.6V. The Ra detection threshold becomes lower than 0.4V. If the sensed temperature exceeds 85°C and lasts 16s, the USB type-C current capability changes back to 3A (Rp = 4.7kΩ).

In QC3.0 charging mode, the VBUS restarts to 5V in DCP charging mode if load shedding occurs. When the device exits load shedding, the VBUS restarts and QC3.0 enables.

The load shedding function works when USB_IN > UVLO.

System

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165°C, it shuts down the entire chip. When the temperature falls below its lower threshold, (about 145°C), the chip enables.

APPLICATION INFORMATION

Design example for the ADJ resistor, R1, R2 and RT resistors

The resistors of the ADJ resistor, R1 and R2, are limited by the ADJ sink capability and maximum output voltage.

The ADJ pin's sink current capability is 500μA. To achieve a 12V output voltage during QC 3.0 mode and let the feedback current flowing through R1 remain below 500μA, R1 should meet the below equation. ΔV is the output differential voltage value set by subtracting the voltage buck sets from the QC3.0 max voltage. If the buck set output is 3.5V, R1 can be estimated with Equation (4):

$$R1(k\Omega) > \frac{\Delta V(V)}{0.5} = \frac{12-3.5}{0.5} = 17k\Omega \quad (4)$$

R1 must remain greater than 17kΩ to provide an 8.5V buck output voltage change. If R1 equals 39kΩ. R2 can be calculated with Equation (5):

$$R2(k\Omega) = \frac{V_{FB} \times R_1}{V_{BUCK} - V_{FB}} \quad (5)$$

Set V_{BUCK} to 3.5V, then R2 is 11.5kΩ.

When R1 and R2 are determined, the ADJ pin's current through the R1 at $12V_{OUT}$ can be calculated with Equation (2):

$$I_{ADJ}(\mu A) = \frac{\Delta V(mV)}{R_1(k\Omega)} = \frac{8500}{39} = 218\mu A$$

R5's maximum value can be calculated with Equation (4):

$$R_5(k\Omega) < \frac{V_{FB} - V_{OFFSET}(V)}{I_{ADJ}} = \frac{0.796-0.1}{0.218} = 3.19k\Omega$$

Then select R5 to equal 2kΩ.

RT + R1 sets the loop bandwidth. The higher RT + R1, the lower the bandwidth. To ensure loop stability, it is recommended to limit the bandwidth between one fifth and one tenth of switching frequency. If R1 is 39kΩ, make RT 51kΩ or choose a higher resistance.

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 125% of the maximum load current. Select an inductor with a small DC resistance for optimum efficiency. The inductor value can be calculated with Equation (6):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (6)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current at approximately 30% to 80% of the maximum load current. The maximum inductor peak current can be estimated with Equation (7):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (7)$$

Inductor peak current must be lower than buck peak current limit.

Selecting Buck Input Capacitor

The input current to the step-down converter is discontinuous, and requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for optimum performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For automotive applications, it is recommended to use a 100μF electrolytic capacitor, two 10μF ceramic capacitors, and one 0.1μF ceramic capacitor.

The input capacitor (C1) absorbs the input switching current, and requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated with Equation (8):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (8)$$

Equation (9) shows the worst case condition when $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (9)$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using an electrolytic capacitor, place two additional high-quality ceramic capacitors as close to IN as possible. The input

voltage ripple can be calculated with Equation (10):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

Selecting a Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. The output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (11)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

The characteristics of the output capacitor affect the stability of the regulatory system.

For applications, it is recommended to use a 100µF electrolytic capacitor with low ESR and two 10µF ceramic capacitors or four 22µF ceramic capacitors.

Other Considerations

Add a 1nF capacitor to CC1 to ensure Type-C mode can be distinguished. See the typical schematic on page 2 for more information.

V_{IN} Under-Voltage Lockout (UVLO) Setting

The MPQ4482-Q has an internal, fixed, under-voltage lockout (UVLO) threshold. The rising threshold is 3.5V, while its falling threshold is about 3.3V. To raise the UVLO point, place an external resistor divider between EN/SYNC and IN (see Figure 9).

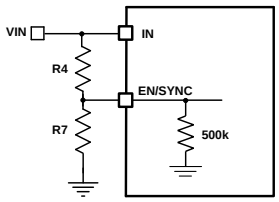


Figure 9: Adjustable UVLO using EN/SYNC Divider

The UVLO threshold can be calculated with Equation (13) and Equation (14):

$$INUV_{RISING} = (1 + \frac{R4}{500k//R7}) \times V_{EN\_RISING} \quad (13)$$

$$INUV_{FALLING} = (1 + \frac{R4}{500k//R7}) \times V_{EN\_FALLING} \quad (14)$$

Where V_{EN_RISING} is 1.4V and $V_{EN\_FALLING}$ is 1.25V.

When selecting R4, ensure that it is large enough to limit the current flowing into EN/SYNC below 150µA.

When R4 = 100kΩ, and R7 = 24kΩ, the MPQ4482-Q powers up when V_{IN} exceeds 7.23V. The MPQ4482-Q powers off when V_{IN} drops below 6.2V.

When R4 = 100kΩ, and R7 = 22kΩ, the MPQ4482-Q powers up when Vin exceeds 7.76V. The MPQ4482-Q powers off when V_{IN} drops below 6.65V.

ESD Protection for I/O Pins

Consider high ESD levels for all USB I/O pins. To further extend the DP, DM, CC1, and CC2 pins' ESD level to cover complicated application environments, add an additional ESD diode to all pins (see Figure 10).

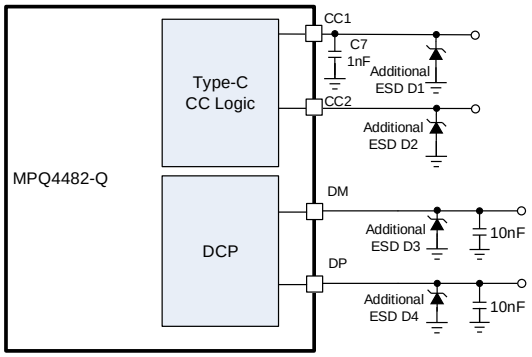
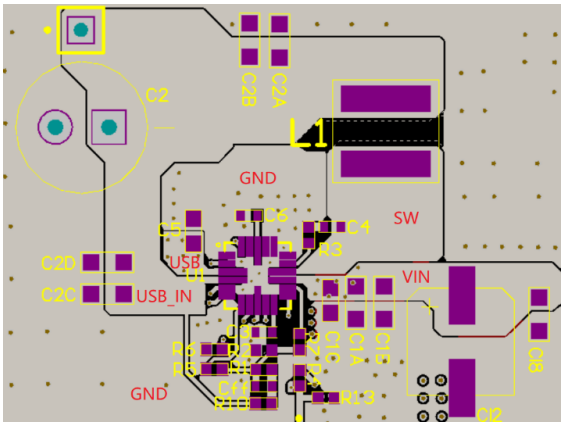


Figure 10: Recommended I/O Pins to Enhance ESD

PCB Layout [8]

Efficient PCB layout is critical for standard operation. Use 4 layers for the PCB to improve thermal performance and dissipation. For the best results, see Figure 11 and the PCB layout guidelines below:

1. Place the ceramic input capacitor as close to IN and GND as possible, especially the small package size (0603) input bypass capacitor.
2. Keep the connection between the input capacitor and IN as short and wide as possible.
3. Place the VCC1/2 capacitor as close as possible to VCC1/2 and GND.
4. Make VCC1/2's trace length from the capacitor to GND as short as possible.
5. Use a large ground plane connected directly to GND.
6. Add vias near GND if the bottom layer is the ground plane.
7. Route SW and BST away from sensitive analog areas such as FB.
8. Place the T-type feedback resistor close to the chip to ensure that the trace connecting to FB is as short as possible.
9. Ensure the SW area is small to reduce EMC-radiated noise.



Top layer

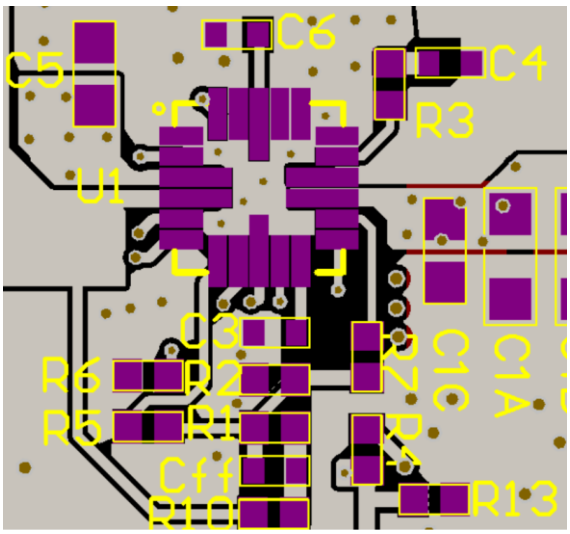


Figure 11: PCB Layout

Notes:

8) The recommended layout is based on the typical application circuit (see Figure 12). Some of the resistor or capacitor names may be different.

TYPICAL APPLICATION CIRCUITS

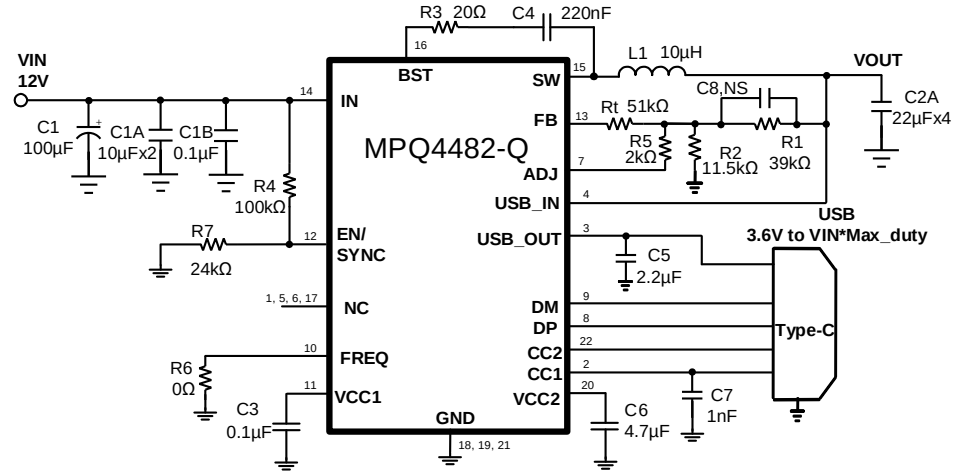


Figure 12: 12Vin, USB Type-C 5V@3A DFP and QC3.0 mode

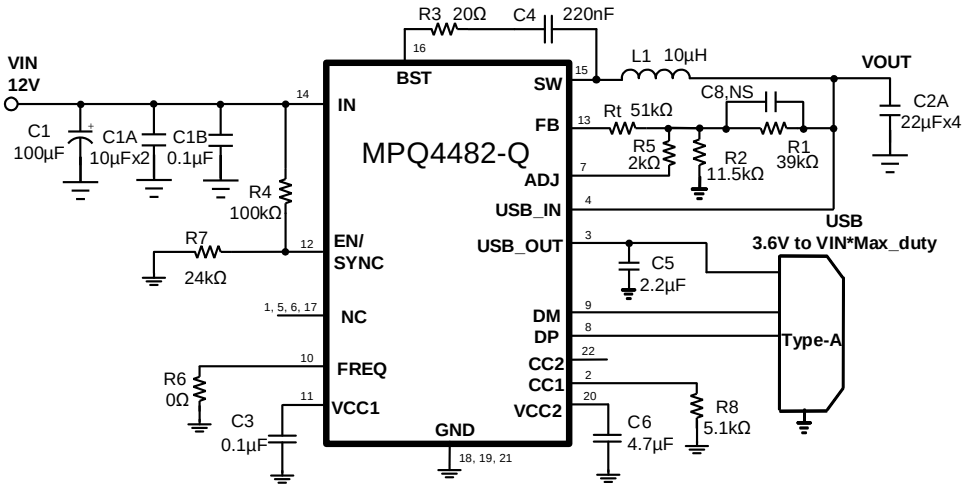
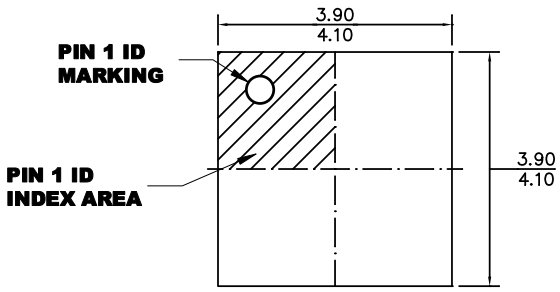


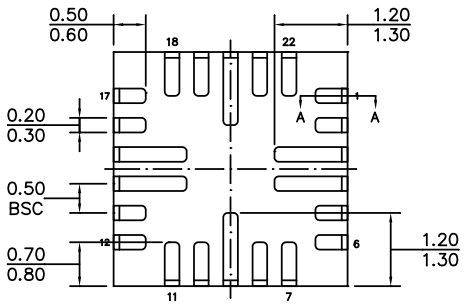
Figure 13: 12Vin, USB Type-A Port and QC3.0 mode

PACKAGE INFORMATION

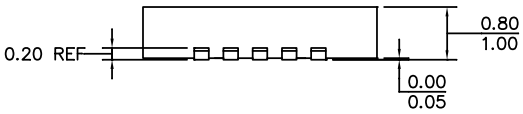
QFN-22 (4mmx4mm)



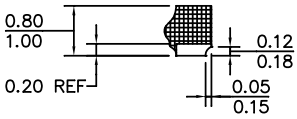
TOP VIEW



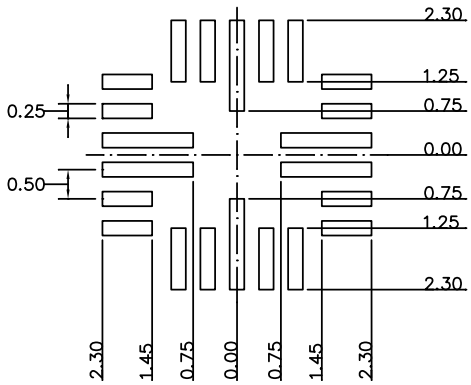
BOTTOM VIEW



SIDE VIEW



SECTION A-A

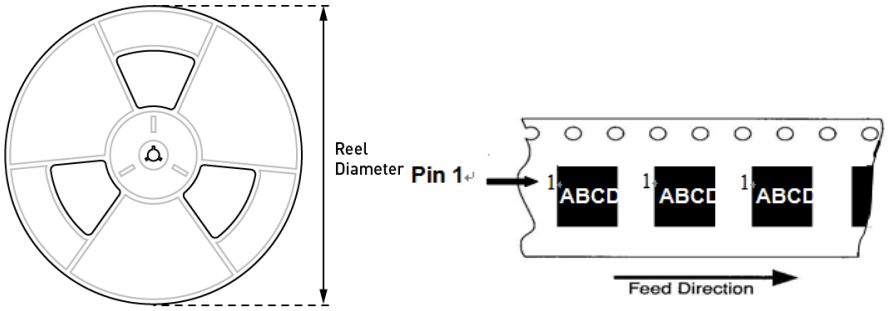


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHOULD BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4482GR-Q-AEC1-Z	QFN 4x4	5000	N/A	13in.	12mm	8mm