MPQ6628

40V, 0.8A, Octal Half-Bridge Motor Driver with Serial Input Control, AEC-Q100 Qualified

DESCRIPTION

The MPQ6628 is an 8-channel, half-bridge DMOS output driver with integrated power MOSFETs. The input voltage ranges between 5.5V and 40V, with an output current capability up to 0.8A.

The right half-bridges can be controlled separately via a standard serial data interface, and each half-bridge has various diagnostic functions. The device has very low quiescent current in standby mode.

Full protection includes short-circuit protection (SCP), under-voltage protection (UVP), and thermal shutdown.

The MPQ6628 requires a minimal number of readily available, standard external components. It is available in a TSSOP-28EP package.

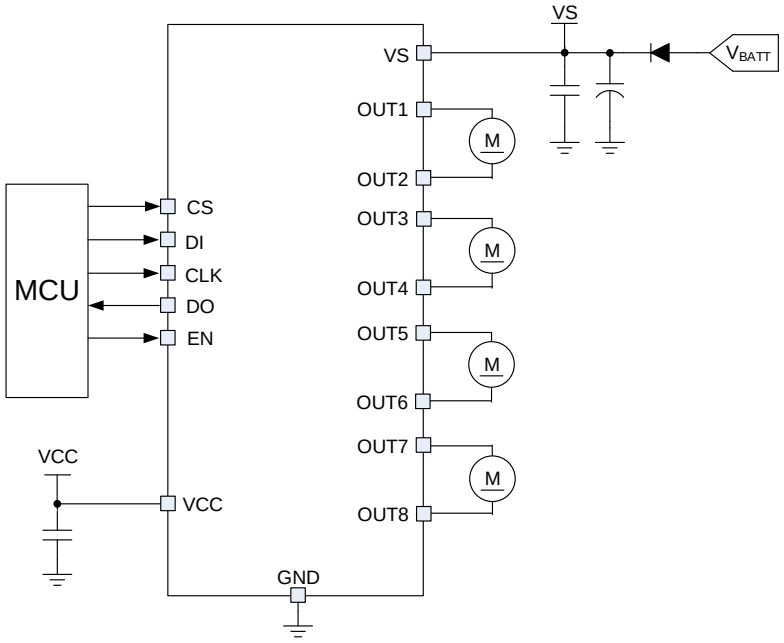
FEATURES

- Wide 5.5V to 40V Operating Input Range
- High-Side and Low-Side Drivers Connected in Half-Bridge Configurations
- Up to 0.8A Output Current
- Typical 1.3Ω $R_{DS(ON)}$ (HS + LS)
- Very Low Quiescent Current in Standby Mode versus Total Temperature Range
- Outputs Are Short-Circuit Protected
- Over-Temperature Protection and Pre-Warning
- Under-Voltage Lockout (UVLO) and Over-Voltage Lockout (OVLO)
- Serial Data Interface
- Diagnostic Functions include: Shorted Output, Open-Load, Over-Temperature (OT), Over-Voltage (OV), and Under-Voltage (UV)
- Serial Interface Clock Frequency Up to 5MHz
- Supports 3.3V and 5V Systems
- Available in a TSSOP-28EP Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive and Industrial Loads
- DC Motors

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ6628GF-AEC1	TSSOP-28EP	*See Below*	2A

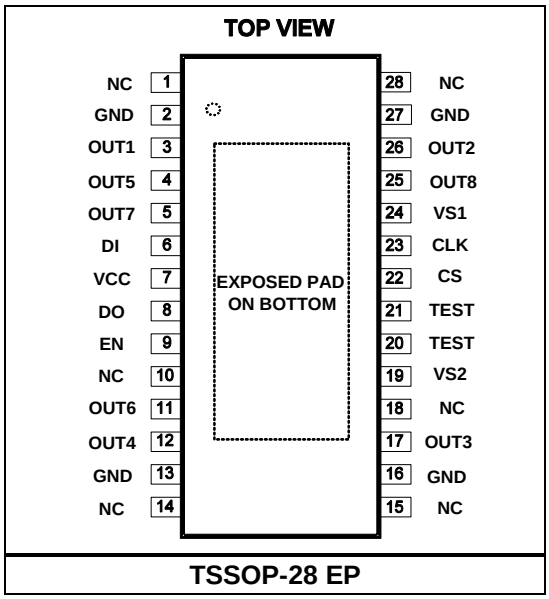
* For Tape & Reel, add suffix -Z (e.g. MPQ6628GF-AEC1-Z).

TOP MARKING

MPSYYWW
MP6628
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6628: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



TSSOP-28 EP

PIN FUNCTIONS

Pin #	Name	Description
1, 10, 14, 15, 18, 28	NC	**Not connected.**
2, 13, 16, 27	GND	**Ground.**
3	OUT1	**Half-bridge output 1.**
4	OUT5	**Half-bridge output 5.**
5	OUT7	**Half-bridge output 7.**
6	DI	**Serial data input.**
7	VCC	**Logic supply voltage**
8	DO	**Serial data output.**
9	EN	**Enable pin.** Pull this pin low to set the MPQ6628 to standby mode; pull it high to set the MPQ6628 to normal operation.
11	OUT6	**Half-bridge output 6.**
12	OUT4	**Half-bridge output 4.**
17	OUT3	**Half-bridge output 3.**
19	VS2	**Power supply for drivers 3, 4 and 6.** Connect this pin to VS1 externally.
20, 21	TEST	**Test pin for internal use.** Connect this pin to ground.
22	CS	**Chip selection input.** This pin is active low.
23	CLK	**Serial clock input.**
24	VS1	**Power supply for drivers 1, 2, 5, 7 and 8, all pre-drivers, and the charge pump.** Connect this pin to VS2 externally.
25	OUT8	**Half-bridge output 8.**
26	OUT2	**Half-bridge output 2.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{VS}) 45V
V_{OUTx} ..... -0.3V to V_{VS} +0.3V
Logic supply voltage (V_{VCC}) ..... -0.3V to +6V
Logic input voltage ..... -0.3 to V_{VCC} + 0.3V
Logic output voltage ..... -0.3 to V_{VCC} + 0.3V
All other pins ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
TSSOP-28EP 3.9W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings (3)

Human body model (OUTx and VSx pins) 4kV
Human body model (all other pins) 2kV
Machine mode (MM) 200V
Charged device model (CDM) 750V

Recommended Operating Conditions (4)

Supply voltage (V_{VS}) ..... 5.5V to 40V
Logic supply voltage (V_{VCC}) ..... 3.15V to 5.25V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance (5) θ_{JA} θ_{JC}

TSSOP-28EP	32	6 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Devices are ESD-sensitive. Handling precaution is recommended.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

5.5V ≤ V_{VS} ≤ 40V, 3.15V ≤ V_{VCC} ≤ 5.25V, EN = V_{VCC}, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Operating supply current (VS)	I_{VSO}	V_{VS} < 28V, EN = V_{CC}, no load		5.5	6.5	mA
Operating supply current (VCC)	I_{VCCO}	3.15V < V_{VCC} < 5.25V, EN = high, DI = CLK = low, CS = high, no load		100	150	µA
Quiescent current (VS)	I_{VSQ}	V_{VS} = 13.2V, V_{VCC} = 0V or V_{VCC} = 5V, EN = low		1	5	µA
Quiescent current (VCC)	I_{VCCQ}	3.15V < V_{VCC} < 5.25V, EN = low, DI = CLK = how, CS = high		1	5	µA
Discharge current (VS)	I_{VS}	V_{VS} = 40V, EN = low			3	mA
Power-on reset threshold	V_{VCC}	VCC increasing	2.3	2.7	3.0	V
Power-on reset delay		After switching on V_{VCC}	30	100	160	µs
VS under-voltage lockout (UVLO) threshold	V_{VS}	VS decreasing	3.5		4.5	V
VS UVLO threshold hysteresis	V_{UVOFF}		0.1	0.3	0.5	V
VS UVLO delay time			7		21	ms
VS over-voltage lockout (OVLO) threshold	V_{OVOFF}	OVLO = 1, VS increasing	33	36	39	V
VS OVLO threshold hysteresis			1	2.5	4	V
Output Specifications						
HS-FET + LS-FET on resistance	$R_{DS(ON)}$	T_J = -40°C to +125°C		1.3	2.2	Ω
		T_J = 150°C (7)			2.8	Ω
Over-current limit	I_{OCP}	V_{VS} = 13.2V	1	1.3	2.5	A
Over-current shutdown delay time	t_{D_OC}		10	25	50	µs
Open-load detection current	I_{OLD}	V_{VS} = 13.2V, LS-FET on	1	16	45	mA
Open-load delay time	t_{D_OLD}		200	350	600	µs
Output enable time		V_{VS} = 13.2V, R_{LOAD} = 50Ω		50	65	µs
Output disable time				50	65	
Delay time		HBCNFx high to OUTx high, V_{VS} = 13.2V, R_{LOAD} = 50Ω		75	105	
		HBCNFx low to OUTx low, V_{VS} = 13.2V, R_{LOAD} = 50Ω		65	95	
Output rise time		V_{VS} = 13.2V, 10% to 90% V_{OUT}, R_{LOAD} = 50Ω	13	27	42	µs
Output fall time			11	20	27	

ELECTRICAL CHARACTERISTICS *(continued)*

5.5V ≤ V_{VS} ≤ 40V, 3.15V ≤ V_{VCC} ≤ 5.25V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Dead time		V_{VS} = 13V, R_{LOAD} = 50Ω	1.5			µs
EN Input						
EN low-level threshold					0.6	V
EN high-level threshold			2.0			V
EN threshold hysteresis				0.4		V
Pull-down resistor		V_{EN} = V_{VCC}		125		kΩ
Serial Interface: DI, CLK, and CS Logic Inputs						
Input low-level threshold					0.6	V
Input high-level threshold			2.0			V
Input threshold hysteresis				150		mV
DI, CLK pin pull-down resistor		V_{DI}, V_{CLK} = V_{VCC}		125		kΩ
CS pin pull-up current		V_{CS} = 0V		125		kΩ
Input capacitance (6)	C_{IN}				15	pF
Serial Interface: DO Logic Output						
Output low level					0.4	V
Output high level			V_{VCC} - 0.6			V
Tri-state leakage current		0V < V_{DO} < V_{VCC}, V_{CS} = V_{VCC}	-5		+5	µA
Thermal Shutdown and Pre-Warning (6)						
Thermal pre-warning threshold	T_{JW}		120	140	170	°C
Thermal pre-warning hysteresis				20		°C
Thermal shutdown threshold	T_{JSD}		150	175	200	°C
Thermal shutdown hysteresis				20		°C
Ratio thermal shutdown/thermal pre-warning			1.05	1.2		

SERIAL INTERFACE TIMING CHARACTERISTICS (6)

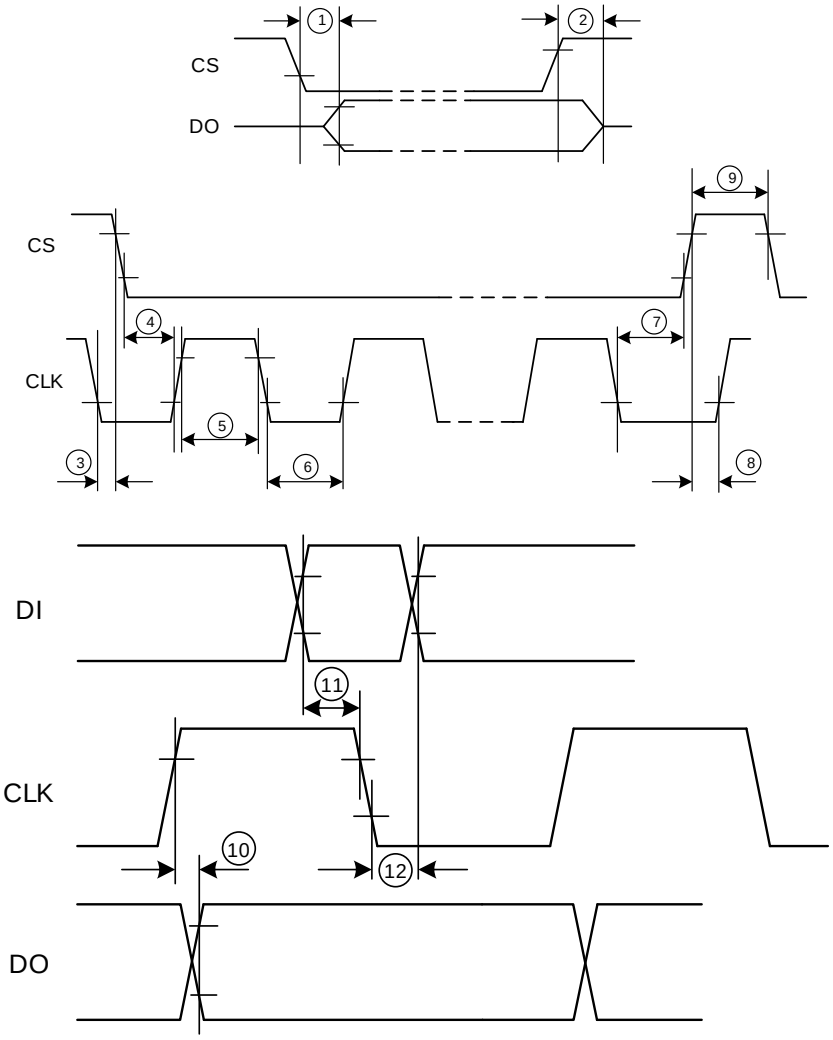
5.5V < V_{VS} < 40V, 3.15V ≤ V_{VCC} ≤ 5.25V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
CLK frequency	f_{CLK}				5	MHz
CLK period time	t_{pCLK}	VCC = 5V	200			ns
		VCC = 3.3V	500			
CLK high time	t_5		85			ns
CLK low time	t_6		85			ns
CLK set-up time (high to low)	t_7		85			ns
CLK set-up time (low to high)	t_3		85			ns
DI set-up time	t_{11}		50			ns
DI hold time	t_{12}		50			ns
CS set-up time (low to high)	t_8		100			ns
CS set-up time (high to low)	t_4		100			ns
CS high time	t_9		5			µs
DO enable after CS falling edge	t_1	C_{DO} = 40pF			200	ns
DO disable after CS rising edge	t_2	C_{DO} = 40pF			200	ns
DO falling/rising time		C_{DO} = 40pF		10	25	ns
DO valid time	t_{10}	C_{DO} = 40pF		20	50	ns
EN low valid time		VCC = 5V, EN high to low (50%) to OUTx turning off 50%		50		µs
EN high to SPI valid					100	µs
Time between two consecutive SRR commands			100			µs

Note:

6) Not tested in production. Specified by design.
7) Guaranteed by characterization data.

SERIAL TIMING INTERFACE DIAGRAM

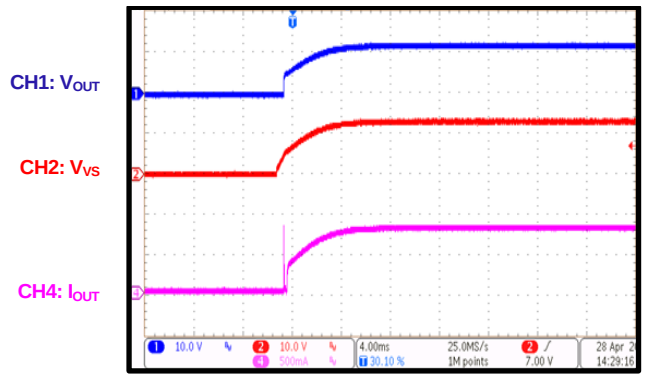


Inputs DI, CLK, and CS: High Level = 0.7 x V_{CC}, Low Level = 0.3 x V_{CC}
Output DO: High Level = 0.8 x V_{CC}, Low Level = 0.2 x V_{CC}

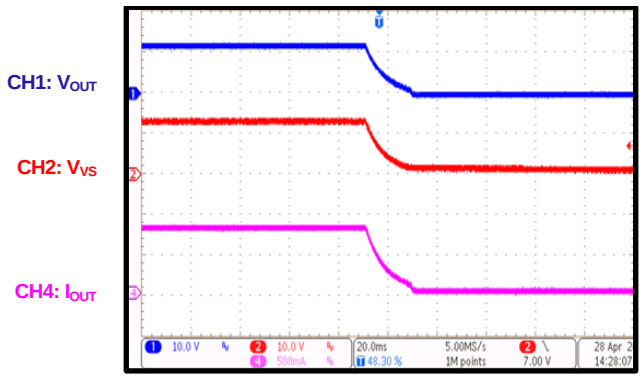
TYPICAL PERFORMANCE CHARACTERISTICS

V_{VS} = 13V, V_{VCC} = 3.3V, T_A = 25°C, unless otherwise noted.

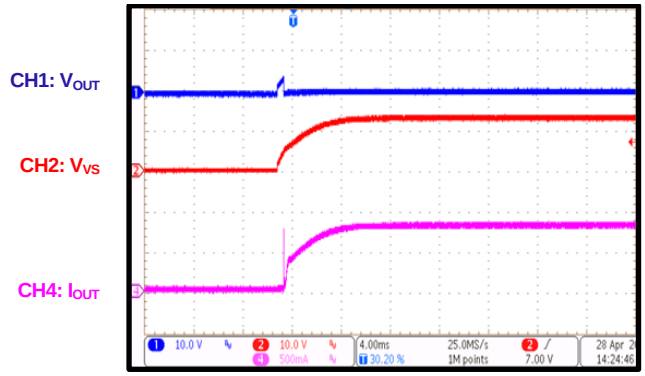
V_{VS} Start-Up
HS on, I_{OUT} = 800mA



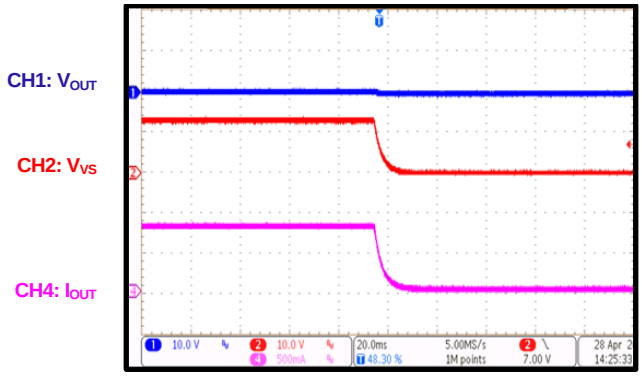
V_{VS} Shutdown
HS on, I_{OUT} = 800mA



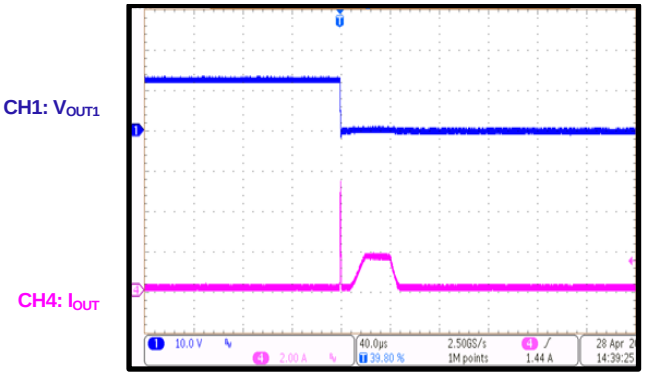
V_{VS} Start-Up
LS on, I_{OUT} = 800mA



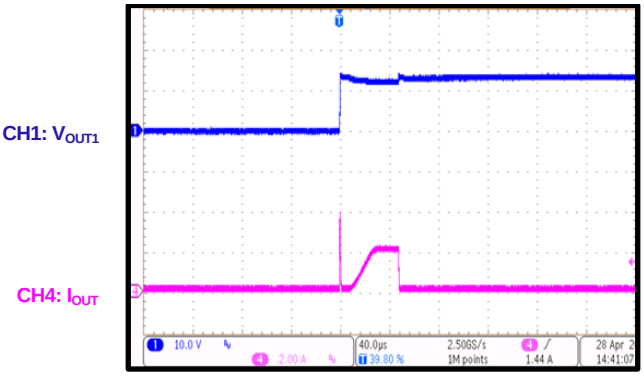
V_{VS} Shutdown
LS on, I_{OUT} = 800mA



OCP
OUT short to GND



OCP
OUT short to VS

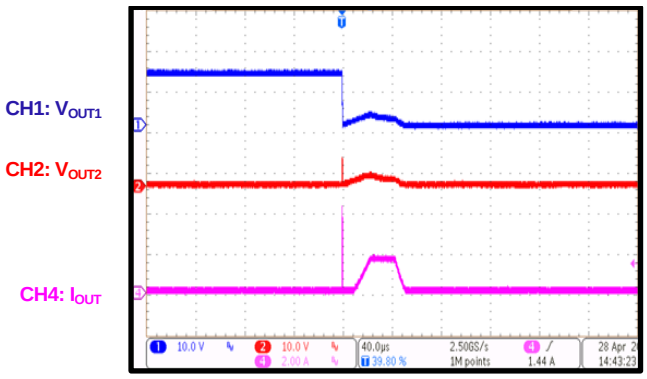


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{VS} = 13V, V_{VCC} = 3.3V, T_A = 25°C, unless otherwise noted.

OCP

Two outputs short circuit



BLOCK DIAGRAM

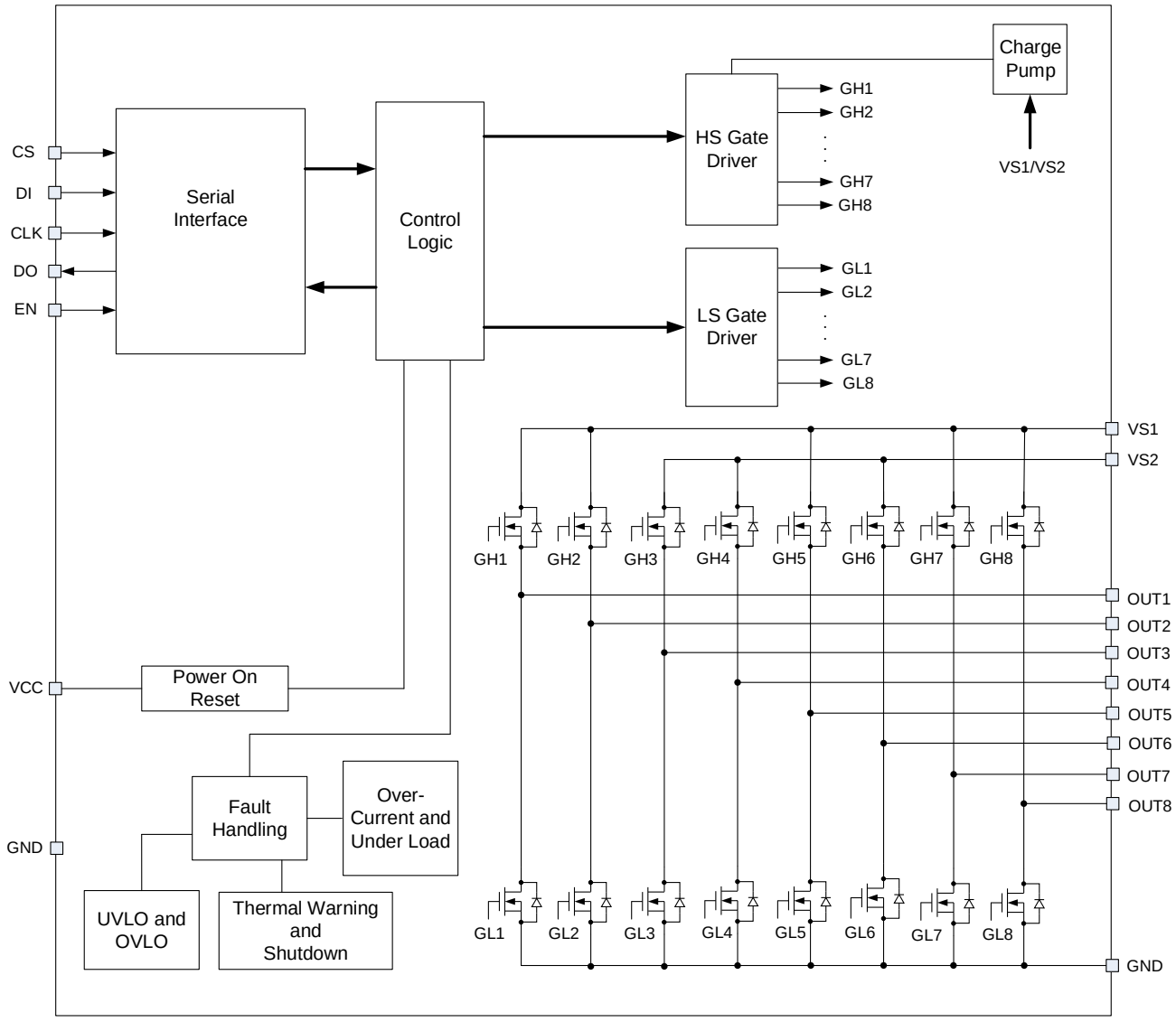


Figure 1: Functional Block Diagram

OPERATION

The MPQ6628 is an 8-channel half-bridge DMOS output driver with integrated power MOSFETs. The eight half-bridges of the MPQ6628 can be controlled separately from a standard serial data interface, and have various diagnostic functions.

Serial Interface

Data transfer starts with the falling edge of the CS signal. Execution of new input data is enabled on the rising edge of the CS signal. Data must appear when the DI pin is synchronized to the CLK pin. Then the data is accepted on the falling edge of the CLK signal. For DI, the MSB (SRR, bit[15]) has to be transferred first. The last 16 bits clocked into DI are transferred to the device's data register if there no frame error. Otherwise, all DI data is ignored, and the previous input data is preserved.

The output data at the DO pin is enabled on the falling edge of CS. In addition to the 16-bit status data, a pseudo-bit (PRE_15) can also be retrieved from the DO output. The latched thermal shutdown (TSD) status bit (PRE_15) is available on DO until the first rising CLK edge after CS goes low. DO changes its state with the rising edge of CLK, and remains stable until the next rising edge of CLK. When CS is high, the DO pin is in a tri-state condition.

The following conditions must be met for a valid TSD read to be captured:

- CLK and DI are low before the CS cycle
- CS transitions from high to low
- CS set-up time is satisfied

Figure 2 shows the SPI communication. Table 1 and Table 2 list the input control registers. Table 3 and Table 4 list the output diagnostic registers.

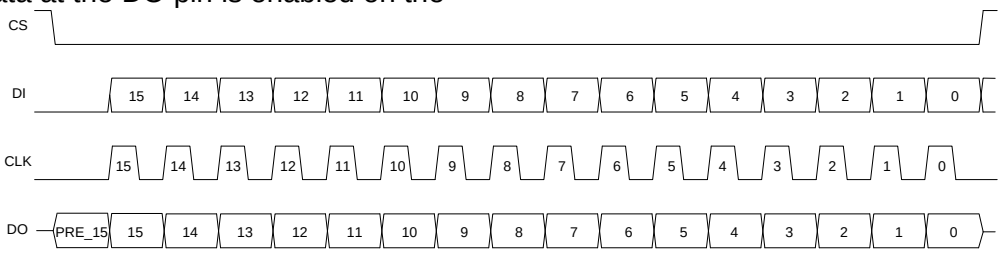


Figure 2: Data Transfer

Table 1: Input Control Registers (Channels 1–6, Input Bit[14] = 0)

Channels 1–6 (Input Bit[14] = 0)		
Bit	**Input Register**	**Function**
15	SRR	This bit resets the status register. 1: Reset. The errors bits of the corresponding status register in the output data register are set to low
14	CH_SEL	Channel Group Select = 0. 1: HB [8:7] 0: HB [6:1]
13	OLSD_EN	This bit enables open load detection shutdown (OLD_SD) for half-bridges 1–6. This feature allows the affected output stage to be switched off if a true open load or under-load condition has been detected. 1: Enabled
12	HBEN6	Enables half-bridge 6. 1: Half-bridge 6 is active 0: Half-bridge 6 is in Hi-Z

11	HBEN5	Enables half-bridge 5. 1: Half-bridge 5 is active 0: Half-bridge 5 is in Hi-Z
10	HBEN4	Enables half-bridge 4. 1: Half-bridge 4 is active 0: Half-bridge 4 is in Hi-Z
9	HBEN3	Enables half-bridge 3. 1: Half-bridge 3 is active 0: Half-bridge 3 is in Hi-Z
8	HBEN2	Enables half-bridge 2. 1: Half-bridge 2 is active 0: Half-bridge 2 is in Hi-Z
7	HBEN1	Enables half-bridge 1. 1: Half-bridge 1 is active 0: Half-bridge 1 is in Hi-Z
6	HBCNF6	Configures half-bridge 6. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
5	HBCNF5	Configures half-bridge 5. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
4	HBCNF4	Configures half-bridge 4. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
3	HBCNF3	Configures half-bridge 3. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
2	HBCNF2	Configures half-bridge 2. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
1	HBCNF1	Configures half-bridge 1. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
0	OVLO	This bit enables VSx over-voltage lockout (OVLO). 1: Enabled

Table 2: Input Control Registers (Channels 7–8, Input Bit[14] = 1) (8)

Channels 7–8 (Input Bit[14] = 1)		
Bit	**Input Register**	**Function**
15	SRR	Status register reset 1: Reset. The errors bits of the corresponding status register in the output data register are set to low
14	CH_SEL	Channel Group Select = 1. 1: HB [8:7] 0: HB [6:1]
13	OLSD_EN	This bit enables open load detection shutdown (OLD_SD) for half-bridges 7 and 8. This feature allows the affected output stage to be switched off if a true open load or under-load condition has been detected. 1: Enabled
12	RESERVED	Reserved.
11	RESERVED	Reserved.
10	RESERVED	Reserved.
9	RESERVED	Reserved.
8	HBEN8	Enables half-bridge 8. 1: Half-bridge 8 is active 0: Half-bridge 8 is in Hi-Z
7	HBEN7	Enables half-bridge 8. 1: Half-bridge 8 is active 0: Half-bridge 8 is in Hi-Z
6	RESERVED	Reserved.
5	RESERVED	Reserved.
4	RESERVED	Reserved.
3	RESERVED	Reserved.
2	HBCNF8	Configures half-bridge 8. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
1	HBCNF7	Configures half-bridge 7. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
0	OVLO	This bit enables VSx over-voltage lockout. 1: Enabled

Note:

8) All input bits are set to 0 after there is a VCC power-on reset.

Table 3: Output Diagnostic Registers (Channels 1–6, Input Bit[14] = 0)

Channels 1–6 (Input Bit[14] = 0)		
Bit	**Input Register**	**Function**
PRE_15	TSD	This bit indicates if latched thermal shutdown occurs. The error is latched and the corresponding output is switched off if thermal shutdown occurs. The bit can only be reset via SRR or a power-on reset. 1: Thermal shutdown has occurred
15	OC (HB [6:1])	This bit indicates if latched over-current (OC) shutdown occurs. If an OC fault (e.g. an overload or short-circuit fault) is detected on any half-bridge between half-bridge 1 and half-bridge 6, the error is latched, and the corresponding output is switched off. The bit can only be reset via SRR or a power-on reset. 1: An OC fault has occurred
14	PSF	This bit indicates if a power supply failure occurs. This bit is set if there is an over-voltage or under-voltage condition on VS1 or VS2, and all outputs switch off. This bit automatically resets if VSx returns to its normal operating range. 1: A power supply failure has occurred
13	OLD (HB [6:1])	This bit indicates if an open load fault has occurred. If there is a true open load or under-load condition on any half-bridge between half-bridge 1 and half-bridge 6, the error is latched. The corresponding output is switched off if input bit[13] (OLD_SD) is high. The bit can only be reset via SRR or a power-on reset. 1: An open load fault has occurred
12	SHBEN6	Half-bridge 6 output status. 1: Half-bridge 6 is active 0: Half-bridge 6 is in Hi-Z
11	SHBEN5	Half-bridge 5 output status. 1: Half-bridge 5 is active 0: Half-bridge 5 is in Hi-Z
10	SHBEN4	Half-bridge 4 output status. 1: Half-bridge 4 is active 0: Half-bridge 4 is in Hi-Z
9	SHBEN3	Half-bridge 3 output status. 1: Half-bridge 3 is active 0: Half-bridge 3 is in Hi-Z
8	SHBEN2	Half-bridge 2 output status. 1: Half-bridge 3 is active 0: Half-bridge 2 is in Hi-Z
7	SHBEN1	Half-bridge 1 output status. 1: Half-bridge 1 is active 0: Half-bridge 1 is in Hi-Z
6	HBCNF6	Half-bridge 6 configuration status. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on

5	HBCNF5	Half-bridge 5 configuration status. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
4	HBCNF4	Half-bridge 4 configuration status. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
3	HBCNF3	Half-bridge 3 configuration status. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
2	HBCNF2	Half-bridge 2 configuration status. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
1	HBCNF1	Half-bridge 1 configuration status. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
0	TW	This bit indicates if a thermal warning has been detected. This bit is treated as an early warning, and is set high if the junction temperature reaches T_{JW}. The output remains on until one or more sensors reach T_{SD}. This bit automatically resets if the junction temperature drops below the thermal warning recovery point. 1: A thermal warning has been detected

Table 4: Output Diagnostic Registers (Channels 7–8, input Bit[14] = 1)

Channels 7–8 (Input Bit[14] = 1)		
Bit	**Input Register**	**Function**
PRE_15	TSD	This bit indicates if latched thermal shutdown occurs. The error is latched and the corresponding output is switched off if thermal shutdown occurs. The bit can only be reset via SRR or a power-on reset. 1: Thermal shutdown has occurred
15	OC (HB [8:7])	This bit indicates if latched over-current (OC) shutdown occurs. If an OC fault (e.g. an overload or short-circuit fault) is detected on half-bridge 7 or half-bridge 8, the error is latched, and the corresponding output is switched off. The bit can only be reset via SRR or a power-on reset. 1: An OC fault has occurred
14	PSF	This bit indicates if a power supply failure occurs. This bit is set if there is an over-voltage or under-voltage condition on VS1 or VS2, and all outputs switch off. This bit automatically resets if VSx returns to its normal operating range. 1: A power supply failure has occurred
13	OLD (HB [8:7])	This bit indicates if an open load fault has occurred. If there is a true open load or under-load condition on half-bridge 7 or half-bridge 8, the error is latched. The corresponding output is switched off if input bit[13] (OLD_SD) is high. The bit can only be reset via SRR or a power-on reset. 1: An open load fault has occurred
12	RESERVED	Reserved.

11	RESERVED	Reserved.
10	RESERVED	Reserved.
9	RESERVED	Reserved.
8	SHBEN8	Half-bridge 8 output status. 1: Half-bridge 8 is active 0: Half-bridge 8 is in Hi-Z
7	SHBEN7	Half-bridge 7 output status. 1: Half-bridge 7 is active 0: Half-bridge 7 is in Hi-Z
6	RESERVED	Reserved.
5	RESERVED	Reserved.
4	RESERVED	Reserved.
3	RESERVED	Reserved.
2	HBCNF8	Half-bridge 8 configuration status. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
1	HBCNF7	Half-bridge 7 configuration status. 1: The high-side (HS) half-bridge is on, and the low-side (LS) half-bridge is off 0: The HS half-bridge is off, and the LS half-bridge is on
0	TW	This bit indicates if a thermal warning has been detected. This bit is treated as an early warning, and is set high if the junction temperature reaches T_{JW}. The output remains on until one or more sensors reach T_{SD}. This bit automatically resets if the junction temperature drops below the thermal warning recovery point. 1: A thermal warning has been detected

Enable Control

The MPQ6628 enters low-power mode (or sleep mode) when the EN pin is pulled low. The EN input has an internal pull-down resistor. In sleep mode, all output stages turn off, and the SPI register banks are reset. The output stages can be activated again by pulling EN high.

Status Register Reset (SRR)

The status register reset (SRR) command bit is executed at the end of the SPI transmission (CS low to high). Sending SRR = 1 clears the status memory and reactivates faulted outputs for channels (as selected by CH_SEL).

If a fault is still present when SRR is sent, the protection can be triggered, and the device may shutdown again. The device can be reset by toggling the EN pin or by a VCC power-on reset.

Open-Load Detection (OLD)

While the device is on, open-load detection (OLD) is implemented in the low-side (LS) switches of the bridge outputs. If the current through the LS transistor is below the reference current (I_{OLD}) for longer than the OLD delay time (t_{DOLD}), the corresponding OLD diagnostic bit is set. If an under-load condition occurs in another channel after the global timer has started, the delay for any subsequent under-load condition is the remainder of the timer. The timer runs continuously if the under-load condition remains.

If the OLSD_EN bit is set, and an open load is detected on the LS switch, the respective output is disabled, and the open load error bit is latched. Otherwise, the output remains on, and only the open load error bit is set. If OLSD_EN is set, the

error remains latched, and the output stays off until an SRR or power-on reset is performed. The channel group selection input bit (CH_SEL) determines which channels are affected by SRR, and also determines which half-bridges are latched off via the OLSD_EN bit. This provides the advantage of independently diagnosing and isolating error flags to the corresponding failed output.

For example, consider a motor that is connected between outputs OUT1 and OUT2 with a broken wire (see Figure 3). Table 5 shows the corresponding diagnostic information.

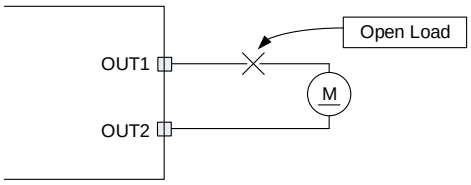


Figure 3: Half-Bridge Open Load Example

Table 5: Open Load Diagnostic Example

Control				Diagnostic Information	
				Motor Connected	Motor Disconnected
LS1	HS1	LS2	HS2	OLD (Output Bit[13])	
0	0	0	0	0	0
1	0	0	1	0	1
0	1	1	0	0	1
0	1	0	1	0	0
1	0	1	0	1	1

In motor applications, it is often advantageous to actively brake the motor by turning on both high-side (HS) or low-side (LS) drivers in two half-bridge channels. If the configuration has two LS drivers (LS brake), an under-load condition occurs as the motor current decays normally. Use an HS brake to avoid an under-load notification.

Discharge Circuit

Many typical applications use an inverse-polarity protection diode (e.g. D1) (see Figure 4).

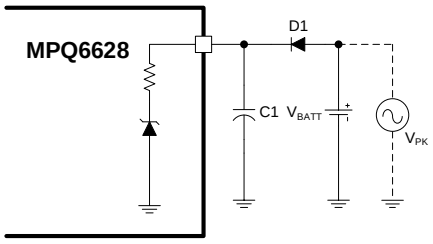


Figure 4: Functional Principle of the Discharger Circuit

However, this method poses certain risks. During inhibit mode, the IC consumes an extremely low current (I_{VS}) that is about 20µA maximum. Any peaks on the supply voltage gradually charge the blocking capacitor.

D1 prevents the capacitor from discharging via the power supply. Due to the extremely small quiescent current, discharging via the IC can also be ignored. This means that during long periods in inhibit mode, the IC's supply voltage could increase continuously, until the device exceeds the maximum supply voltage limit (about 40V). This could damage the IC.

The MPQ6628 features a discharger circuit to protect the device. If the VS voltage exceeds its threshold (about 37V), the blocking capacitor is discharged via an integrated resistor until VS falls below the threshold.

Diagnostics Overview

Table 6 on page 20 lists the diagnostic classes and functions.

Table 6: Diagnostic Classes and Functions

Fault	Qualifier	State and Recovery	
		OUTx	Output Register
Thermal shutdown	-	Hi-Z, use SRR to reset	TSD = 1, use SRR to reset
Over-current Shutdown	-		OC = 1, use SRR to reset
Open-load detection	OLSD_EN= 1		OLD = 1, use SRR to reset
	OLSD_EN = 0	Unaffected	
Over-voltage lockout	OVLO = 1	Hi-Z, unlatched (9)	PSF = 1, unlatched (10)
	OVLO = 0	Unaffected	
Under-voltage lockout	-	Hi-Z, unlatched (9)	
Thermal warning	-	Unaffected	TW = 1, unlatched (10)

Notes:

9) OUTx returns to its previous state if fault is removed.
10) The corresponding output register returns to its no-fault state if fault is removed

Over-Current Protection (OCP)

The MPQ6628 has internal overload and short-circuit protection (SCP). The currents in both the high-side and low-side MOSFETs are measured, and if the current exceeds the current limit, an internal timer starts. If the permanent over-current shutdown delay time (t_{OC}) is reached, the short-circuit detection bit (OC) is set, and the shorted output is disabled. Reset the OC bit and enable the disabled output by writing a high to the SRR bit in the input register. The channel group selection input bit (CH_SEL) determines which channels are affected by SRR.

Thermal Shutdown and Thermal Pre-Warning

Thermal monitoring is integrated into the MPQ6628. Each half-bridge monitors the driver pair's (one channel including the high-side and low-side MOSFETs) thermal sensor. If the junction temperature rises above the thermal pre-warning threshold, the temperature pre-warning bit (TW) in the output register is set. When the temperature falls below the thermal pre-warning threshold, this bit is reset.

If the junction temperature rises above the thermal shutdown threshold, the channel's HS and LS drivers latch off, the TW bit remains set, and the TSD (PRE_15) bit is set. The TSD bit is cleared, and all affected channels in a group resume immediately once the following conditions are met:

- The junction temperature falls below the thermal shutdown threshold
- A high has been written to the SRR bit in the input register.

The channel group selection input bit (CH_SEL) determines which channels are affected by SRR.

The thermal pre-warning and shutdown thresholds have hysteresis values.

VS Under-Voltage Lockout (UVLO)

If the voltage on the VS pin falls below the under-voltage lockout (UVLO) threshold, an internal timer starts. The power supply fail bit (PSF) in the output register is set, and all outputs are disabled if the permanent UVLO delay time is reached. Operation resumes immediately when VS rises above the UVLO threshold, and the PSF bit is cleared.

VCC Under-Voltage Lockout (UVLO)

The SPI interface does not function if VCC is below the under-voltage lockout (UVLO) threshold. If this occurs, all outputs turn off, then the input and status output registers are cleared.

Once the VCC voltage rises above the under-voltage threshold, the under-voltage bit is reset, and SRR is released

VS Over-Voltage Lockout (OVLO)

If the supply voltage on VS rises above the switch off voltage (V_{OVOFF}), all outputs switch off if the over-voltage lockout input bit is set (OVLO = 1), and the PSF error bit is set. The error is not latched. This means that if the VS voltage falls below the switch-on threshold, the power stages restart, and the error flags reset.

APPLICATION INFORMATION

PCB Layout Guidelines

PCB layout is critical for the stable operation. For the best results, follow the guidelines below:

1. Place a supply-rated X5R or X7R bypass capacitor as close as possible to the IC.
2. Place as much copper as possible on the long pads.
3. Place thermal vias inside the pad area to dissipate heat to the copper layers. Place vias just outside the pad area if via-in-pad construction is not applicable.
4. Place a bulk capacitor on the VS pin to absorb the energy flowing from the motor or power supply. This capacitor should be sized according to the application requirements.

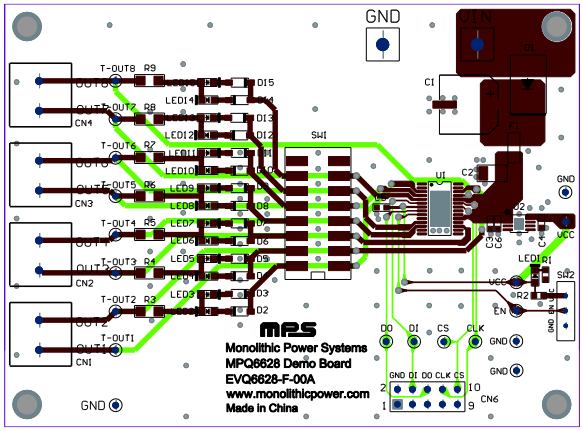
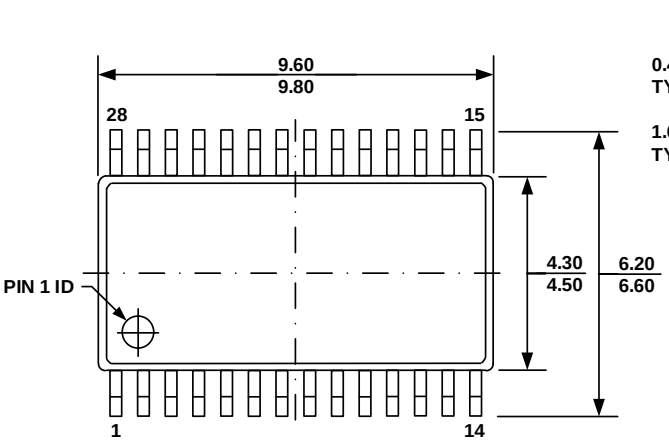


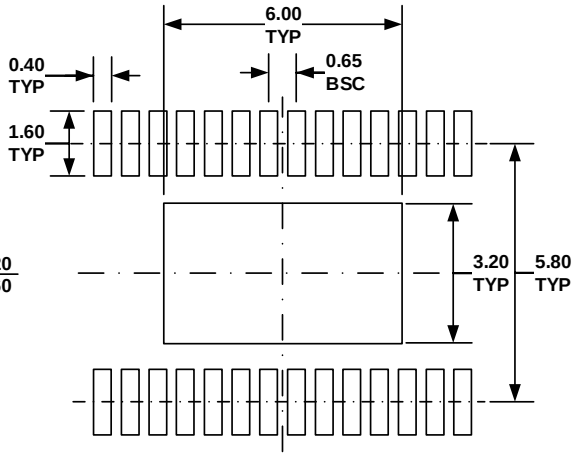
Figure 5: Recommended PCB Layout

PACKAGE INFORMATION

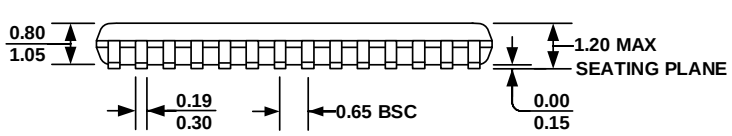
TSSOP-28EP



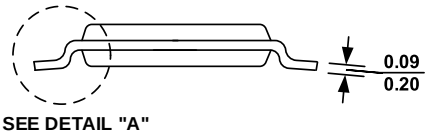
TOP VIEW



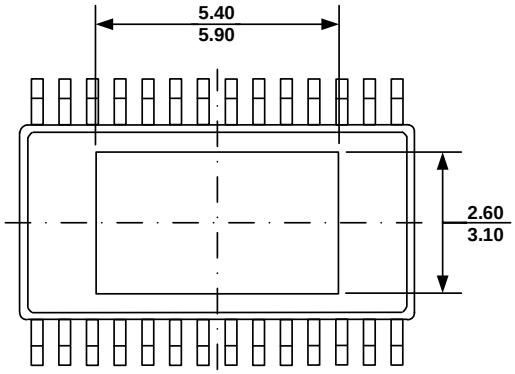
RECOMMENDED LAND PATTERN



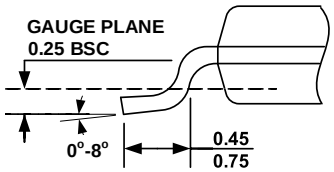
FRONT VIEW



SIDE VIEW



BOTTOM VIEW

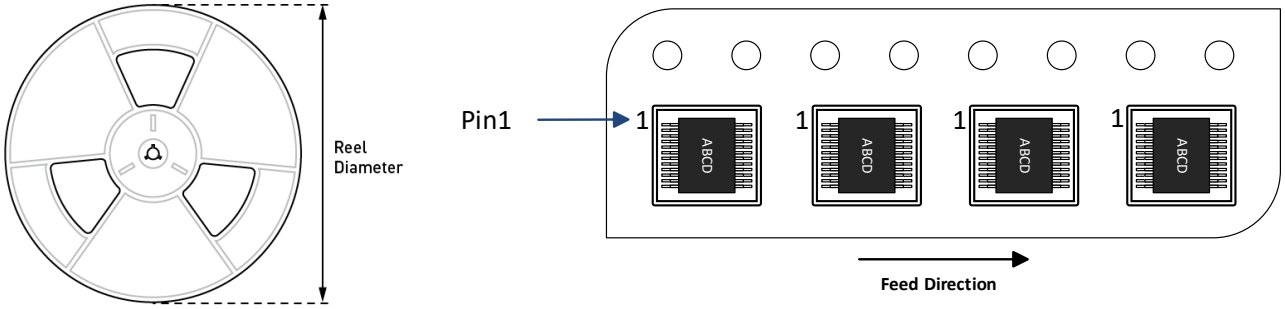


DETAIL “A”

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6628GF-AEC1-Z	TSSOP-28EP	2500	50	13in	16mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/08/2021	Initial Release	-