MP2018

16V, 500mA, Low Quiescent Current Linear Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP2018 is a low-power linear regulator that supplies power to systems with high-voltage batteries. The MP2018 includes a wide 3V to 16V input voltage range, low dropout voltage, and low quiescent supply current. The low quiescent current and low dropout voltage allow the MP2018 to operate at extremely low power levels. Therefore, the MP2018 is ideal for low-power microcontrollers and battery-powered equipment.

The MP2018 provides two fixed output voltage options: 3.3V and 5.0V.

The regulator output current is limited internally, and the device is protected against short-circuit, overload, and over-temperature conditions. The MP2018 also includes thermal shutdown and current-limiting fault protection.

The MP2018 is available in a TO252-5 package.

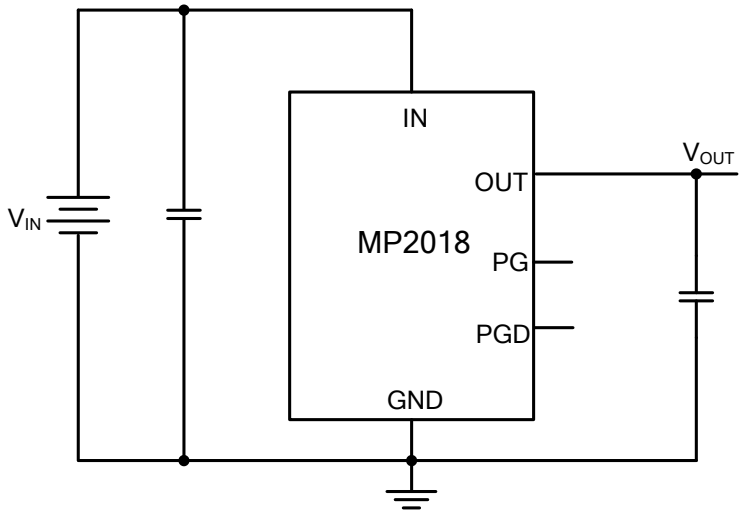
FEATURES

- 3V to 16V Input Range
- 10µA Quiescent Supply Current
- Stable with Low-Value Output Ceramic Capacitor (>0.47µF)
- 500mA Specified Current
- Fixed Output Voltage
- Output ±2% Accuracy
- Specified Current Limit
- Power Good
- Programmable Power Good Delay
- Thermal Shutdown and Short-Circuit Protection (SCP)
- -40°C to +150°C Specified Junction Temperature Range
- Available in a TO252-5 Package

APPLICATIONS

- Portable/Battery-Powered Equipment
- Ultra-Low Power Microcontrollers
- Cellular Handsets
- Medical Imaging

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2018GZD-33	TO252-5	*See Below*
MP2018GZD-5	TO252-5	*See Below*

* For Tape & Reel, add suffix –Z (e.g.: MP2018GZD-5–Z).

TOP MARKING (MP2018GZD-33)

MPS YYWW
MP2018-33
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP2018-33: Part number
LLLLLLLLL: Lot number

TOP MARKING (MP2018GZD-5)

MPS YYWW
MP2018-5
LLLLLLLLL

MPS: MPS prefix
YY: Year code
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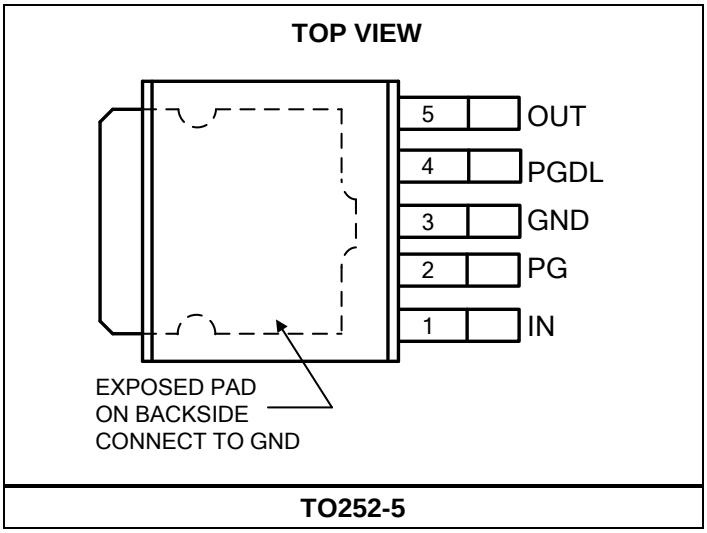
PACKAGE REFERENCE



TO252-5

ABSOLUTE MAXIMUM RATINGS (1)

IN..... -0.3V to +20V
OUT..... -0.3V to +17V
PG ..... -0.3V to +15V
PGDL..... -0.3V to +6V
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C
Continuous power dissipation (T_A = +25°C) (2)
TO252-5 ..... 2.27W

ESD Susceptibility (3)

Human body mode (HBM) 4kV
Machine mode (MM)..... 200V

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) ..... 3V to 16V
Operating temperature.... T_A = -40°C to +125°C,
$T_A \le T_J \le$ +150°C

Thermal Resistance (5) θ_{JA} θ_{JC}

TO252-5..... 55..... 3 .... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Devices are ESD-sensitive. Handling precaution is recommended.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 13.5V, T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
GND pin current	I_{GND}	0 < I_{OUT} < 1mA		12	17	µA
		1mA < I_{OUT} < 30mA		16	22	
		30mA < I_{OUT} < 500mA		105	150	
Load current limit	I_{LIMIT}	V_{OUT} = 0V	550	900	1450	mA
Output voltage accuracy		MP2018GZD-5, V_{IN} = 6V to 16V, I_{LOAD} = 5mA	4.9	5	5.1	V
		MP2018GZD-33, V_{IN} = 4.3V to 16V, I_{LOAD} = 5mA	3.234	3.3	3.366	
Dropout voltage (6)	$V_{DROPOUT}$	MP2018GZD-5, I_{LOAD} = 300mA, $V_{DROPOUT}$ = V_{IN} - V_O		400	650	mV
		MP2018GZD-33, I_{LOAD} = 300mA, $V_{DROPOUT}$ = V_{IN} - V_O		500	700	
		MP2018GZD-5, I_{LOAD} = 500mA, $V_{DROPOUT}$ = V_{IN} - V_O		750	1000	
		MP2018GZD-33, I_{LOAD} = 500mA, $V_{DROPOUT}$ = V_{IN} - V_O		1000	1300	
Line regulation		V_{IN} = 8V to 16V, I_{LOAD} = 5mA	-10	1	10	mV
Load regulation		I_{LOAD} = 5mA to 500mA		1	15	mV
Output voltage PSRR (7)		100Hz, C_{OUT} = 10µF, I_{LOAD} = 10mA		57		dB
		1kHz, C_{OUT} = 10µF, I_{LOAD} = 10mA		45		dB
		100kHz, C_{OUT} = 10µF, I_{LOAD} = 10mA		51		dB
Startup response time		MP2018GZD-5, I_{LOAD} = 10mA, C_{OUT} = 22µF		1	2	ms
		MP2018GZD-33, I_{LOAD} = 10mA, C_{OUT} = 22µF		0.6	1.5	
PG rising threshold			90%	93%	96%	V_{OUT}
PG rising threshold hysteresis				5%		V_{OUT}
PG low voltage		Sink 1mA current		0.1	0.4	V
PG leakage current		V_{PG} = 5V			1	µA
PGDL charging current	I_{PGDL}	V_{PGDL} = 1V	3	5.5	9	µA
PGDL rising threshold			1.5	1.65	2	V
PGDL falling threshold			0.2	0.4	0.7	V
PG delay time	t_{PGDL}	C_{PGDL} = 47nF, 10% to 90% PGDL rising threshold	6	11	14	ms
PG reaction time		C_{PGDL} = 47nF		0.5	2	µs
Thermal shutdown (7)	T_{SD}			165		°C
Thermal shutdown hysteresis (7)	ΔTSD			30		°C

NOTES:

6) Dropout voltage: Measured when the output voltage (V_{OUT}) has dropped 100mV from the nominal value obtained at V_{IN} = 13.5V.

1) Derived from bench characterization. Not tested in production.

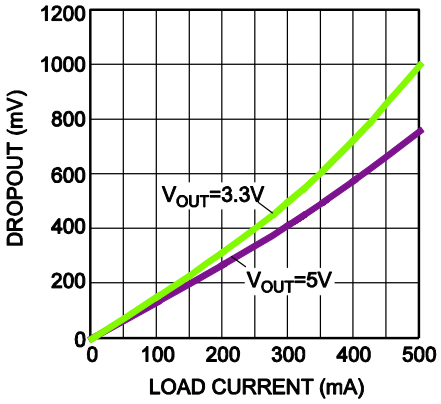
PIN FUNCTIONS

Pin #	Name	Description
1	IN	**Input voltage.** Connect a 3V to 16V supply to IN.
2	PG	**Power good.**
3	GND	**Ground.** GND is connected to the exposed pad internally. GND and the exposed pad must be connected to the same ground plane.
4	PGDL	**Programmable power good delay time.**
5	OUT	**Regulated output voltage.** Connect a low-value ceramic capacitor (≥0.47μF) to the output for stability.

TYPICAL PERFORMANCE CHARACTERISTICS

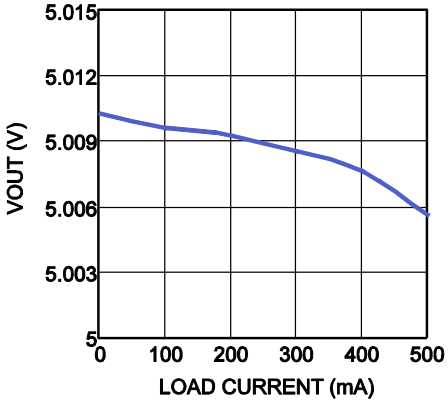
C_{IN} = 1µF, C_{OUT} = 22µF, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

Dropout vs. Load Current



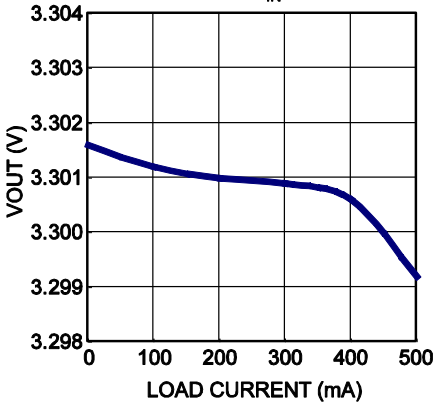
V_{OUT} vs. I_{OUT}

MP2018GZD-5, V_{IN}=6V



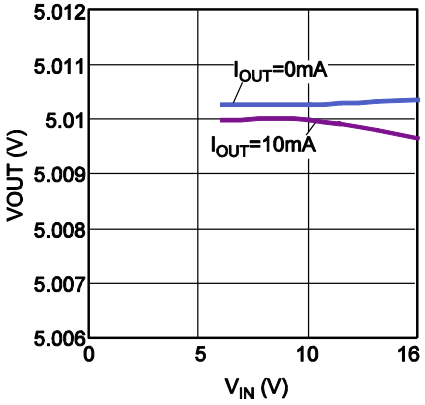
V_{OUT} vs. I_{OUT}

MP2018GZD-33, V_{IN}=4.5V



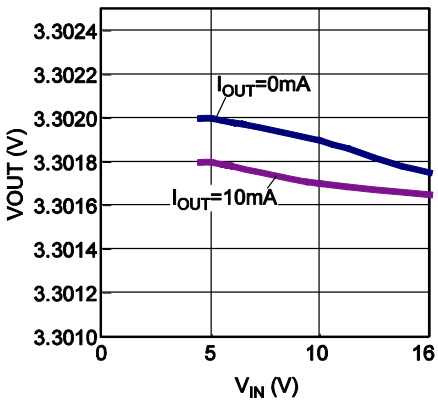
V_{OUT} vs. V_{IN}

MP2018GZD-5



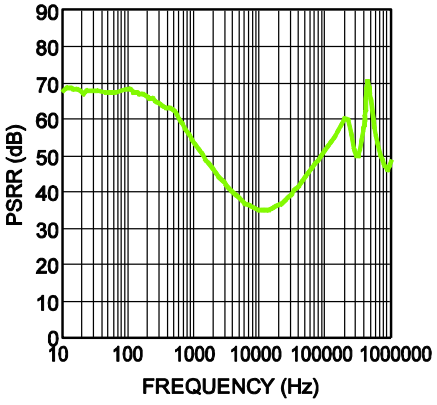
V_{OUT} vs. V_{IN}

MP2018GZD-33



PSRR vs. Frequency

C_{IN}=100pF, C_{OUT}=10µF, I_{OUT}=10mA

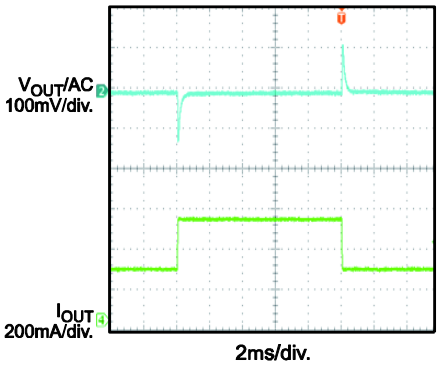


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 1µF, C_{OUT} = 22µF, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

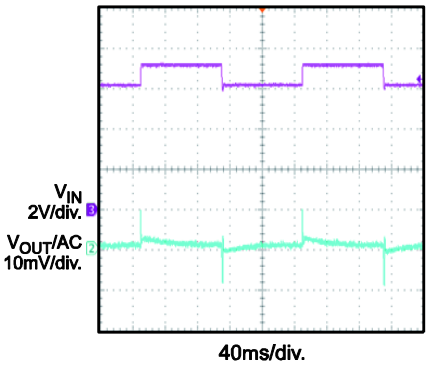
Load Transient

V_{IN}=12V, I_{OUT}=250mA-500mA



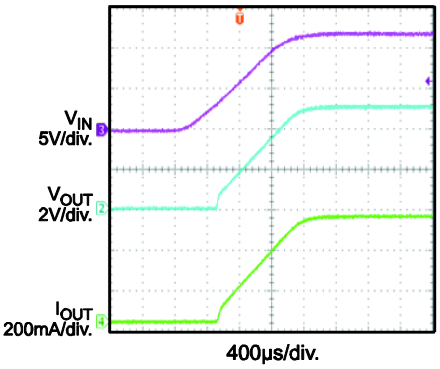
Line Transient

V_{IN}=6V-7V, I_{OUT}=500mA



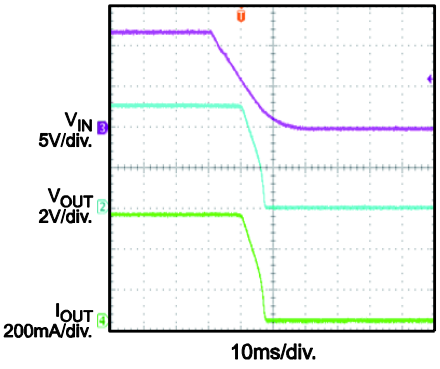
Start-Up through V_{IN}

V_{IN}=12V, I_{OUT}=500mA



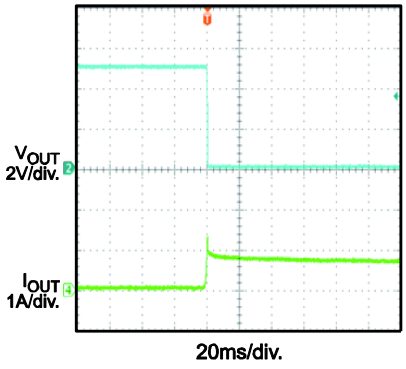
Shutdown through V_{IN}

V_{IN}=12V, I_{OUT}=500mA



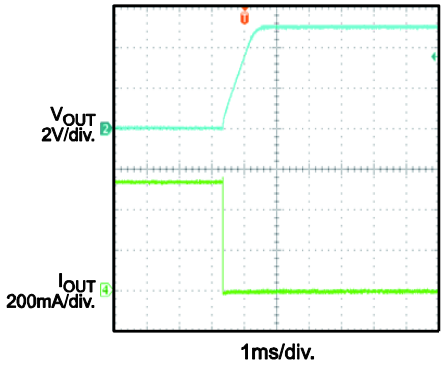
Short-Circuit Entry

I_{OUT}=0mA to Short Circuit



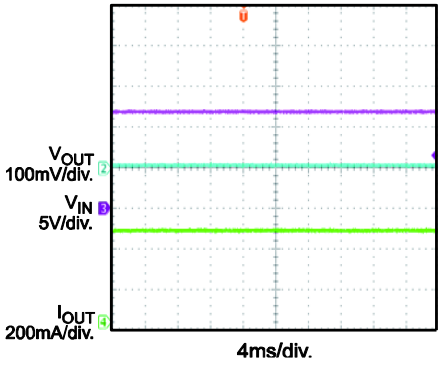
Short-Circuit Recovery

Short Circuit to I_{OUT}=0mA



Short-Circuit Steady State

V_{IN}=12V



BLOCK DIAGRAM

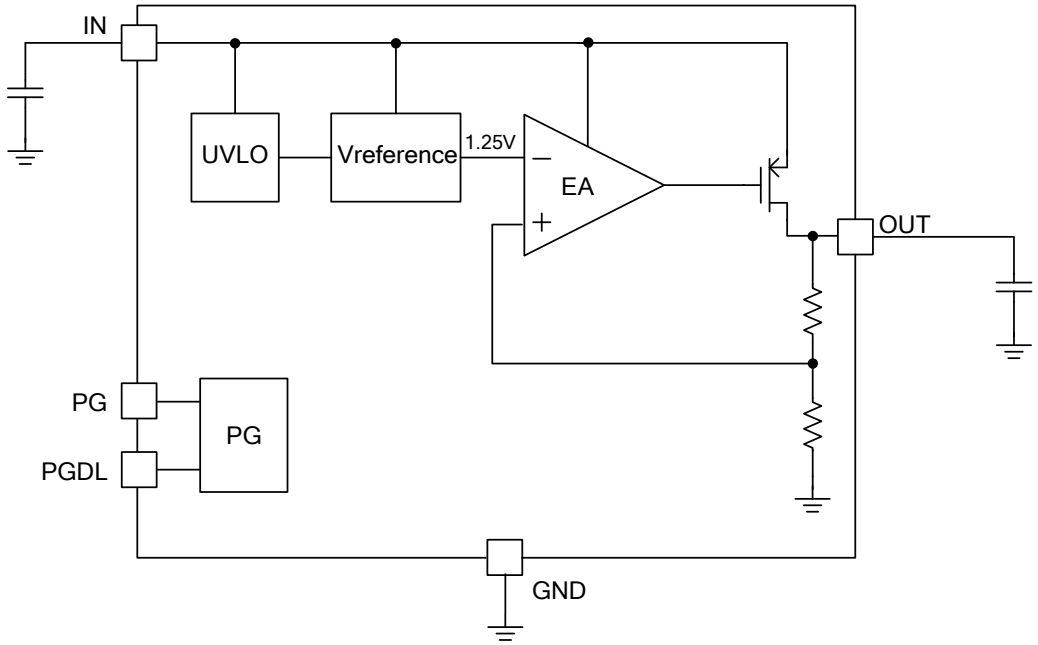


Figure 1: Functional Block Diagram

OPERATION

The MP2018 is a linear regulator that supplies power to systems with high-voltage batteries. The MP2018 includes a wide 3V to 16V input range, low dropout voltage, and low quiescent supply current.

Short-Circuit Protection (SCP)

The regulator output current is limited internally, and the device is protected against short-circuit and overload conditions. The peak output current is limited to around 900mA, which exceeds the 500mA recommended continuous output current.

Thermal Shutdown

When the junction temperature exceeds the upper threshold (165°C), the thermal sensor sends a signal to the control logic to shut down the IC. The IC restarts when the temperature has cooled sufficiently (135°C).

The maximum power output current is a function of the package's maximum power dissipation for a given temperature.

The maximum power dissipation depends on the thermal resistance of the case and the circuit board, the temperature difference between the die junction and the ambient air, and the rate of the air flow. GND and the exposed pad must be connected to the ground plane for proper dissipation.

Power Good (PG) Output

The MP2018 has a power good pin (PG). PG is the open drain of an internal MOSFET and should be connected to the output voltage (V_{OUT}) or an external voltage source (<15V) through a resistor (i.e.: 100kΩ). If V_{OUT} reaches 93% of the nominal value, the MOSFET turns off, and PG is pulled high by V_{OUT} or an external voltage source. When V_{OUT} drops to 88% of the nominal value, the PG voltage is pulled to GND.

There is a delay time when PG asserts high. The delay time can be programmed by adding a capacitor on PGDL. Select a capacitor for PGDL using Equation (1):

$$C_{PGDL}(nF) = \frac{t_{PGDL}(ms) \times I_{PGDL}(\mu A)}{V_{th\_PGDL}(V)} \quad (1)$$

Where t_{PGDL} is the desired delay time when PG asserts high, I_{PGDL} is the PGDL charging current, and V_{th_PGDL} is 1.65V.

Figure 2 shows the power good timing.

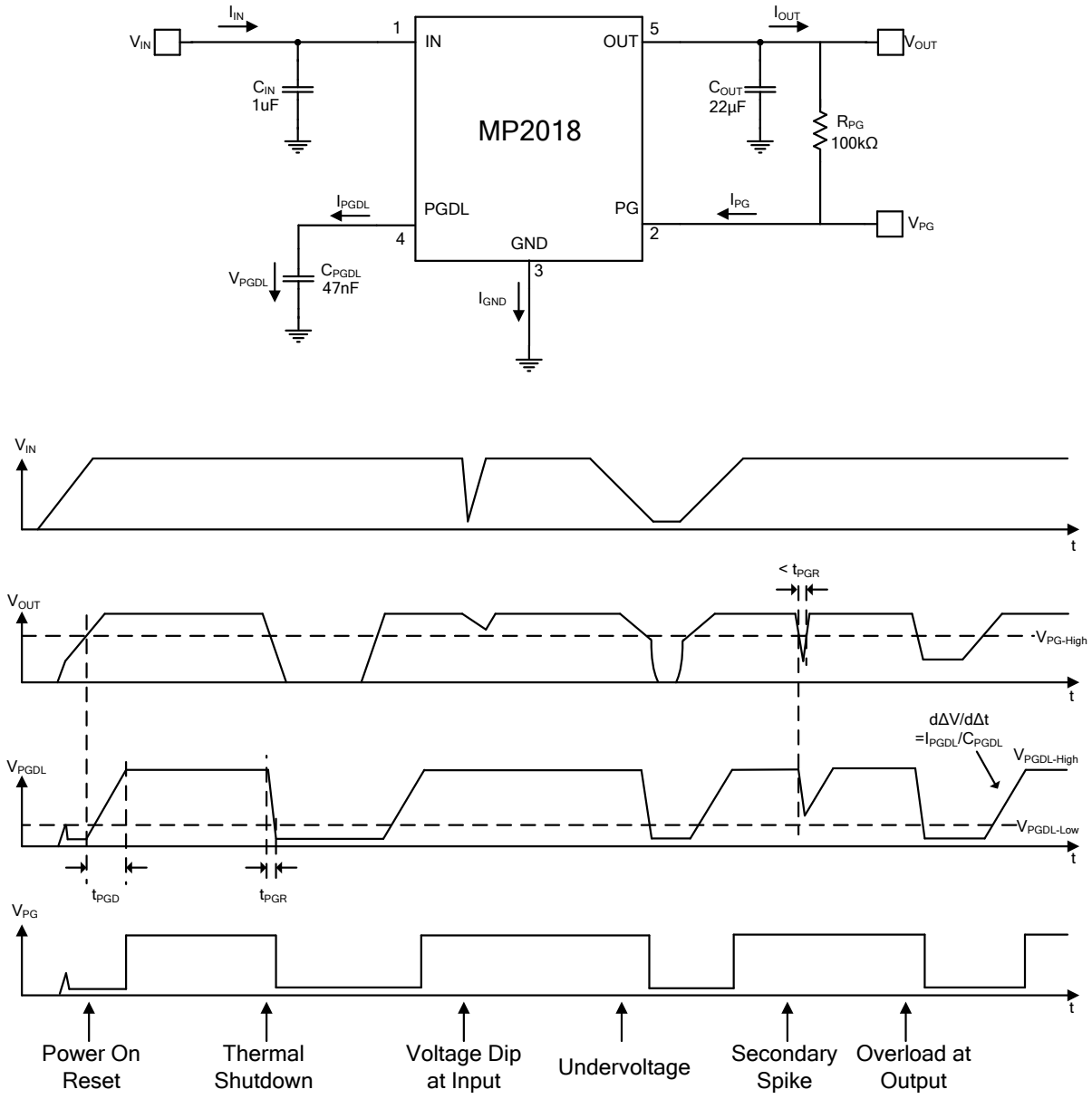


Figure 2: Power Good Timing

APPLICATION INFORMATION

Selecting the Input Capacitor

For proper operation, place a dielectric type X5R or X7R ceramic capacitor between 1 - 10µF (C1) between the input pin and ground. Larger values in this range help improve line transient response.

Selecting the Output Capacitor

For stable operation, use a dielectric type X5R or X7R ceramic capacitor (C2) between 1 - 22µF. Larger values in this range help improve load transient response and reduce noise. Output capacitors of other dielectric types may be used but are not recommended since their capacitance can deviate greatly from their rated value over temperature.

PCB Layout Guidelines

Efficient PCB layout is critical for good regulation, ripple rejection, transient response, and thermal performance. It is highly recommended to duplicate the EVB layout for optimal performance. For best results, refer to Figure 3, Figure 4, and follow the guidelines below.

1. Place the input and output bypass ceramic capacitors close to IN and OUT respectively.
2. Connect IN, OUT, and especially GND to a large copper area to cool the chip and improve thermal performance and long-term reliability.

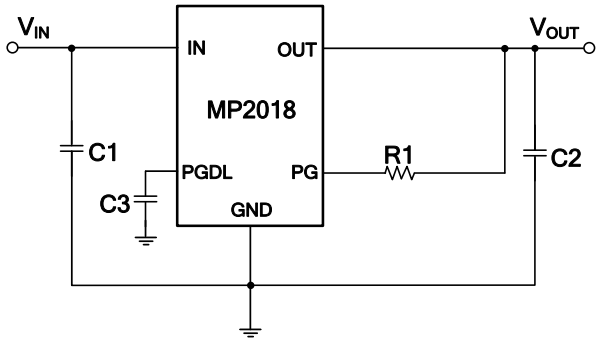
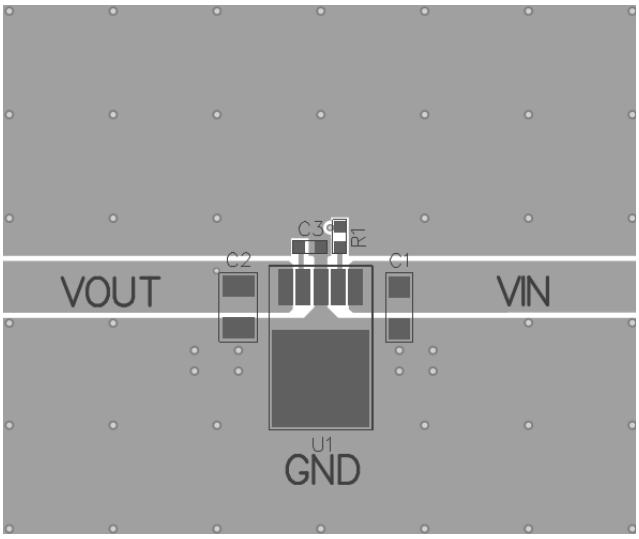
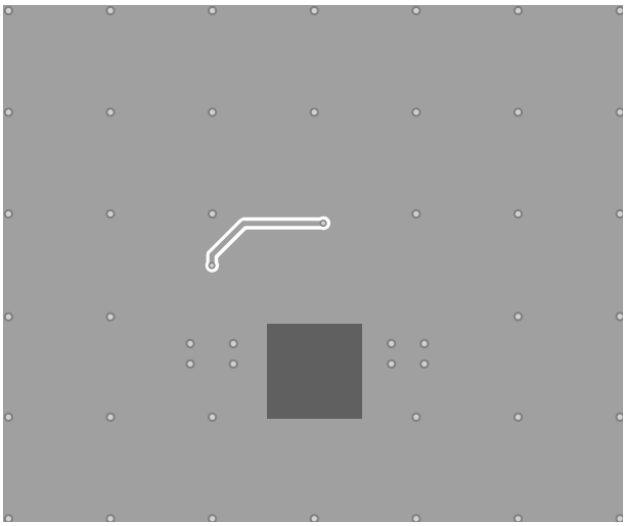


Figure 3: MP2018 Schematic



Top Layer



Bottom Layer

Figure 4: Recommended Layout

Design Example

Figure 5 shows a design example following the application guidelines.

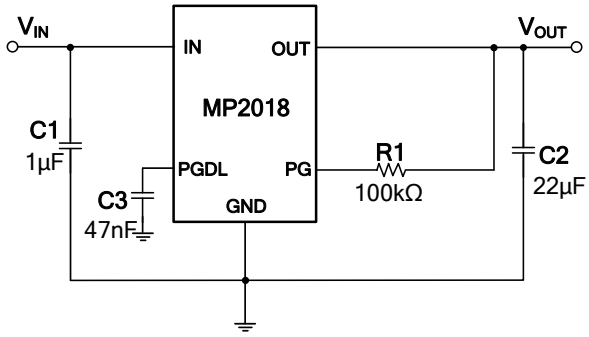


Figure 5: Design Example

TYPICAL APPLICATION CIRCUIT

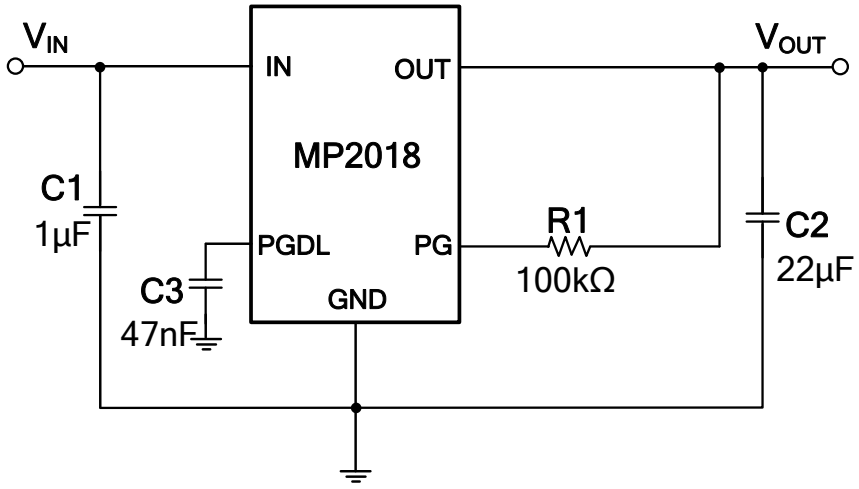
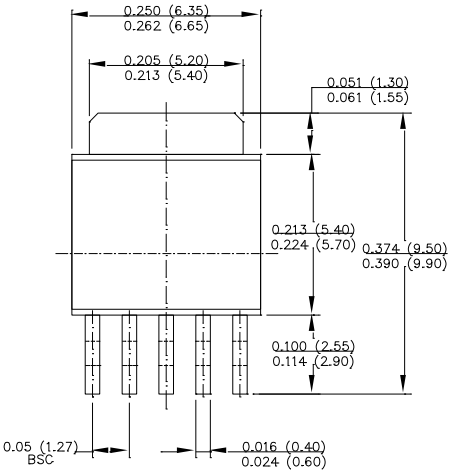


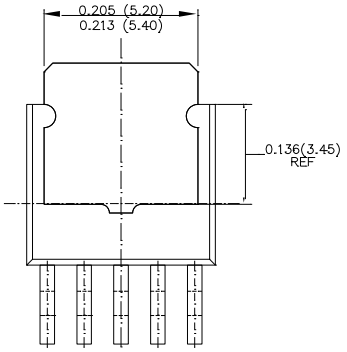
Figure 6: Typical Application Circuit

PACKAGE INFORMATION

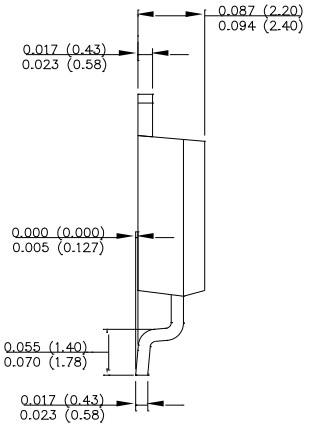
TO252-5



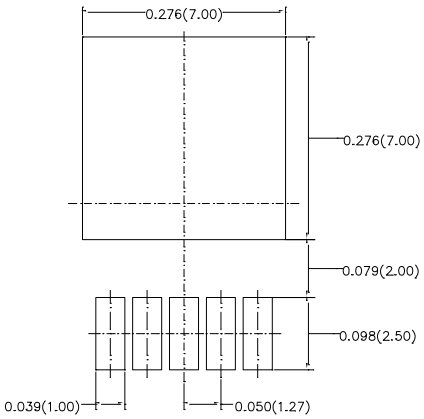
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) DRAWING CONFORMS TO JEDEC TO-252.
5) DRAWING IS NOT TO SCALE.