

DESCRIPTION

The MP2615A is a high-efficiency, switch mode battery charger suitable for 1- or 2- cell lithium-ion or lithium-polymer applications. The MP2615A is capable of delivering 2 A of charge current programmable via an accurate sense resistor over the entire input range.

The MP2615A regulates the charge current and full battery voltage using two control loops to achieve high-accuracy constant current (CC) charge and constant voltage (CV) charge.

Constant-off-time (COT) control allows operation at up to 99% duty cycle when the battery voltage is close to the input voltage, ensuring the charge current always remains at a relatively high level.

The battery temperature and charging status are always monitored during each charging cycle. Two status monitor output pins are provided to indicate the battery charging status and input power status. Also, the MP2615A features internal reverse-blocking protection.

The MP2615A is available in a 3mm × 3mm 16-pin QFN package.

FEATURES

- 4.75 V to 18 V Operating Input Voltage
- Up to 99% Duty Cycle Operation
- Up to 2 A Programmable Charging Current
- ±0.75% Full Battery Voltage Accuracy
- 4.2 V/Cell and 4.35 V/Cell Selection for Full Battery Voltage
- Fully Integrated Power Switches
- Internal Loop Compensation
- No External Reverse-Blocking Diode Required
- Preconditioning for Fully Depleted Battery
- Charging Operation Indicator
- Programmable Safety Timer
- Thermal Shutdown Protection
- Cycle-by-Cycle Over-Current Protection
- Battery Temperature Monitor and Protection

APPLICATIONS

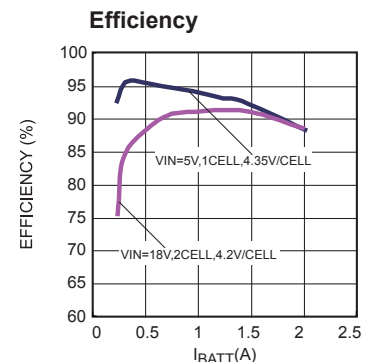
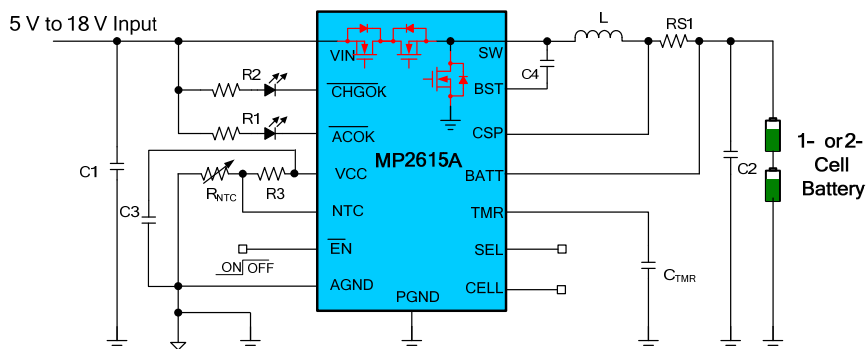
- Smart Phones
- Portable Hand-Held Solutions
- Portable Media Players

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2615AGQ	QFN-16 (3mm × 3mm)	See Below

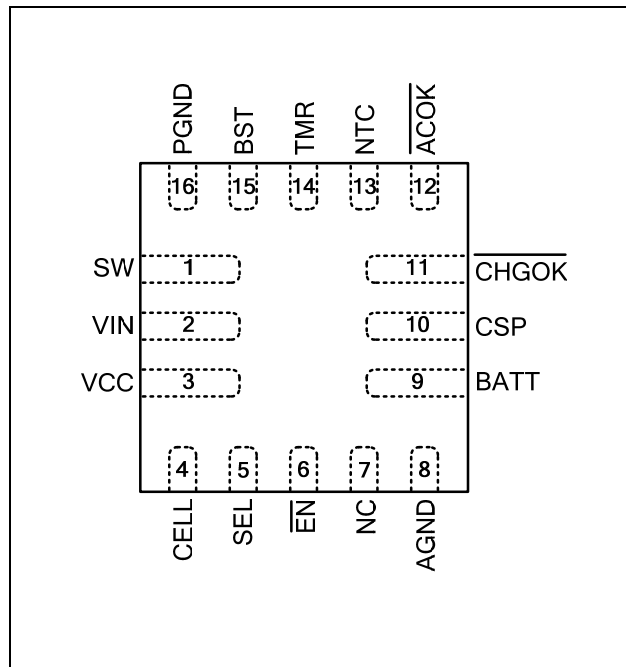
* For Tape & Reel, add suffix –Z (e.g. MP2615AGQ–Z).

TOP MARKING

ANKY
 LLL

ANK: Product code of MP2615A
 Y: Year code
 LLL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

V_{SW}	-0.3 V to 23 V
$V_{IN}, V_{ACOK}, V_{CHGOK}$	-0.3 V to 23 V
V_{BATT}, V_{CSP}	-0.3 V to 12 V
V_{BST}	$V_{SW} + 6$ V
All other pins.....	-0.3 V to 6 V
Junction temperature.....	150°C
Lead temperature.....	260°C
Continuous power dissipation ($T_A = +25^\circ\text{C}$) ⁽²⁾	2.5 W
Operating temperature.....	-40°C to +85°C

Recommended Operating Conditions ⁽³⁾

V_{IN}	4.75 V to 18 V
V_{BATT}	2 V to 8.7 V
Operating junction temp. (T_J)..	-40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
QFN-16 (3mm x 3mm).....	50.....	12... °C/W

NOTES:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX)- T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 12\text{ V}$, $V_{CELL} = 0\text{ V}$, $V_{SEL} = 0\text{ V}$, $C1 = 22\text{ }\mu\text{F}$, $C2 = 22\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage and current						
Input voltage	V_{IN}	$V_{CELL} = 4\text{ V}$	4.5	5	18	V
		$V_{CELL} = 0\text{ V}$	8.75	12	18	
Under-voltage lockout threshold rising	V_{UVLO}		3.55	3.75	3.95	V
Under-voltage lockout threshold hysteresis				225		mV
Supply current	I_{SHDN}	$\overline{EN} = 4\text{ V}$, Shutdown current		0.27		mA
	I_Q	$\overline{EN} = 0\text{ V}$, Quiescent current		1.1		
Power MOS						
High-side switch on resistance	$R_{H_DS(ON)}$	Measured from VIN to SW		110		m Ω
Low-side switch on resistance	$R_{L_DS(ON)}$			110		m Ω
Switch leakage		$\overline{EN} = 4\text{ V}$, $V_{SW} = 0\text{ V}$		0	1	μA
Frequency and time parameter						
Switching frequency	F_{SW}	$V_{BATT} = 7.5\text{ V}$		760		kHz
Foldback frequency		$V_{BATT} = 0\text{ V}$		160		kHz
Minimum off time ⁽⁵⁾	T_{OFF}	$V_{BATT} = 9\text{ V}$		200		ns
Charging parameter						
Terminal battery voltage	V_{BATT_FULL}	$V_{SEL} = 0\text{ V}$	4.328	4.35	4.386	V/Cell
		$V_{SEL} = 4\text{ V}$	4.168	4.2	4.252	
Battery over-voltage threshold	V_{BOVP}	$V_{SEL} = 0\text{ V}$ $V_{CELL} = 0\text{ V}$	8.62	8.99	9.36	V
		$V_{SEL} = 4\text{ V}$ $V_{CELL} = 0\text{ V}$	8.34	8.71	9.08	
		$V_{SEL} = 0\text{ V}$ $V_{CELL} = 4\text{ V}$	4.3	4.49	4.67	
		$V_{SEL} = 4\text{ V}$ $V_{CELL} = 4\text{ V}$	4.17	4.36	4.54	
Recharge threshold at V_{BATT}	V_{RECH}	$V_{SEL} = 0\text{ V}$		4.1		V/Cell
		$V_{SEL} = 4\text{ V}$		4.0		
Recharge hysteresis				150		mV/Cell
Trickle charge voltage threshold	V_{TC}	$V_{SEL} = 0\text{ V}$		3.1		V/Cell
		$V_{SEL} = 4\text{ V}$		3.0		
Trickle charge hysteresis				225		mV/Cell
Peak current limit		CC	3.2			A
		Trickle		2.2		
CC current	I_{CC}	$RS1 = 50\text{ m}\Omega$	1.8	2	2.2	A
Trickle charge current	I_{TC}		5%	10%	15%	I_{CC}

ELECTRICAL CHARACTERISTICS (continued)
 $V_{IN} = 12\text{ V}$, $V_{CELL} = 0\text{ V}$, $V_{SEL} = 0\text{ V}$, $C1 = 22\ \mu\text{F}$, $C2 = 22\ \mu\text{F}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Termination current threshold	I_{BF}		5%	10%	15%	I_{CC}
V_{IN} minimum head-room (reverse blocking)		$V_{IN} - V_{BATT}$		300		mV
Maximum current-sense voltage (CSP to BATT)	V_{SENSE}		90	100	110	mV
CSP, BATT current	I_{CSP} , I_{BATT}	Charging disabled			3	μA
ACOK/CHGOK open-drain sink current		$V_{DRAIN} = 0.3\text{ V}$	5			mA
VCC regulator output						
VCC output voltage	V_{CC}		4.25	4.5	4.75	V
VCC load regulation	ΔV_{CC}	$I_{LOAD} = 0\text{ to }10\text{ mA}$			10	mV
EN control						
\overline{EN} input low voltage					0.4	V
\overline{EN} input high voltage			1.8			V
\overline{EN} input current	I_{EN}	$\overline{EN} = 4\text{ V}$		4		μA
		$\overline{EN} = 0\text{ V}$		0.2		
Timer protection						
Trickle charge time	$t_{Trickle_tmr}$	$C_{TMR} = 0.47\ \mu\text{F}$		30		Mins
CC/CV charge time	t_{Total_tmr}	$C_{TMR} = 0.47\ \mu\text{F}$		165		
NTC protection						
NTC low temp rising threshold		$R_{NTC} = \text{NCP18 x } 103, 0^\circ\text{C}$	72	73.3	74.6	% V_{CC}
NTC low temp rising threshold hysteresis				2		
NTC high temp falling threshold		$R_{NTC} = \text{NCP18 x } 103, 50^\circ\text{C}$	28	29.3	30.6	
NTC low temp falling threshold hysteresis				2		
Thermal protection						
Thermal shutdown ⁽⁵⁾	T_{SHDN}			150		$^\circ\text{C}$
Thermal shutdown hysteresis ⁽⁵⁾				20		$^\circ\text{C}$
Reverse leakage blocking						
Battery reverse leakage current	$I_{LEAKAGE}$	$V_{CELL} = 0\text{ V}$			3	μA
		$V_{CELL} = 4\text{ V}$			0.5	μA

NOTES:

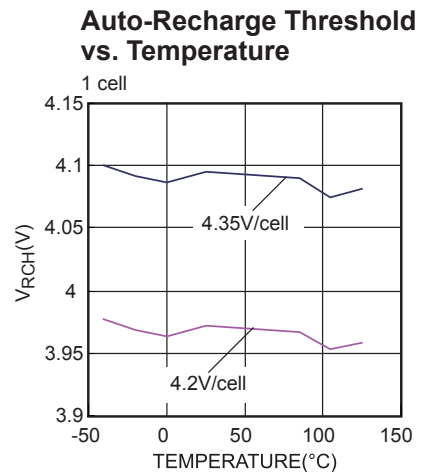
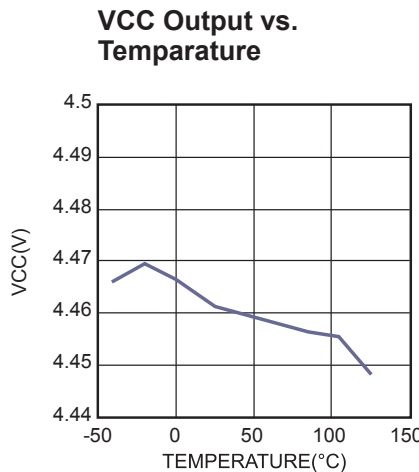
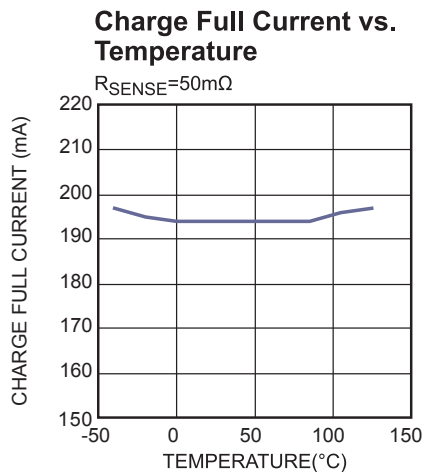
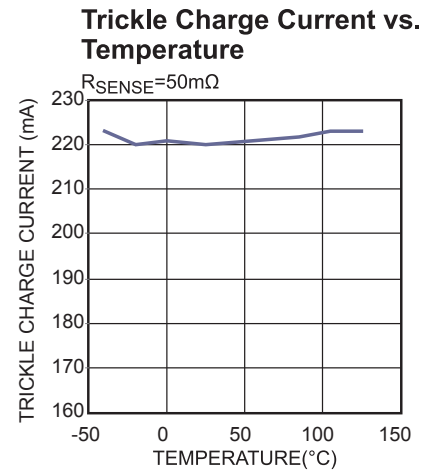
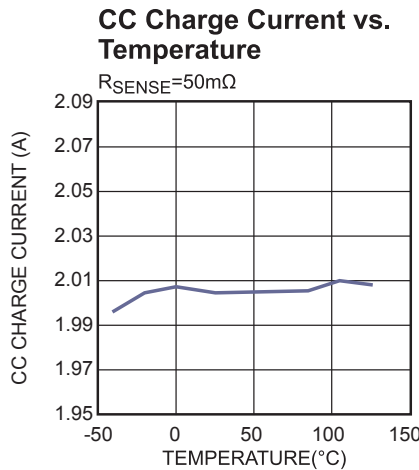
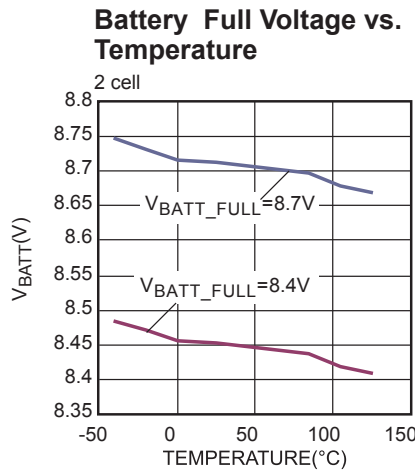
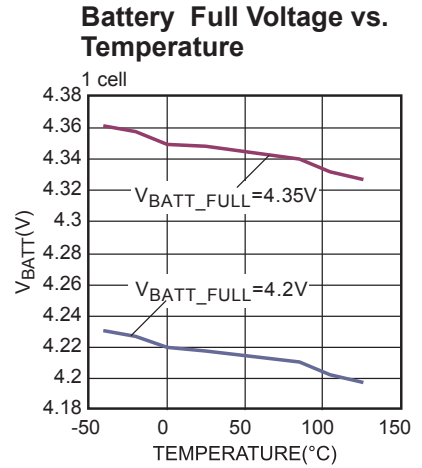
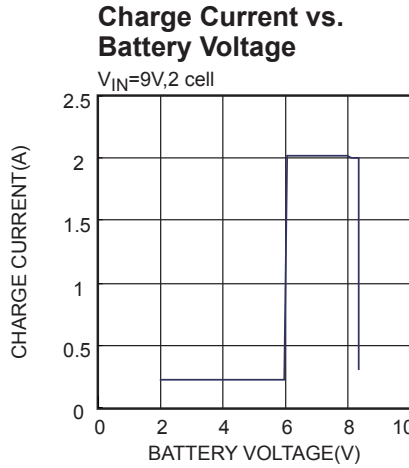
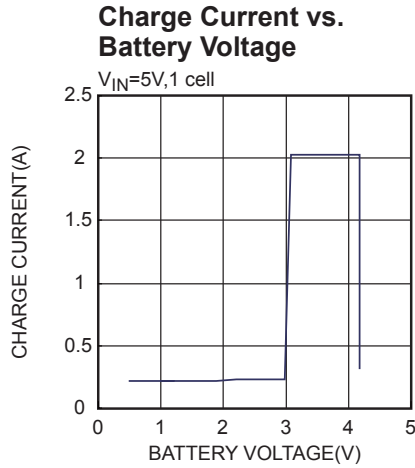
5) Guaranteed by design.

PIN FUNCTIONS

Package Pin #	Name	Description
1	SW	Switch output.
2	VIN	Power supply voltage.
3	VCC	Coarse regulator output. Internally generated 4.5 V. Bypass with a 1 μ F capacitor to AGND. Used as low-side switch driver and pull-up bias voltage NTC resistive divider. Do NOT connect an external load to VCC.
4	CELL	Command input for the number of li-ion cells. Connect CELL to VCC for 1-cell application; short CELL to AGND for 2-cell application.
5	SEL	Input pin for setting terminal battery voltage: SEL = Low-level: $V_{BATT} = 4.35$ V/cell. SEL = High-level: $V_{BATT} = 4.2$ V/cell.
6	\overline{EN}	On/off control input. \overline{EN} is pulled to GND with a 1 M internal resistor.
7	NC	No connection. Please leave NC floating.
8	AGND	Analog ground.
9	BATT	Positive battery terminal.
10	CSP	Battery current sense positive input. Connect a resistor (RS1) between CSP and BATT.
11	\overline{CHGOK}	Charging complete indicator. A logic low indicates a charging operation. \overline{CHGOK} will become an open drain once the charge is completed or suspended.
12	\overline{ACOK}	Valid input supply indicator. A logic low on \overline{ACOK} indicates the presence of a valid input power supply.
13	NTC	Thermistor input. Connect a resistor from NTC to VCC and the thermistor from NTC to ground.
14	TMR	Internal safety timer control. Connect a capacitor from this node to AGND to set the timer. The timer can be disabled by connecting TMR to AGND directly.
15	BST	Bootstrap. A capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BST to form a floating supply across the power switch driver.
16	PGND	Power ground.

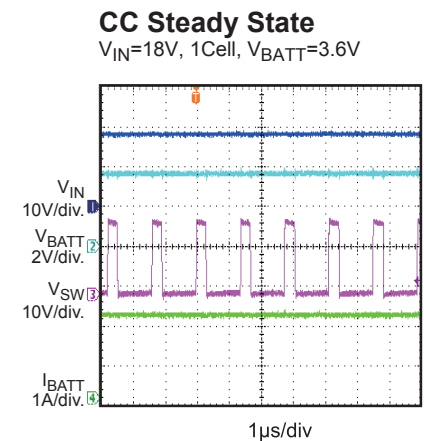
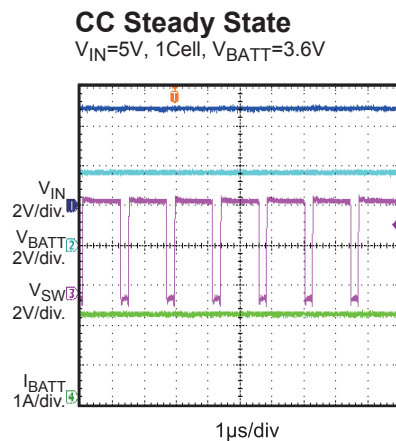
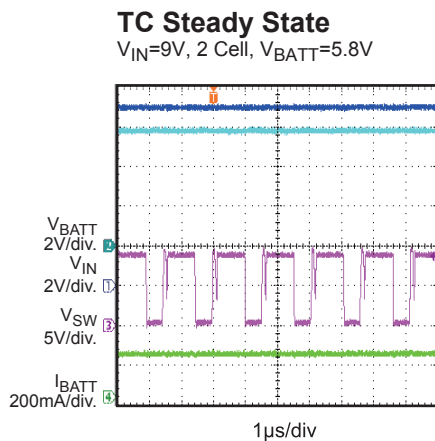
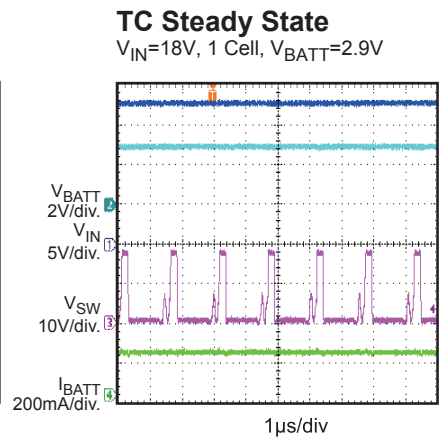
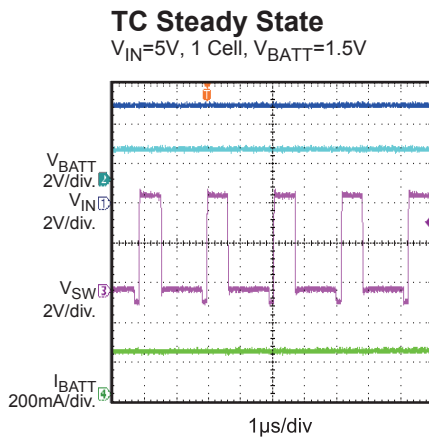
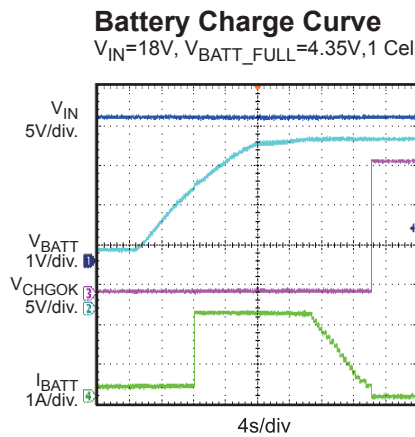
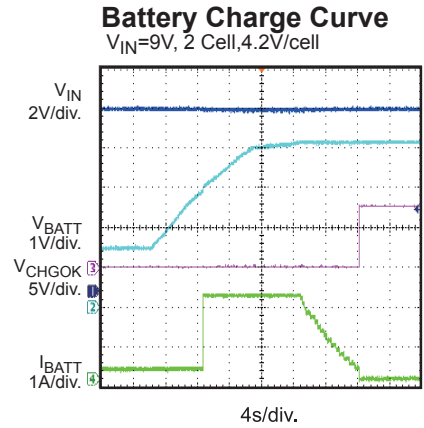
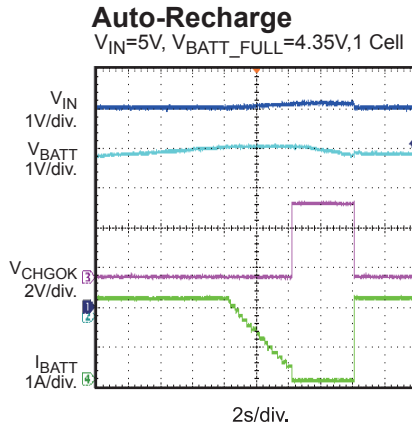
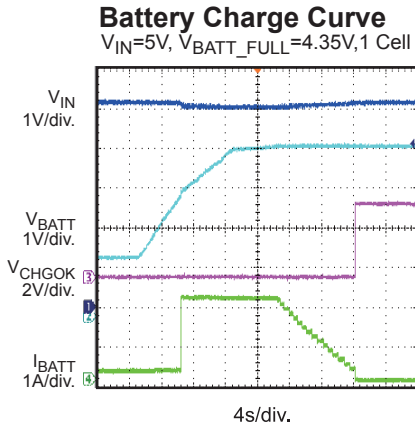
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 5 \text{ V/9 V}$, $C1 = C2 = 22 \mu\text{F}$, $\text{SEL} = \text{Low/High}$, $\text{CELL} = \text{Low/High}$, $L = 6.8 \mu\text{H}$, $\text{RS1} = 50 \text{ m}\Omega$, battery simulator, $T_A = 25^\circ\text{C}$, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 5\text{ V}/9\text{ V}$, $C1 = C2 = 22\ \mu\text{F}$, $SEL = \text{Low/High}$, $CELL = \text{Low/High}$, $L = 6.8\ \mu\text{H}$, $RS1 = 50\ \text{m}\Omega$, battery simulator, $T_A = 25^\circ\text{C}$, unless otherwise noted.

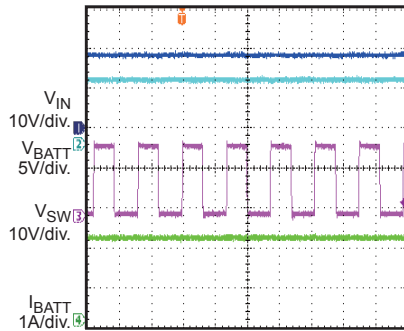


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 5 \text{ V/9 V}$, $C1 = C2 = 22 \mu\text{F}$, $\text{SEL} = \text{Low/High}$, $\text{CELL} = \text{Low/High}$, $L = 6.8 \mu\text{H}$, $R_{S1} = 50 \text{ m}\Omega$, battery simulator, $T_A = 25^\circ\text{C}$, unless otherwise noted.

CC Steady State

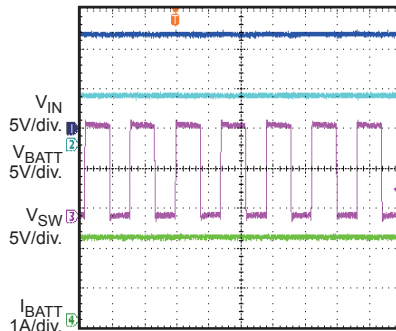
$V_{IN}=18\text{V}$, 2Cell, $V_{BATT}=8.0\text{V}$



1µs/div.

CC Steady State

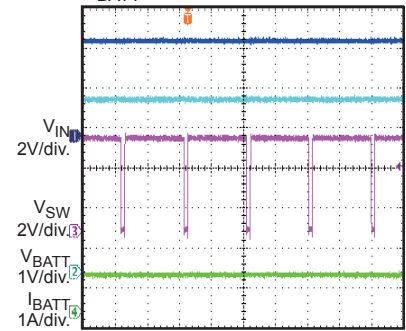
$V_{IN}=12\text{V}$, 2Cell, $V_{BATT}=6\text{V}$



1µs/div.

CC Steady State (COT)

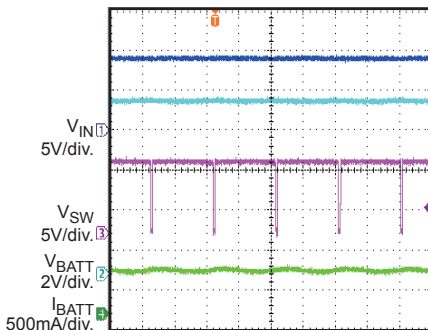
$V_{IN}=4.75\text{V}$, 1Cell, 4.35V/cell, $V_{BATT}=4.1\text{V}$



2µs/div.

CC Steady State (BST Refresh)

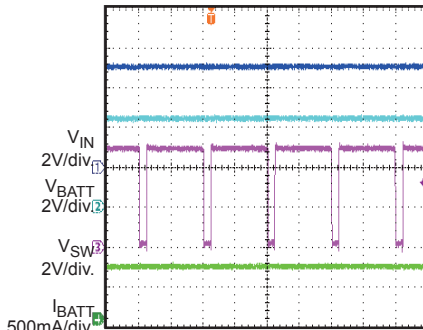
$V_{IN}=9.0\text{V}$, 2Cell, 4.35V/cell, $V_{BATT}=8.67\text{V}$



4µs/div

CV Steady State

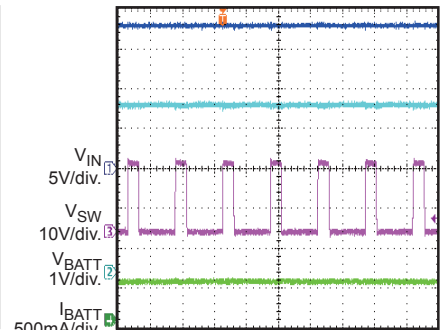
$V_{IN}=5\text{V}$, 1Cell, $V_{BATT}=4.35\text{V}$



1µs/div

CV Steady State

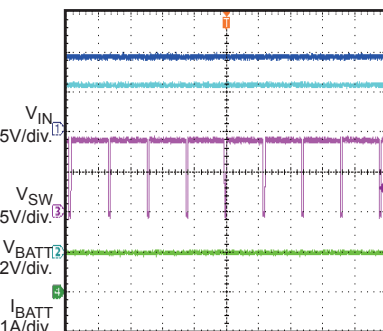
$V_{IN}=18\text{V}$, 1Cell, $V_{BATT}=4.2\text{V}$



1µs/div

CV Steady State (COT)

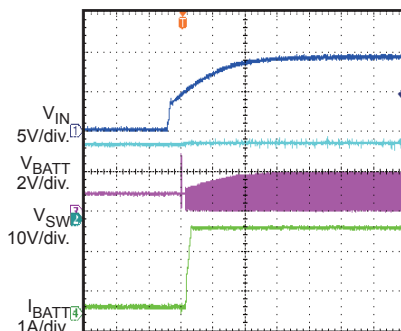
$V_{IN}=9\text{V}$, 2Cell, $V_{BATT}=8.4\text{V}$



2µs/div

Power On

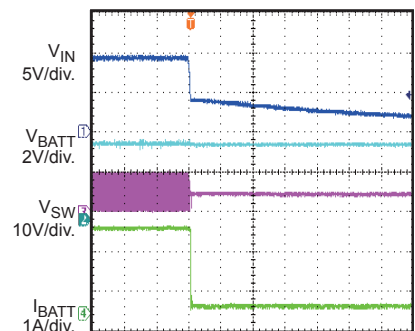
$V_{IN}=9\text{V}$, 1Cell, $V_{BATT}=3.6\text{V}$



2ms/div

Power Off

$V_{IN}=5\text{V}$, 1Cell, $V_{BATT}=3.6\text{V}$



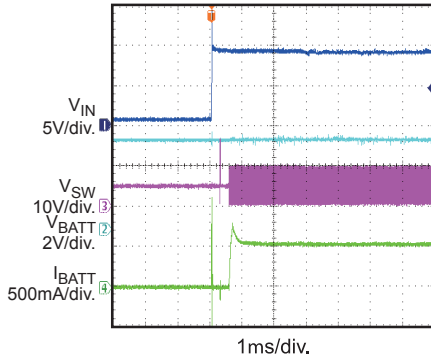
20ms/div

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

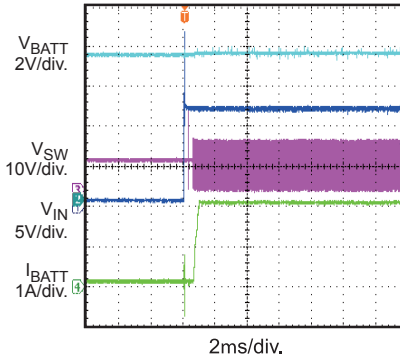
$V_{IN} = 5 \text{ V}/9 \text{ V}$, $C1 = C2 = 22 \mu\text{F}$, SEL = Low/High, CELL = Low/High, $L = 6.8 \mu\text{H}$, $RS1 = 50 \text{ m}\Omega$, battery simulator, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Hot Insertion

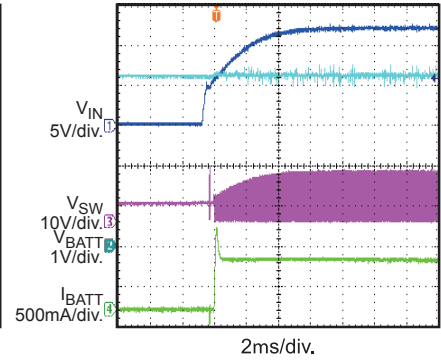
$V_{IN} = 9\text{V}$, 1 Cell, $V_{BATT} = 4.35\text{V}$


Hot Insertion

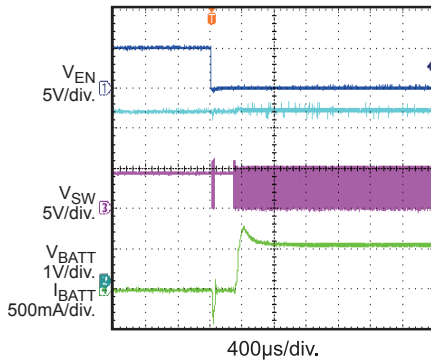
$V_{IN} = 12\text{V}$, 2 Cell, $V_{BATT} = 7.2\text{V}$


Power On

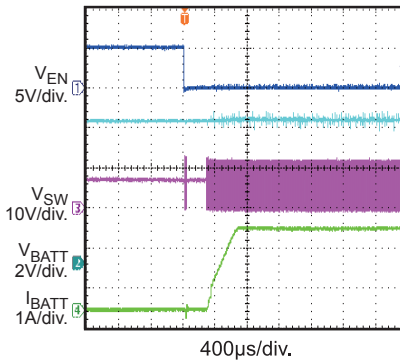
$V_{IN} = 12\text{V}$, 1 Cell, $V_{BATT} = 4.2\text{V}$


EN On

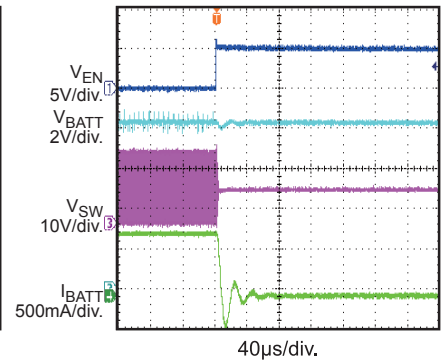
$V_{IN} = 5\text{V}$, 1 Cell, $V_{BATT} = 4.35\text{V}$


EN On

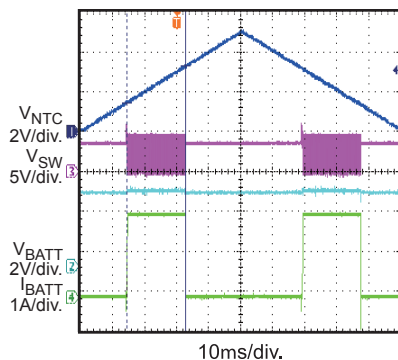
$V_{IN} = 12\text{V}$, 2 Cell, $V_{BATT} = 7.2\text{V}$


EN Off

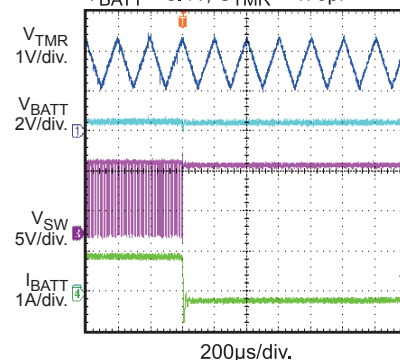
$V_{IN} = 18\text{V}$, 2 Cell, $V_{BATT} = 8.4\text{V}$


NTC Fault Control

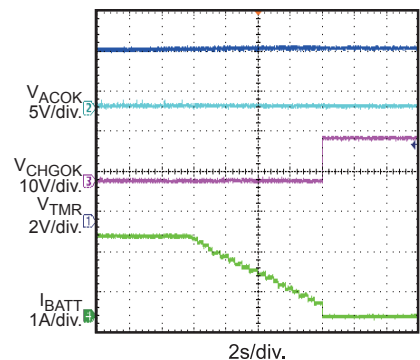
$V_{IN} = 5\text{V}$, 1 Cell, $V_{BATT} = 3.6\text{V}$


Timer Out

$V_{IN} = 9\text{V}$, 2 Cell,
 $V_{BATT} = 8.4\text{V}$, $C_{TMR} = 470\text{pF}$


Charge Full Indication

$V_{IN} = 12\text{V}$, 2 Cell, $V_{BATT} = 8.4\text{V}$



FUNCTIONAL BLOCK DIAGRAM

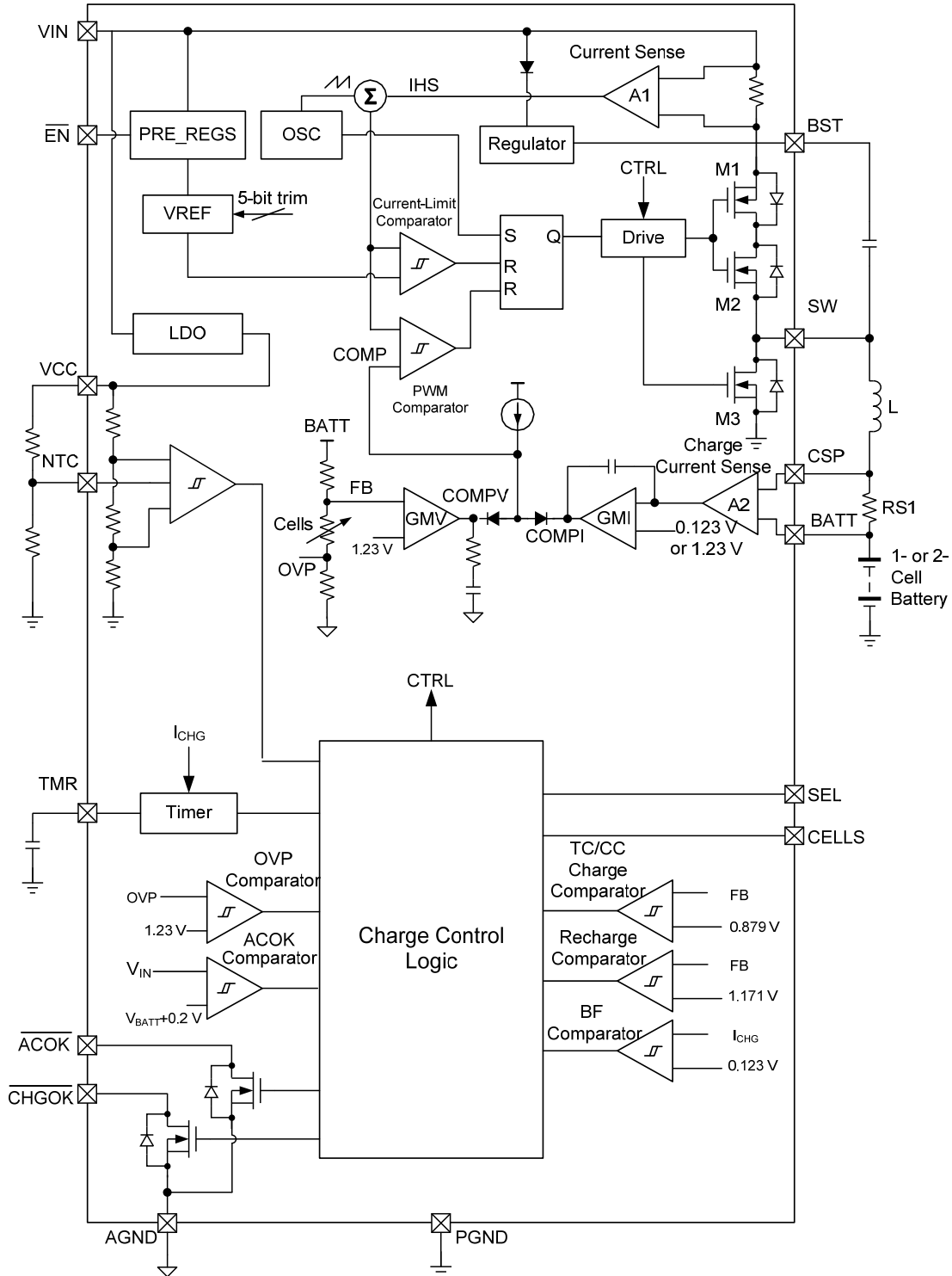


Figure 1—Functional block diagram

OPERATION

The MP2615A is a peak current mode controlled switching charger for 1- or 2- cell lithium-ion and lithium-polymer batteries. The MP2615A integrates both the high-side and low-side switches of the synchronous buck converter to provide high efficiency and save space on the PCB.

Charge Cycle (Mode Change: TC→ CC→ CV)

The MP2615A regulates the charge current (I_{CHG}) and battery voltage (V_{BATT}) using two control loops. This achieves highly-accurate constant current (CC) charge and constant voltage (CV) charge.

As shown in Figure 2, when the $V_{BATT} < V_{TC}$, the MP2615A stays in trickle-charge mode, and the output of the charge current loop (COMPI) dominates the control. The battery is charged by

a trickle-charge current (I_{TC}) until the battery voltage reaches V_{TC} . If the charger stays in the trickle-charge mode until the trickle-charge timer is triggered, charging will be terminated.

The MP2615A enters constant-current charge mode once the battery voltage rises higher than V_{TC} . In this mode, the charge current increases from I_{TC} to I_{CC} to fast charge the battery.

When the battery voltage rises over the full battery voltage (V_{BATT_FULL}), the charger enters constant-voltage mode. In constant-voltage mode, the battery voltage is regulated at V_{BATT_FULL} precisely, and the charge current decreases naturally due to the existing equivalent internal resistance of the battery. For the operation flow chart, please refer to Figure 4.

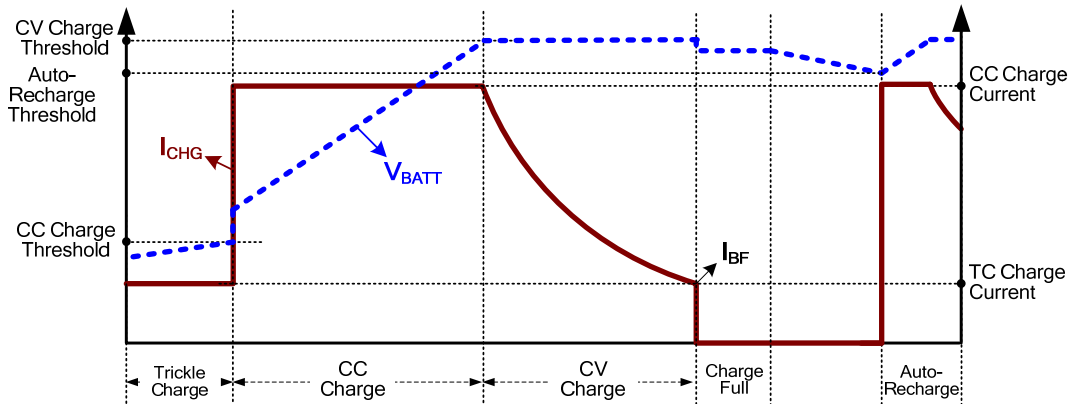


Figure 2—Li-ion battery charge profile

Charge Full Termination and Auto-Recharge

When the charge current drops below the termination threshold (I_{BF}) during the CV charge phase, the charger stops charging and \overline{CHGOK} becomes an open drain. Also, the timer is re-set and turns off. Once the battery voltage decreases below the recharge threshold (V_{RECH}), recharging kicks in automatically, and the timer re-starts a new charge cycle.

COT Charge Mode

The MP2615A uses the floating ground method to drive the high-side MOSFET (HS-FET) of the buck converter. During the HS-FET off time, the BST capacitor is recharged, and the voltage across the BST capacitor is used as the HS-FET gate drive. Thus a minimum off-time (200ns) is required to maintain sufficient voltage at the BST capacitor.

When the 200ns minimum off-time is achieved, due to a large duty cycle, the MP2615A enters constant off-time (COT) charge mode. In this mode of operation, the switching frequency is decreased slightly in order to achieve a 99% duty cycle.

Charge Status Indication

The MP2615A has two open-drain status outputs: \overline{CHGOK} and \overline{ACOK} . \overline{ACOK} goes low when the input voltage is 300 mV larger than the battery voltage, and it rises above the under-voltage lockout threshold. \overline{CHGOK} indicates the status of the charge cycle. Table 1 summarizes the operation of both \overline{CHGOK} and \overline{ACOK} according to the charging status.

Table 1—Charging status indication

\overline{ACOK}	\overline{CHGOK}	Charger Status
Low	Low	In charging
Low	High impedance	End of charge NTC fault Timer out \overline{EN} disable Thermal shutdown
High impedance	High impedance	V_{IN} absent $V_{IN} - V_{BATT} < 0.3 V$

Safety Timer Operation

The MP2615A has an internal safety timer to terminate charging during time out. The capacitor (C_{TMR}) connected between TMR and GND is used to set the internal oscillator period. See Equation (1):

$$T_p(\text{seconds}) = 0.46 \times C_{TMR}(\mu\text{F}) \quad (1)$$

This timer limits the maximum trickle charge time to 8192 internal oscillating periods. If the charger stays in trickle-charge mode for longer than the maximum oscillating periods, it is terminated.

\overline{CHGOK} becomes an open drain to indicate the timer-out fault. If the charge cycle goes through the trickle charge successfully within the allowed time limit, it enters CC charge mode, and the timer continues to count the oscillating periods. When the battery is fully charged, the timer turns off and clears the counter, waiting for the auto-recharge to re-start.

If the charge time during the CC/CV modes exceed 49152 oscillating periods, and the *battery full* has not been qualified, the charger is terminated, and a timer-out fault is indicated by floating \overline{CHGOK} . The charger exits the timer-out fault state, and the on-chip safety timer re-starts counting when the following conditions occur:

- The battery voltage falls below the auto-recharge threshold (V_{RECH});
- a power-on-reset (POR) event occurs;
- \overline{EN} is toggled.

The timer can be disabled by pulling TMR to AGND.

Thus, the trickle mode charge time is calculated using Equation (2):

$$t_{\text{Trickle_tmr}}(\text{minutes}) = 62.8 \times C_{TMR}(\mu\text{F}) \quad (2)$$

If a C_{TMR} (0.47 μF) is connected, the trickle charge time is about 30 minutes.

The CC/CV mode charge time is calculated with Equation (3):

$$t_{\text{Total_tmr}}(\text{hours}) = 6.28 \times C_{TMR}(\mu\text{F}) \quad (3)$$

If a C_{TMR} (0.47 μF) is connected, the CC/CV charge time is 2.95 hours.

Negative Thermal Coefficient (NTC) Thermistor

NTC allows the MP2615A to sense the battery temperature using an negative thermal coefficient (NTC) resistor. This resistor is available in the battery pack to ensure a safe operating environment for the battery. A resistor with an appropriate value should be connected from VCC to NTC, and the thermistor should be connected from NTC to AGND. The voltage on NTC is determined by the resistor divider whose divide-ratio depends on the battery temperature. When the voltage at NTC falls out of the NTC window range, the charging will pause until the battery temperature goes back to normal operating conditions.

As a result, the MP2615A stops charging and reports this condition to the status pins. Charging resumes automatically after the temperature falls back within safe range.

Short-Circuit Protection

The MP2615A has an internal comparator to check for a battery short circuit. Once V_{BATT} falls below 2 V, the device detects a battery-short status, and the cycle-by-cycle peak current limit falls to about 2.2 A to limit the current spike during the battery-short transition. Also, the switching frequency folds back to minimize the power loss.

Thermal Shutdown Protection (TSD)

To prevent the chip from overheating during charging, the MP2615A monitors the junction temperature (T_J), of the die. Once T_J reaches the thermal shutdown threshold ($T_{SHUTDOWN}$) of 150°C, the charger converter turns off. Once T_J falls below 130°C the charging re-starts.

INPUT POWER-UP, START-UP TIMING FLOW

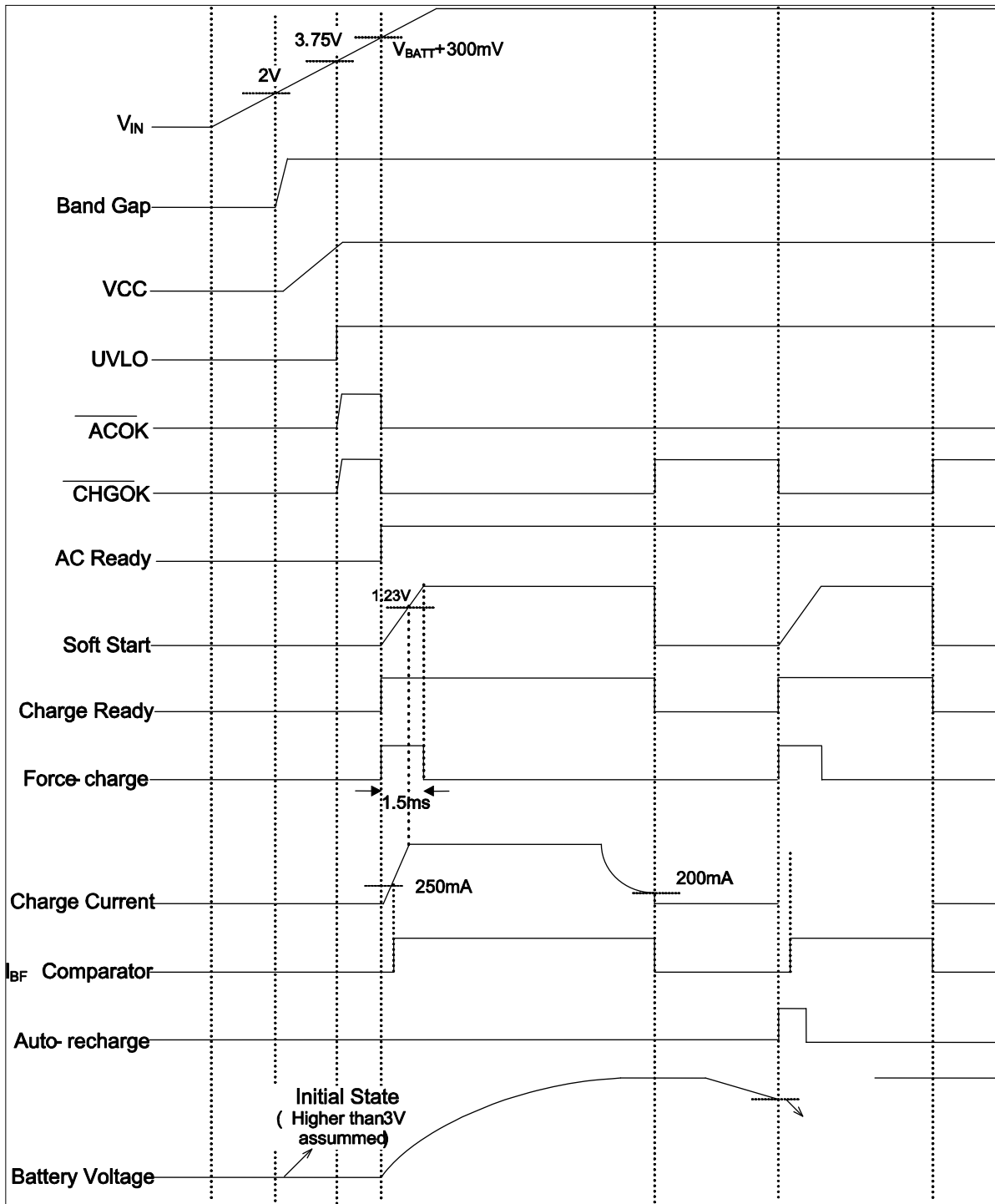


Figure 3—Input power start-up timing diagram

OPERATION FLOW CHART

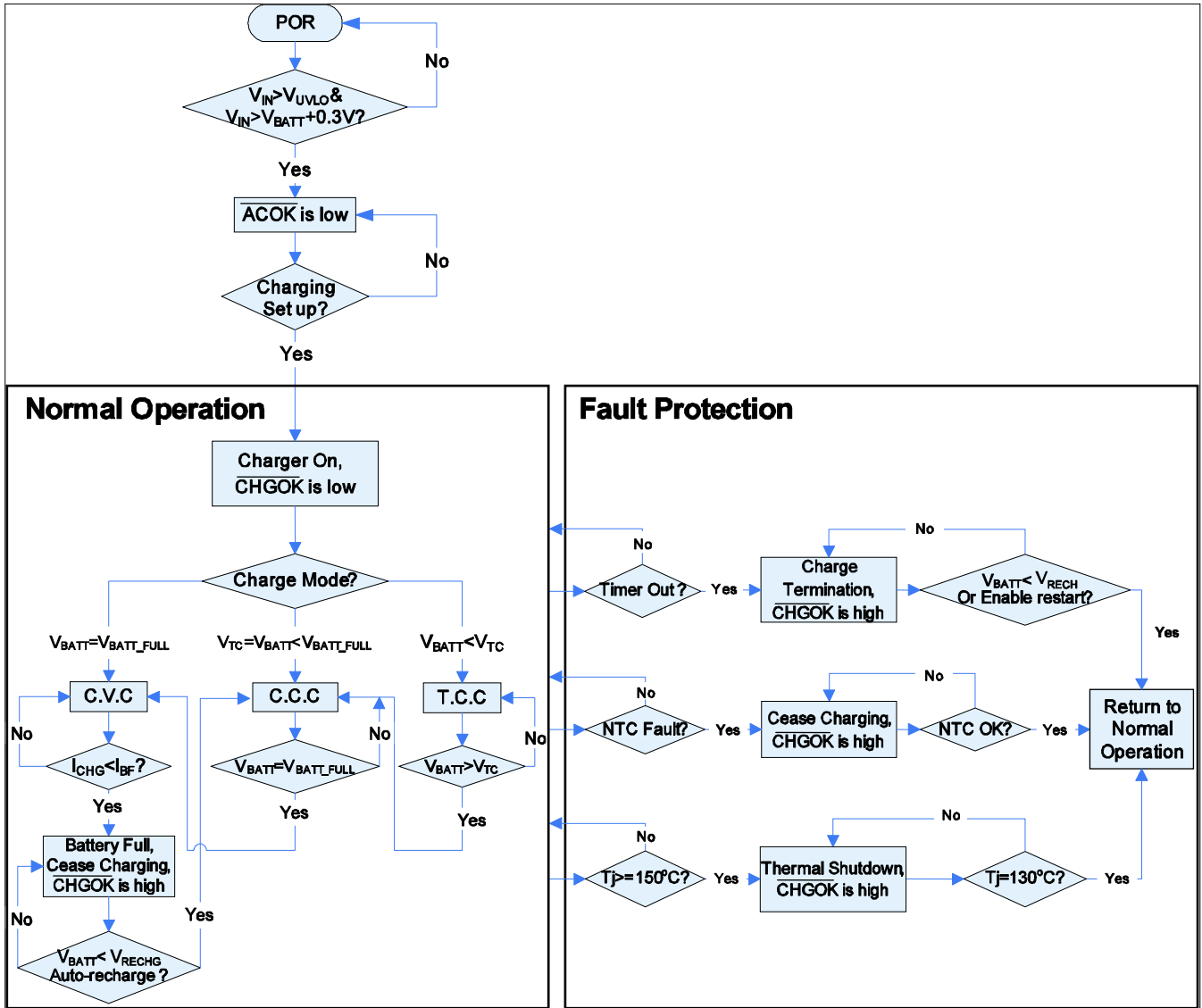


Figure 4—Operation flow chart

APPLICATION INFORMATION

COMPONENT SELECTION

Charge Current Setting

The constant charge current (I_{CC}) of the MP2615A can be set by the sense resistor RS1 (see Typical Application). The equation to determine the programmable CC charge current is expressed in Equation (4):

$$I_{CC} = \frac{100\text{mV}}{RS1(\text{m}\Omega)} \text{ (A)} \quad (4)$$

To get 2 A I_{CC} , a RS1 of 50 m Ω should be selected.

Accordingly, the trickle-charge current (I_{TC}) can be obtained using Equation (5):

$$I_{TC} = 10\%I_{CC} = \frac{10\text{mV}}{RS1(\text{m}\Omega)} \text{ (A)} \quad (5)$$

Inductor Selection

To select the right inductor, a trade off should be made between cost, size, and efficiency. An inductor with a lower inductance value corresponds with smaller size, but it results in higher ripple currents, higher magnetic hysteretic losses, and higher output capacitances. Conversely, a higher inductance value is beneficial to getting a lower ripple current and smaller output filter capacitors. However, this results in higher inductor DC resistance (DCR) loss. Based on practical experience, the inductor ripple current should not exceed 30% of the maximum charge current under worst cases. For the MP2615A with a typical 12 V input voltage to charge a 2-cell battery, the maximum inductor current ripple occurs at the corner point between the trickle charge and the CC charge ($V_{BATT} = 6 \text{ V}$). Inductance estimations are calculated with Equation (6):

$$L = \frac{V_{IN} - V_{BATT}}{\Delta I_{L_MAX}} \cdot \frac{V_{BATT}}{V_{IN} \cdot f_S} \quad (6)$$

Where V_{IN} , V_{BATT} , and f_S are the typical input voltage, the CC charge threshold, and the switching frequency, respectively. And ΔI_{L_MAX} is the maximum inductor ripple current, which is usually 30% of the CC charge current. See Equation (7):

$$\Delta I_{L_MAX} = 30\%I_{CC} \quad (7)$$

Based on the condition where $I_{CC} = 2 \text{ A}$, $V_{IN} = 12 \text{ V}$, $V_{BATT} = 6 \text{ V}$, and $f_S = 760 \text{ kHz}$, the calculated inductance is 6.6 μH . The inductor saturation current must exceed at least 2.6 A and have some tolerance. To optimize efficiency, chose an inductor with a DC resistance less than 50 m Ω .

NTC Resistor Divider Selection

Figure 5 shows that an internal resistor divider is used to set the low temperature threshold at 29.3%·VCC and the high temperature threshold at 73.3%·VCC, respectively. For a given NTC thermistor, select the appropriate R_{T1} and R_{T2} to set the NTC window.

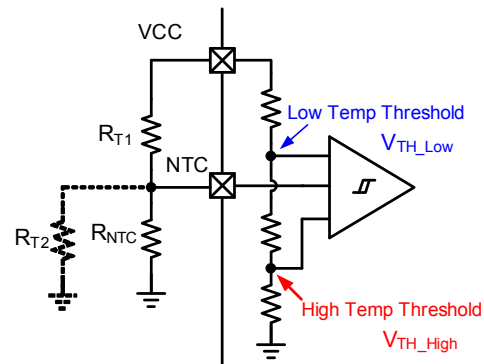


Figure 5—NTC function block

The thermistor (NCP18XH103) noted above has the following electrical characteristics:

- At 0°C, $R_{NTC_Cold} = 27.445 \text{ k}\Omega$;
- At 50°C, $R_{NTC_Hot} = 4.1601\text{k}\Omega$.

Equation (8) and Equation (9) are derived assuming that the NTC window is between 0°C and 50°C:

$$\frac{R_{T2} // R_{NTC_Cold}}{R_{T1} + R_{T2} // R_{NTC_Cold}} = \frac{V_{TH_Low}}{V_{REF33}} = 73.3\% \quad (8)$$

$$\frac{R_{T2} // R_{NTC_Hot}}{R_{T1} + R_{T2} // R_{NTC_Hot}} = \frac{V_{TH_High}}{V_{REF33}} = 29.3\% \quad (9)$$

Calculate R_{T1} and R_{T2} according to Equation (8) and Equation (9) and the required battery temperature range.

Input Capacitor Selection

The input capacitor C1 from the typical application circuit absorbs the maximum ripple current from the buck converter, which is given by Equation (10):

$$I_{\text{RMS_MAX}} = I_{\text{CC}} \frac{\sqrt{V_{\text{TC}}(V_{\text{IN_MAX}} - V_{\text{TC}})}}{V_{\text{IN_MAX}}} \quad (10)$$

For a given $I_{\text{CC}} = 2 \text{ A}$, and $V_{\text{TC}} = 6 \text{ V}$ when $V_{\text{IN_MAX}} = 12 \text{ V}$ (the duty is 0.5), the maximum ripple current is 1 A. Select the input capacitors so that the temperature rise due to the ripple current does not exceed 10°C . Use ceramic capacitors with X5R or X7R dielectrics because of their low ESR and small temperature coefficients. For most applications, use a $22 \mu\text{F}$ capacitor. A small, high-quality ceramic capacitor (i.e. $1.0 \mu\text{F}$) should be placed as close to the IC as possible from VIN to PGND.

Output Capacitor Selection

The output capacitor C2 (see the typical application circuit) is in parallel with the battery. C2 absorbs the high-frequency switching ripple current and smoothes the output voltage. Its impedance must be much less than that of the battery to ensure it absorbs the ripple current. Use a ceramic capacitor because it has a lower ESR and smaller size. The output voltage ripple is given by Equation (11):

$$\Delta r_o = \frac{\Delta V_o}{V_o} = \frac{1 - \frac{V_o}{V_{\text{IN}}}}{8C_o f_s^2 L} \quad (11)$$

In order to guarantee $\pm 0.5\%$ full battery voltage accuracy, the maximum output voltage ripple must not exceed 0.5% (e.g., 0.1%). The maximum output voltage ripple occurs at the minimum battery voltage of the CC charge and the maximum input voltage.

For $V_{\text{IN_MAX}} = 18 \text{ V}$, $V_{\text{CC_MIN}} = V_{\text{TC}} = 6 \text{ V}$, $L = 6.8 \mu\text{H}$, $f_s = 760 \text{ kHz}$, $\Delta r_{o_MAX} = 0.1\%$, the output capacitor can be calculated using Equation (12):

$$C_o = \frac{1 - \frac{V_{\text{TC}}}{V_{\text{IN_MAX}}}}{8f_s^2 L \Delta r_{o_MAX}} = 21.3 \mu\text{F} \quad (12)$$

We can then approximate this value and choose a $22 \mu\text{F}$ ceramic capacitor.

PCB Layout Guidelines

Efficient PCB layout is critical to meet specified noise, efficiency, and stability requirements. For optimum performance, refer to Figure 6 and follow the design considerations below:

- 1) Route the power stage adjacent to the grounds. Aim to minimize the high-side switching node (SW, inductor), trace lengths in the high-current paths, and the current-sense resistor trace. Keep the switching node short and far away from the feedback network.
- 2) Connect the charge current-sense resistor to CSP (pin 10) and BATT (pin 9). Minimize the length and area of this circuit loop.
- 3) Place the input capacitor as close as possible to VIN and PGND. Place the output inductor close to the IC and connect the output capacitor between the inductor and PGND of the IC. This minimizes the current path loop area from SW through the LC filter and back to PGND.
- 4) Connect AGND and PGND at a single point.

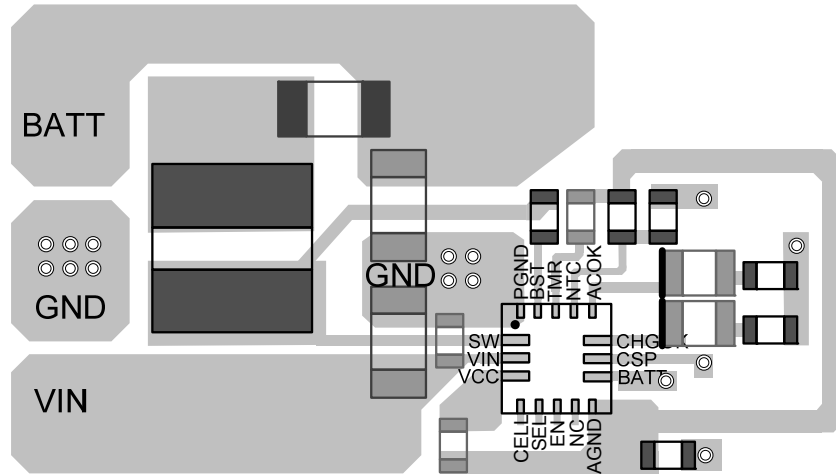


Figure 6—Recommended PCB layout

TYPICAL APPLICATION CIRCUITS

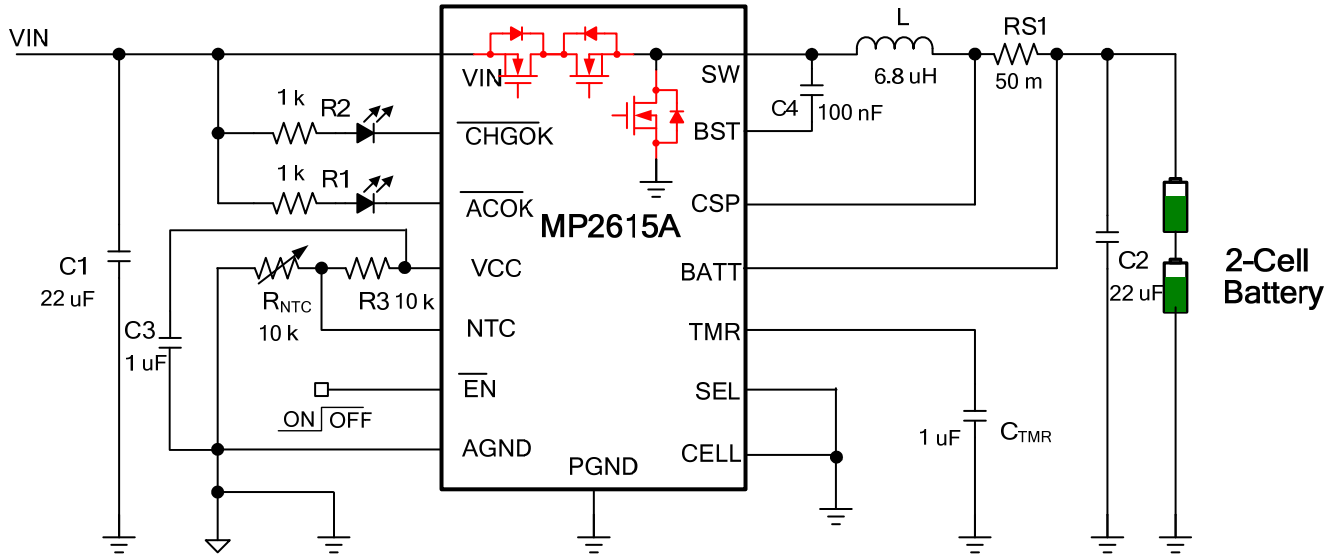
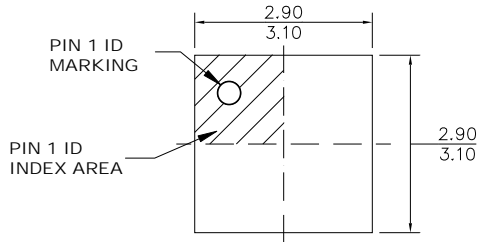
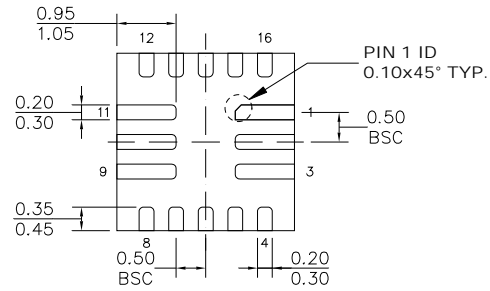
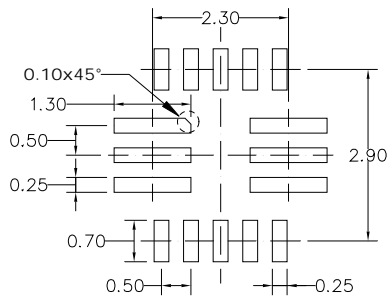


Figure 7—Typical application circuit to charge a 2-cell battery with 12 VIN.

PACKAGE INFORMATION
QFN-16 (3mm x 3mm)

TOP VIEW

BOTTOM VIEW

SIDE VIEW

RECOMMENDED LAND PATTERN
NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

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